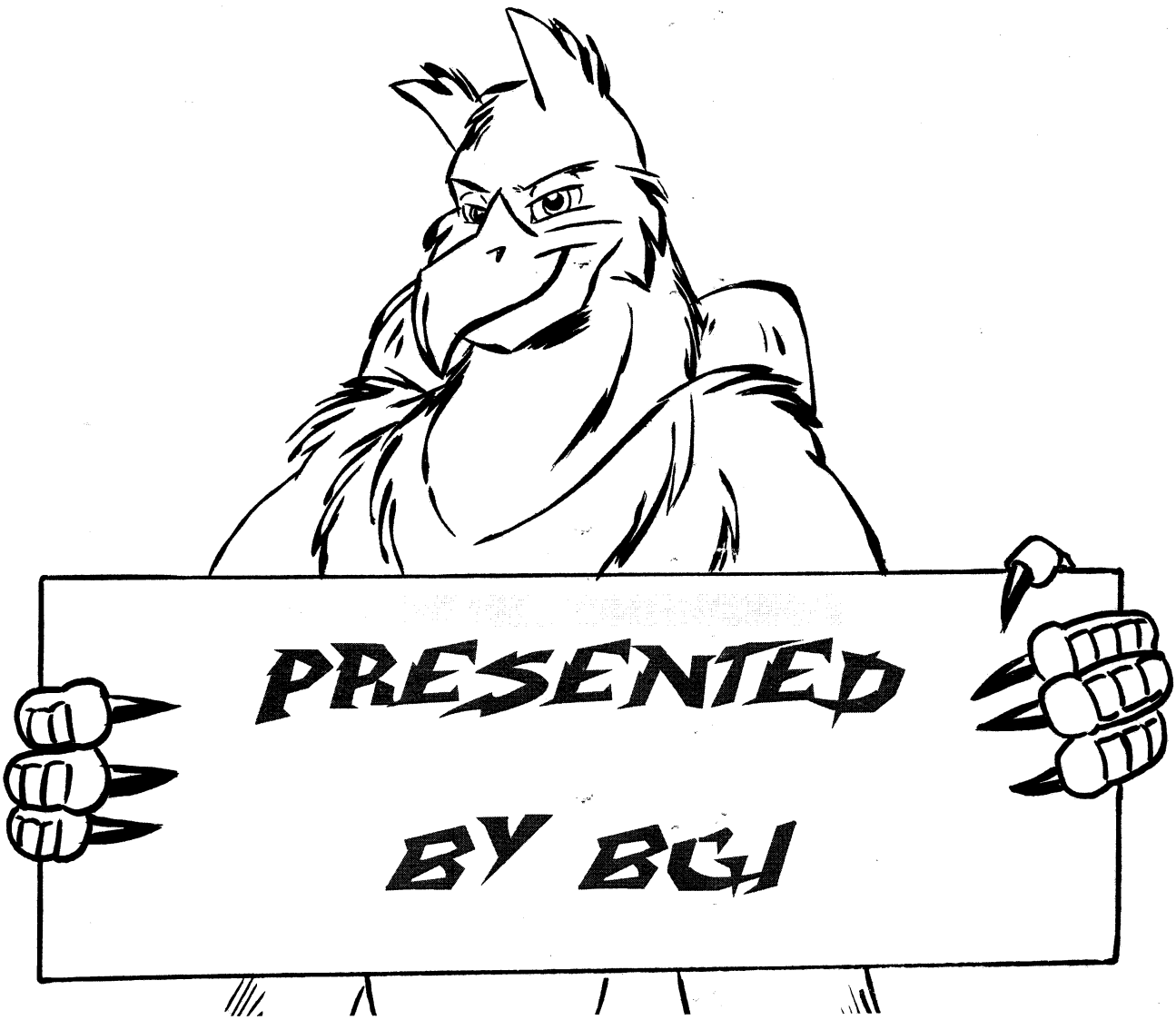
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PUBLICATION NO. 980535

OPERATORS MANUAL

9000A

MICROPROCESSING TIMER/COUNTERS

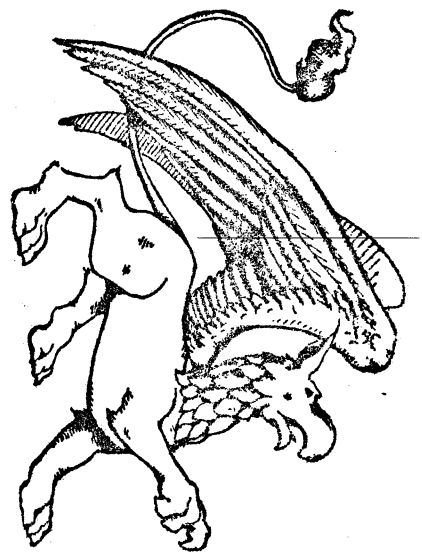

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TABLE OF CONTENTS

Section	Title	Page
1	**GENERAL DESCRIPTION**	**1-1**
1.1	General	1-1
1.2	General Description	1-1
1.3	Mechanical Description	1-3
1.4	Electrical Description	1-4
1.5	Miscellaneous	1-4
1.5.1	Items Furnished	1-4
1.5.2	Required Tools & Test Equipment	1-4
1.6	Specifications	1-4
2	**INSTALLATION & OPERATION**	**2-1**
2.1	General	2-1
2.2	Unpacking and Inspection	2-1
2.3	Bench Operation	2-1
2.4	Rack Mounting	2-1
2.5	Power Connections	2-1
2.6	Grounding Requirements	2-2
2.7	Storage Requirements	2-2
2.8	Reshipment Packaging Requirements	2-2
2.9	Controls, Indicators & Connectors	2-2
2.9.2	Keyboard	2-2
2.10	Operation	2-11
2.10.2	General Usage Instructions	2-11
2.10.3	Arithmetic Computation	2-12
2.10.4	Trigger Level	2-12
2.10.5	Pulse Parameter (-11A Models)	2-12
2.11	Option 56, High Speed Interface	2-12
2.12	High-Speed Interface Installation	2-12
2.13	External Gate Control	2-35
2.13.2	Normal Mode	2-35
2.13.3	Selective Gate Control Mode	2-35
2.13.4	Synchronous Window Control	2-36
2.13.5	Programmable Arming Modes (Option 06PA)	2-36
3	**SYSTEMS INTERFACE**	**3-1**
3.1	General	3-1
3.2	Option 55 General Purpose Interface Bus	3-1
3.2.3	Bus Description	3-2
3.2.4	Handshake	3-3

TABLE OF CONTENTS continued

Section	Title	Page
3.2.5	Address Assignment	3-3
3.2.6	Bus Operation Sequence	3-7
3.2.7	Interface Message Repertoire	3-10
3.2.8	Status Byte	3-12
3.2.9	Device Dependent Messages	3-13
3.2.10	Trigger Level & Measurement Data Output Messages	3-19
3.2.11	Programmable External Gate Control (Option 06PA)	3-20
3.3	Software Organization	3-25
3.3.3	Counter Transactions	3-25
3.4	High Speed Interface, Option 56	3-26
3.4.1	Programming Considerations	3-26
3.4.2	Programming Commands	3-26
3.4.3	Interface Electrical Connection	3-26
3.4.4	Control Signal Description	3-26
4	**APPLICATIONS**	**4-1**
4.1	Introduction	4-1
5	**THEORY OF OPERATION**	
6	**CALIBRATION**	
7	**DRAWINGS**	
8	**PARTS LIST**	

These sections are included in the Model 9000A Maintenance Manual. Publication No. 980537

LIST OF ILLUSTRATIONS

Figure	Title	Page
1.1	9000A Microprocessor Timer/Counter	viii
1.2	Plug-In Board Locations	1-2
1.3	Series 9000A Block Diagram	1-3
2.1	Rack Mount Installation	2-1
2.2	Front Panel	2-2
2.3	Rear Panel	2-4
2.4	Keyboard	2-2
2.5	High Speed Computer Interface	2-13
2.6	Gate Delay Input Connector and Mode Switch	2-35
2.7	Normal Mode Measurement Gate Timing	2-35
2.8	Selective Gate Control Mode Timing	2-36
2.9	Synchronous Window Control Mode, Single Pulse Window	2-36
2.10	Synchronous Window Control, Multiple Pulse Window	2-36
3.1	Series 9000A GPIB System Relationship	3-1
3.2	Handshake Sequence	3-3
3.3	Handshake Flow Chart	3-6
3.4	Handshake Timing	3-7
3.5	Status Byte Format	3-12
3.6	Rise Time Measurement	3-14
3.7	Option 06PA Simplified Block Diagram	3-20
3.8	Selective Gate Example 1	3-21
3.9	Selective Gate Example 2	3-22
3.10	Selective Gate Example 3	3-22
3.11	Synchronous Window Example 1	3-23
3.12	Synchronous Window Example 2	3-23
3.13	Gate Delay Measurement Connections	3-24
3.14	Gate Delay Timing Example	3-24
3.15	Software Organization	3-24
3.16	9000A Counter Transaction For Frequency Measurement, Channel A	3-25
3.17	Function Word Format	3-27
3.18	Trigger Word Format	3-27
3.19	Definition Word Format	3-28
3.20	Constant M Word Format	3-28
3.21	Constant E Word Format	3-29
3.22	Option 56 Pin Description (16-Bit MUX Mode)	3-30
3.23	Command Word Sequence Example	3-30
3.24	Read Mode Handshake Timing	3-33
3.25	Write Mode Handshake Timing	3-34
3.26	Output Word Sequence Example	3-35

LIST OF TABLES

Table	Title	Page
1.1	Measurement Capability	1-1
1.2	Specifications	1-4
2.1	Controls, Indicators & Connectors	2-3
2.2	Gate Time/Multiplier	2-11
2.3	Time Interval Measurement	2-14
2.4	Time Interval Average Measurement	2-16
2.5	Period Measurement	2-18
2.6	Period Average Measurement	2-19
2.7	Frequency Measurement, 0 – 100 MHz (F_A)	2-20
2.8	Frequency Measurement, 100 – 512 MHz (FC), Model 9035 Only	2-21
2.9	A/B Ratio	2-22
2.10	Totalize	2-23
2.11	Arithmetic Computation, Addition (Models 9015A, 9035A Only)	2-25
2.12	Arithmetic Computation, Multiplication (Models 9015A, 9035A Only)	2-27
2.13	Arithmetic Computation, Division (Models 9015A, 9035A Only)	2-28
2.14	Arithmetic Computation, Reciprocal	2-29
2.15	Trigger Level	2-30
2.16	Pulse Width (-11A Models Only)	2-32
2.17	Rise Time (-11A Models Only)	2-33
2.18	Fall Time (-11A Models Only)	2-34
2.19	Mode Switch Operation	2-35
3.1	Connector Contact Assignments	3-1
3.2	IEEE-STD-488-1978 Standard Interface Subset Capability	3-1
3.3	Distribution and Assignment of Interface Signal Lines	3-2
3.4	Series 9000A GPIB Address Assignment	3-4
3.5	Bus Operation Sequence	3-8
3.6	Interface Messages Used With Series 9000A Counter-Timer	3-11
3.7	Home State Condition	3-11
3.8	9000A Device Dependent Messages	3-16
3.9	Program Commands	3-20
3.10	Option 56 Pin Description (Parallel Mode)	3-29
3.11	Control Signal Functions	3-31
3.12	Status Signal Functions	3-32

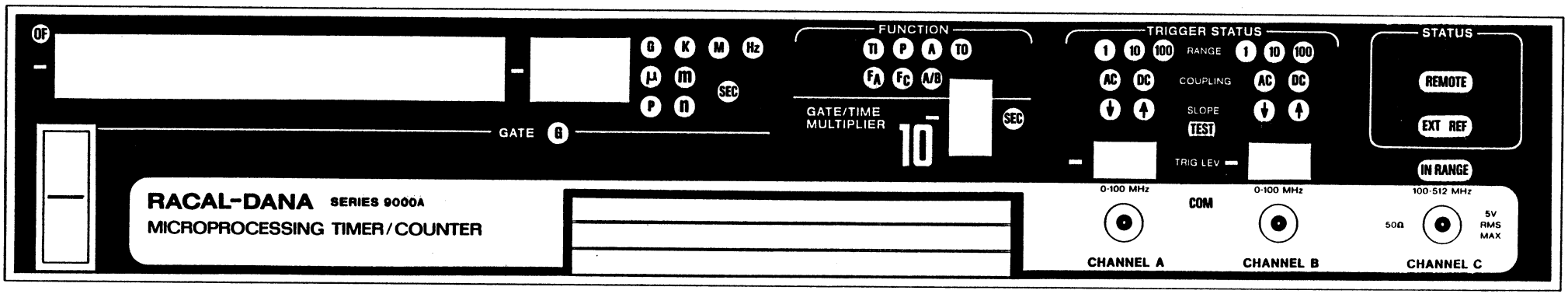


Figure 1.1 - 9000A Microprocessor Timer/Counter

SECTION 1 GENERAL DESCRIPTION

.1 GENERAL.

1.1.1 This manual provides installation, operation and calibration procedures for Models 9015A, 9015/11A, 9035A, and 9035/11A of the Racal-Dana Series 9000A Microprocessor Timer/Counter (Figure 1.1).

1.1.2 The 9000A Series comprises four models: the 9015A, 9035A, 9015/11A and 9035/11A. The 9035A model performs all of the functions of the 9015A model and in addition it measures frequencies from 100 MHz to 512 MHz. The /11A models include the pulse parameters measurement in place of the arithmetic functions of the other models.

1.2 GENERAL DESCRIPTION.

1.2.1 The 9015A and 9035A feature universal counter measurement modes, computation capabilities, keyboard entry, 9-digit display, a full complement of annunciators, and manual and automatic trigger level setting.

1.2.1.1 Standard measurement modes include Time Interval, Time Interval Average, Period, Period Average, Frequency Ratio, Totalizing, Scaling, Frequency A measurements from 0 to 100 MHz and, on the Model 9035A and 9035/11A, Frequency C measurements of from 100 MHz to 512 MHz.

1.2.1.2 The calculating capabilities include addition of a constant to a measurement, the subtraction of a constant from a measurement, multiplication of a measurement by a constant, division of a measurement by a constant, and the reciprocal of a measurement. The constant used in the computation can be any number of either polarity from 1 to 9 digits long with exponent notation from 1 to 99 of either polarity.

1.2.1.3 The keyboard consists of 32 pushbuttons and six slide switches on a drawer that slides into the front of the instrument when not in use. All local control functions except power is through the keyboard including function, timebase, slope, coupling, sep/com, test, auto and manual trigger level, norm/hold, arithmetic entry, reset, initialize, start/stop and remote.

1.2.1.4 The front panel contains the standard input BNC connectors, the power switch, and all of the visual indicators including the display, gate time/multiplier, annunciators and trigger levels. The display provides 9 digit resolution of measurement with fixed decimal and leading and following zero blanking. The display is used for both measurement and arithmetic computation. The display consists of an overflow indicator, a "–" polarity sign, 9 numeric display LEDs, an exponent-polarity sign and 2 numeric exponent LEDs. The display scale consists of a nine LED annunciator indicating the time or frequency or events of the measurement. The function annunciator consists of seven LEDs which indicate the function selected. The gate time/multiplier is a single numeric LED with a "–" polarity indicator and a seconds indicator. The numeric LED signifies the power to which 10 is raised and represents the setting of the timebase/multiplier. The status of the channel A and channel B triggers are shown including the range, coupling, slope, trigger level (3 digits), trigger level polarity and channel A/B common coupling. Other annunciators on the front panel include remote, external reference, in-range (functional on 9035A only), and gate.

1.2.2 Options available for the Series 9000A offer increased flexibility for the user in the areas of pulse measurement, accuracy, and systems use, two oscillator options, two interface options, rack mounting and rear input options. These are described briefly below.

1.2.2.1 *-11A Models Pulse Parameter.* These models provide automatic measurement of rise time from 10% to 90% points, fall time from 90% to 10% points and positive pulse width at 50% of peak points. All pulse measurements are made in the Time Interval or Time Interval Average modes. These options replace the arithmetic computation feature of the instrument. The -11A models provide pulse parameter measurements for signals with a frequency of 400 cycles or more; option 12 provides an extended lower frequency for signals with a frequency as low as 75 cycles.

1.2.2.2 *Option 01 Rear Input.* This option consists of three input connectors provided at the rear panel and the internal movement of the signal conditioning boards to new

Table 1.1 - Measurement Capability

Model	Time Interval	Time Interval Averaging	Period	Period Average	Freq A (to 100 MHz)	Freq C (to 512 MHz)	A/B Ratio	Totalize	Automatic Pulse Parameters	1/X	Arithmetic Functions
9015A	X	X	X	X	X		X	X		X	X
9035A	X	X	X	X	X	X	X	X		X	X
9015/11A	X	X	X	X	X		X	X	X	X	
9035/11A	X	X	X	X	X	X	X	X	X	X	

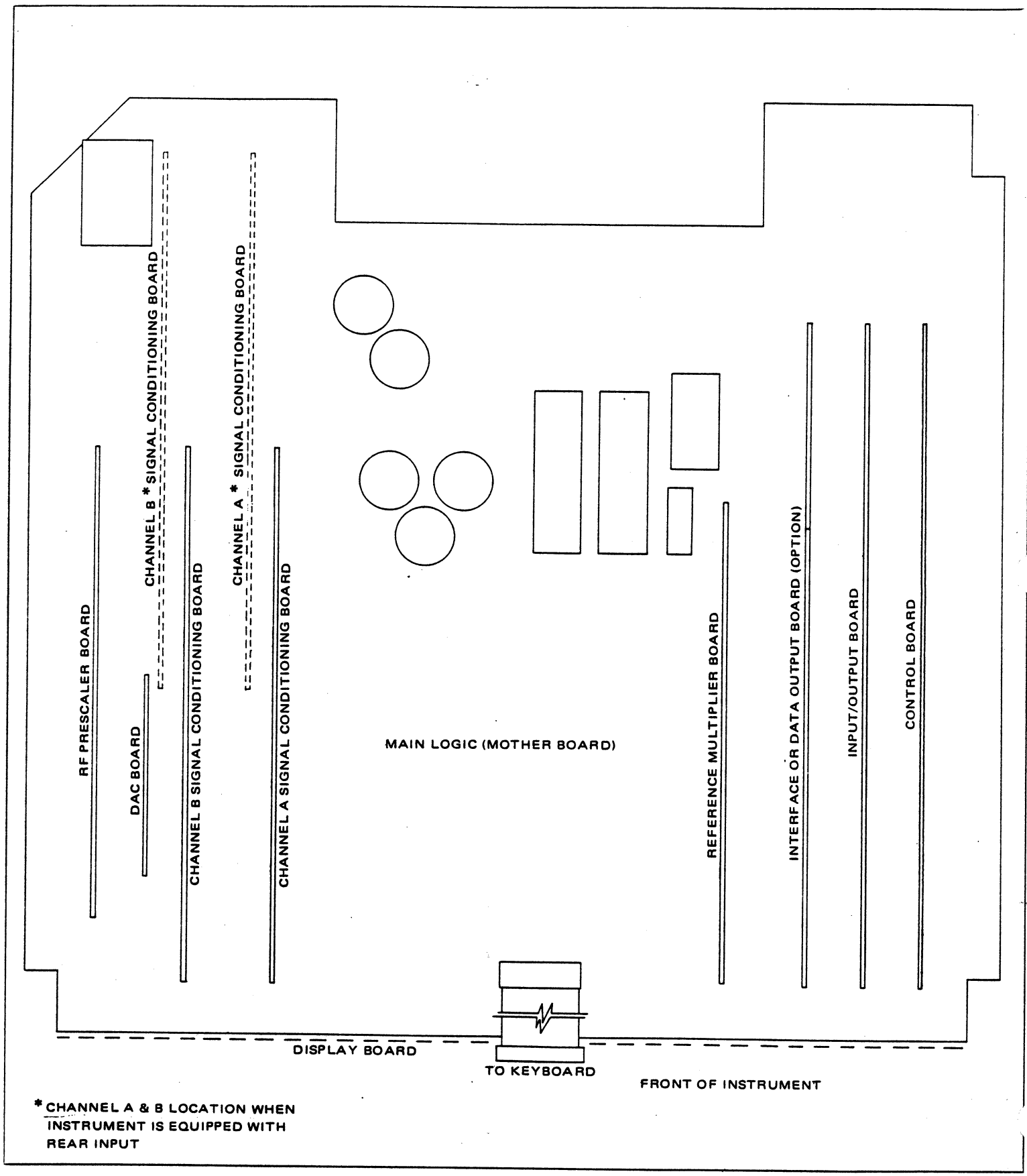


Figure 1.2 - Plug-In Board Locations

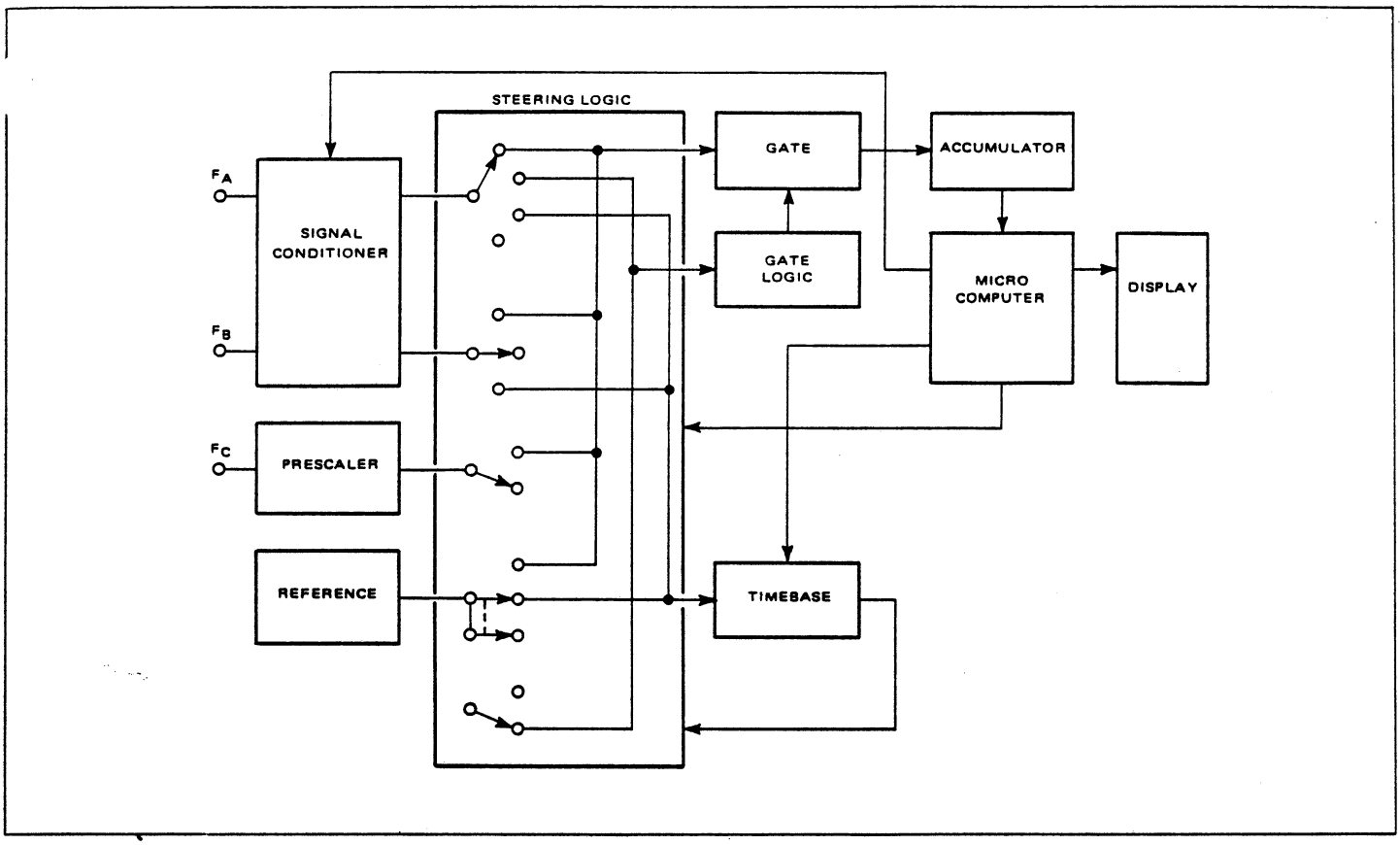


Figure 1.3 - Series 9000A Block Diagram

rear input connector locations. The option is primarily for systems use; the front panel connectors being open. The instrument is converted back to a bench top instrument by placing the signal conditioning boards back to the front panel input locations.

1.2.2.3 *Option 22A Oven Oscillator.* This option replaces the standard internal reference and provides an aging rate of $< 3 \times 10^{-9}$ per day.

1.2.2.4 *Option 24A Oven Oscillator.* Same as option 22A with an aging rate of $< 5 \times 10^{-10}$ per day.

1.2.2.5 *Option 55 Parallel ASCII GPIB Interface.* This option is directly compatible with the IEEE-STD-488-1978 General Purpose Interface Bus and permits direct communication between the 9000A and a controller for both programming and data output.

1.2.2.6 *Option 56 High Speed Computer Interface.* This option is used generally in systems utilizing a computer and permits selection of two speeds; computer speed in which raw data is transmitted by the 9000A and microprocessor speed which allows the data to be manipulated by the microprocessor. Two bus formats allow the user to customize the 9000A interface to fit a particular system.

1.2.2.7 *Option 60 Rack Mounting Flanges.* This option allows the 9000A to be mounted in a standard 19-inch rack.

1.3 MECHANICAL DESCRIPTION.

1.3.1 The Series 9000A is completely enclosed in a standard rack width, aluminum case and is designed for either rack or bench top operation.

1.3.2 The standard instrument (figure 1.2) consists of the mainframe (mother board) with five plug-in boards and the display board. The mainframe is mounted next to the top cover of the instrument with the component side of the board facing down. On the board is mounted most of the logic components, the reference oscillator and the power supply. The plug-in boards plug into the mainframe and are between the mainframe and the bottom cover. The plug-in

boards are the DAC board, channel A Signal Conditioning board, the channel B Signal Conditioning board, the Reference Multiplier, and the Computer III board. (Instruments designed to meet the special requirements of a customer may have three boards in place of the Computer III board.)

1.4 ELECTRICAL DESCRIPTION.

1.4.1 The Series 9000A shown in simplified form in figure 1.3, consists of the following functional blocks: Signal Conditioning circuitry that scales, generates a squared wave output from the input signal, and selects the points on the incoming signal that determine the characteristics of the squared wave output; a stable and accurate 100 MHz reference frequency; an adjustable timebase that allows the signal applied to it to be divided by 1, 10, or some multiple of 10; gate logic that converts a signal input into a corresponding time period; a gate (controlled by the gate logic) that regulates the flow of pulses to the accumulator; an accumulator that counts a signal applied to it and stores the binary value of the count; a microcomputer that controls the operation of the counter, performs any programmed arithmetic operations, and routes the data in the accumulator to the display; the display that provides in visual form the numeric value of the binary data stored in the accumulator as well as the status of the timebase, signal conditioners and other instrument operations.

1.4.2 The instrument performs the various measurement functions by routing the input signal and internal signals, according to the function and timebase division selected, between the various functional blocks. Mathematical operations are performed by routing the data from the accumulator to the microcomputer. All computations then take place within the microcomputer and the results routed to the display.

1.5 MISCELLANEOUS.

1.5.1 Items Furnished.

1.5.1.1 Items provided with the Series 9000A includes:

a. Power Cable.

b. Operators Manual.

1.5.2 Required Tools & Test Equipment.

1.5.2.1 Tools required for maintenance are listed in paragraph 5.9.1.1.

1.5.2.2 Equipment required for calibration is shown in table 5.1.

1.6 SPECIFICATIONS.

1.6.1 The specifications are shown in table 1.2.

Table 1.2 - Specifications

GENERAL	
Calculating Capability:	$\frac{(X+K_1)\,K3}{K_2}$ $\frac{(1/X+K_1)K_3}{K_2}$ where: K_1, K_2 and K_3 are user entered constants and X is the measurement.
Memory Capability:	The constant operates on successive measurements until either the measurement mode is changed or the constant/ operation is changed, or the unit is reinitialized.
Constant Range:	±999.999999 EXP +99 to ± 1E-99
Automatic Ranging:	Channels A and B voltage ranges are automatically selected as a function of the input signals' voltage levels.
Manual Ranging:	Channels A and B voltage ranges are selected as a function of the trigger level resolution.
Automatic Trigger Level:	The counter measures the maximum and minimum peak of the input signal, calculates the arithmetic mean, and automatically sets the trigger level at the mean. Standard on both channels A and B. For inputs ≥ 400 Hz, ≥ 50 mV rms, or minimum sensitivity; whichever is greater
Analog Trigger Level Output:	Scaled analog voltage (+3V to −3V) outputs representing channels A and B trigger points.
Internal Reference Oscillator:	
Aging Rate:	$<3\times10^{-7}$ per month
Temperature Stability:	$<5\times10^{-6}$, 0°C to +50°C
Voltage Stability:	$<1\times10^{-7}$ with 10% line voltage variation
Internal Reference Output:	10 MHz square wave, buffered, TTL compatible

Table 1.2 - Specifications continued

GENERAL continued	
External Reference Input:	1, 5, or 10 MHz; 1V RMS into 1 Kohm. Counter automatically locks to external reference; if present, front panel indicator lights.
Marker Output:	Negative-going pulse (+3V to −12V) available on a rear panel BNC, with duration equal to channel A trigger point toger channel B trigger point.
Display:	
Numeric:	Eleven, 11 mm (.43 inch) yellow LEDs. Leading and following zeros suppressed.
Status Indicators:	LED lamps show status of counter controls: Function, Measurement Time, System Control, External Reference, Input voltage range, Slope, Coupling, Separate/Common, and Test. LED lamps show numeric readout dimensional units, overflow, condition, and channel C input status.
Trigger Level:	Two, 3-digit 2.8 mm (.11 inch) red LEDs.
Sample Rate:	Periodic or hold, switch selectable. In periodic mode, rest time between readings is approximately 300 msec.
Input/Output Connectors:	BNC
Operating Temperature:	0°C to +50°C
Storage Temperatures:	−40°C to +70°C at 75% RH
Operating Humidity:	< 75% RH from +25°C to +40°C <50% RH from +40°C to +50°C
Dimensions: (HxWxD)	3-15/32 x 16-3/4 x 18 inches
Weight:	Net 19 lbs. (8.6 Kg) Shipping 25 lbs. (11.4 Kg)
Line Voltage:	50 to 60 Hz; 100, 120, 220, or 240V +5%, - 10%.
Power Requirement:	120 watts max., 85 watts nom.

INPUT CHARACTERISTICS	
Channel A and B Frequency Range:	
DC Coupled:	0 to 100 MHz
AC Coupled:	20 Hz to 100 MHz
Coupling:	DC or AC, switch selectable
Sensitivity	
Sinewave:	25 mV RMS to 1 MHz 50 mV RMS to 50 MHz 100 mV RMS to 100 MHz
Pulse:	150 mV P-P; 8 nsec minimum width
Input Impedance (Std):	1 Mohm shunted by less than 65 pF.
(Opt):	50 ohms programmable with 06PA.
Maximum Input: (without damage)	X1: 0–20 kHz; 250V RMS 20 kHz – 1 MHz; $5x10^6/f$ 1 MHz – 100 MHz; 5V RMS X10, X100: 0–5.5 MHz; 250V RMS 5.5 MHz – 100 MHz; $1.38x10^9/f$ 5V RMS max with 50Ω input impedance selected.
Voltage Ranges:	1, 10, 100; Keyboard selectable or automatically selected.
Trigger Level:	Digitally adjustable (keyboard entry) from +318.75 to - 320% of voltage range; calibrated to resolution of ± 1.25% of voltage range. Digital levels displayed on front panel and analog levels (DAC outputs) available on rear panel.
Input Trigger Level Accuracy:	±5% of range ±0.1% range per °C
Output Trigger Level Accuracy:	±2% of range of actual trigger point
Channel C (9015A & 9035/11A) Frequency Range:	100 MHz to 512 MHz
Sensitivity Sinewave:	15 mV rms
Input Impedance:	50 Ohms nominal
Maximum Operating Input:	1V rms
Maximum Input: (without damage)	5V rms (fuse protected)
Automatic Gain Control:	40 dB without adjustment
Prescale Factor:	10

Table 1.2 - Specifications continued

TIME INTERVAL MEASUREMENT	
Range:	10 nsec to 10^9 seconds
Resolution:	10 nseconds
Accuracy:	±1 count ± reference error ± trigger error*
Input:	
Separate Mode:	Channel A start and Channel B stop
Common Mode:	Channel A start and stop
Home State:	
Resolution:	10 nsec
Reciprocal Mode (1/X):	Displays $\frac{1}{\text{Time Interval}}$
Display:	nsec, μsec, msec, sec, ksec, or Msec
*trigger error: $\leq \frac{0.0025}{\text{Signal Slope (in V/sec)}}$	

TIME INTERVAL AVERAGE	
Range:	100 psec to 10 psec
Accuracy:	±reference error ± 2 nsec ± $\frac{\text{(trigger error* + 10 nsec)}}{\sqrt{\text{Number of Intervals Averaged}}}$
Intervals Averaged:	1 to 10^9, selectable in decade steps
Dead Time:	Minimum time between stop and start: 50 nsec
Input:	
Separate Mode:	Channel A start and Channel B stop
Common Mode:	Channel A start and stop
Home State:	
No. Intervals Averaged:	'10'
Resolution:	1 nsec
Reciprocal Mode (1/X):	Displays $\frac{1}{\text{Time Interval Average}}$
Display:	psec, nsec, μsec, msec, or sec
*trigger error: $\leq \frac{0.0025}{\text{Signal slope (in V/sec)}}$	

PERIOD MEASUREMENT	
Range:	10 nsec to 10^9
Resolution:	10 nsec
Accuracy:	±1 count ± reference error ± trigger error*
Input:	Channel A
Home State:	
Resolution:	10 nsec
Reciprocal Mode (1/X):	Displays Frequency, 1 Hz to 100 MHz
Display:	nsec, μsec, msec, sec, ksec, or Msec

*trigger error: $\leq \frac{0.3}{(S/N)\, f_A}$ (for sine waves)

where S/N equals signal to noise ratio in volts and f_A equals input frequency

PERIOD AVERAGE	
Range:	10 nsec to 1 sec
Accuracy:	±reference error ± 1 count ± $\frac{\text{trigger error*}}{\text{Number of Periods Averaged}}$
Intervals Averaged:	1 to 10^8, selectable in decade steps
Input:	Channel A
Home State:	
No. Intervals Averaged:	'10'
Resolution:	1 nsec
Reciprocal Mode (1/X):	Displays frequency, 1 Hz to 100 MHz
Display:	nsec, μsec, msec, or sec

*trigger error: $\leq \frac{\leq 0.3}{S/N\, f_A}$ (for sine waves)

where S/N equals signal to noise ratio in volts and f_A equals input frequency

Table 1.2 - Specifications continued

FREQUENCY MEASUREMENT TO 100 MHz	
Frequency Range:	
DC Coupled:	0 to 100 MHz
AC Coupled:	20 Hz to 100 MHz
Accuracy:	
Standard Mode:	±1 count ± reference error
Computing Mode:	$\frac{1}{\text{Accuracy of Period Meas'mt}}$
Input:	Channel A
Measurement:	
Standard Mode:	1 μsec to 10 sec, selectable in decade steps
Home State:	
Measurement Time:	.1 sec
Frequency Resolution:	10 Hz
Reciprocal Mode (1/X):	Displays Period, 10 nsec to 10^6 sec
Display:	9 digits; mHz, Hz, kHz, or MHz
Self Test: (10^{-1} sec timebase):	10.00000 MHz

FREQUENCY MEASUREMENT TO 512 MHz (Models 9035A & 9035/11A Only)	
Frequency Range:	100 MHz to 512 MHz
Accuracy:	±1 count ± reference error
Input:	Channel C
Measurement Time:	1 μsec to 10 sec, selectable in decade steps
Home State:	
Measurement Time:	.1 sec
Frequency Resolution:	100 Hz
Reciprocal Mode (1/X):	Displays Period, 2 nsec to .1 μsec
Display:	9 digits, MHz

FREQUENCY RATIO MEASUREMENTS	
Frequency Range:	
Channel A:	0 to 100 MHz
Channel B:	0 to 100 MHz
Ratio:	10^{-8} to 10^8
Multiplier:	f_B scaled by 1 to 10^9, selectable in decade steps
Accuracy:	±1 count of f_A ± trigger error* of f_B
Home State:	
Multiplier:	10
Reciprocal Mode (1/X):	Displays multiplier $f_B \div f_A$,
Display:	$f_A \div$ multiplier f_B, dimensionless

*trigger error $\frac{\leq 0.0025}{\text{Signal slope (in V/sec)}}$

TOTALIZE MEASUREMENT	
Frequency Range:	0 to 100 MHz
Count Range:	0 to 10^9
Accuracy:	±1 count per gate

SCALING	
Frequency Range:	0 to 100 MHz
Scaling Range:	
≤10 MHz:	1 to 10^9, selectable in decade steps
> 10 MHz:	10 to 10^9, selectable in decade steps
Input:	Channel A

Table 1.2 - Specifications continued

PULSE PARAMETER MEASUREMENTS (Models 9015/11A & 9035/11A)

Initiation of the required measurement by a single key entry activates the microprocessor to measure the pulse amplitude, calculate and set the required start/stop trigger level settings, and initiate the counter to take the time interval measurement. The start and stop trigger level values are displayed on the front panel and are available to the system output.

Rise Time:	
Start Point:	10% of pulse amplitude, positive slope
Stop Point:	90% of pulse amplitude, positive slope
Fall Time:	
Start Point:	90% of pulse amplitude, negative slope
Stop Point:	10% of pulse amplitude, negative slope
Pulse Width:	
Start Point:	50% of pulse amplitude, positive slope
Stop Point:	50% of pulse amplitude, positive slope
Resolution:	Same as function selected; TI or TIA
Minimum Frequency For Proper Operation:	400 Hz (75 Hz with Opt. 12)
Trigger Level Setting Accuracy:	±5% of voltage range
Input:	Channel A
Minimum Pulse Height:	0.5V
Display:	nsec, μsec, msec, sec, ksec, or Msec
Accuracy:	Same as function selected.

REAR INPUT (Option 01)

Option 01 provides channel A, B, and C input on the rear panel of the instrument. When this option is installed the front panel input connectors are disconnected. With this option installed, the counter may be converted back to front panel input by reversing Input PCB.

INTERNAL REFERENCE OSCILLATOR OPTIONS

Option 22A	
Aging Rate:	$<1x10^{-9}$ per day
Temperature Stability:	$<5x10^{-9}$, 0°C to +50°C
Voltage Stability:	$<2x10^{-9}$ with 10% line voltage variation
Option 24A	
Aging Rate:	$<5x10^{-10}$ per day
Temperature Stability:	$<5x10^{-9}$, 0°C to +50°C
Voltage Stability:	$<2x10^{-9}$ with 10% line voltage variation
Warmup (For 1 x 10^{-7} accuracy)	20 minutes

SYNCHRONOUS WINDOW & SELECTIVE GATE CONTROLS

The Selective Gate Control allows an externally applied pulse to control the arming of channels A and B. The rising edge of the positive going TTL pulse would enable channel A, the start channel in a TI or TI average measurement, to trigger at the next correct trigger point and disable channel B, the stop channel, so that it cannot trigger even if the correct trigger point is seen by the counter. The falling edge of the pulse would then enable channel B, the stop channel, to trigger at the next correct trigger point seen by the counter.

The Synchronous Window allows an externally applied pulse to control the arming of channels A and B in the following manner. The rising edge of the positive going TTL pulse would enable both channels A and B to trigger at the next set of correct trigger points. The falling edge disables both channels A and B. Thus a measurement window is established during which time the 9000A can make a measurement. The Synchronous Window Control can be used only with the time interval average measurement mode.

OPTION 06PA

This option allows programming of normal operation, synchronous window mode or selective gate mode through the GPIB option. It also provides 1 Megohm or 50 ohm input impedance on channels A or B.

System Interface Specifications

GENERAL PURPOSE INTERFACE BUS

(Option 55)

The GPIB is compliant with IEEE-STD-488-1978, "IEEE Standard Digital Interface for Programmable Instrumentation." It provides interface capability with other instruments and controls manufactured by other companies also utilizing the "interface bus" structure.

IEEE-STD-488 SUBSET CAPABILITY

GPIB Subset	Description	Applicable Capability
AH1	Acceptor Handshake	Complete Capability
DC1	Device Clear	(1) DCL — Device Clear (2) SDC — Selected Device Clear
DT1	Device Trigger	GET — Group Execute-Trigger
L4	Listener	(1) Basic Listener (2) Unaddress if MTA
PP0	Parallel Poll	No Capability
RL1	Remote/Local	(1) REN—Remote Enable (2) LLO—Local Lockout (3) GTL—Go to Local (4) MLA—My Listen Address
SH1	Source Handshake	Complete Capability
SR1	Service Request	Complete Capability
T5	Talker	(1) Basic Talker (2) Serial Poll (3) Talk only Mode (4) Unaddress if MLA

Programming Inputs:	All front panel controls including digital trigger levels except line power on/off switch. Program settings displayed on front panel.
Data Output Format:	±.XXXXXXXXXE±YY Mantissa resolution same as front panel display resolution.
Electrical Compatibility:	Per IEEE Std 488-1978.
Programming Format:	7 bit ASCII Code.
Data Rate	①: 4.5msec + 160μsec per byte with no front panel display. ②: 6.0msec + 160μsec per byte with front panel display. ③: 17.0msec + 160μsec per byte with (1/X) inverted reading and no front panel display. Note: Measurements taken in Frequency A with a 1μsec gate time.

HIGH SPEED COMPUTER INTERFACE

(Option 56)

The basic interface structure for this option can be "built up" into one of four bus formats via internal switch selection and cable construction. For three of the formats, two operating speeds are available: (1) HI speed, which can be used for raw data transmission; and, (2) μ-processor speed, which allows data manipulation by the internal microprocessor.

Bus Descriptions:

a. 16-bit duplex I/O
Output: 16 lines (data)
Input: 16 lines (counter control)
5 Control lines, Remote line
HI speed or μ-processor speed

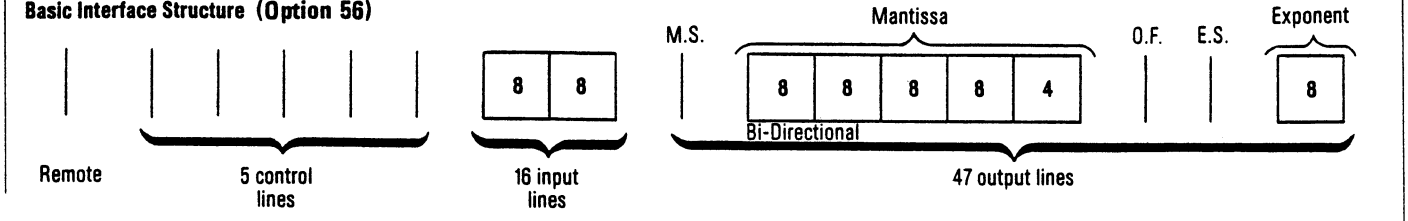
b. 40-bit printer
Output: 40 of 47 lines (data)
2 control lines, Remote line
HI speed or μ-processor speed

c. 40-bit with 16-bit bi-directional
Output: 40 of 47 lines (data)
Input: 16 lines (counter control)
5 control lines, Remote line
HI speed or μ-processor speed

d. 16-bit bi-directional
Output: 16 lines (data)
Input: 16 lines (counter control)
5 control lines, Remote line

Electrical Compatability:	Positive true, standard TTL logic levels
Data Rate:	≦28,000 words per sec

Basic Interface Structure (Option 56)



Remote - Places counter in remote control and disables front panel control

M.S. - Mantissa Sign Bit
O.F. - Overflow Sign Bit

E.S. - Exponent Sign Bit

SECTION 2 INSTALLATION & OPERATION

GENERAL.

2.1.1 This section covers the unpacking, inspection, installation, storage, repacking, and operation of the Series 9000A Counter.

2.1.2 The Operation section consists of brief descriptions of the front and rear panels, and the keyboard. This is followed by a series of tables that provide setup information and typical measurement examples.

2.2 UNPACKING AND INSPECTION.

2.2.1 The Series 9000A counter is packed in a plastic-foam form within a cardboard carton for shipment. The plastic form holds the counter securely in the carton and absorbs any reasonable external shock normally encountered in transit.

2.2.2 Prior to unpacking, examine the exterior of the shipping carton for any signs of damage. Carefully remove the counter from the carton and inspect the exterior of the instrument for any signs of damage. If damage is found, fy the carrier immediately.

2.3 BENCH OPERATION.

2.3.1 Each counter is equipped with a tilt bail or "kickstand" to enable the front of the instrument to be elevated for convenient bench use. The tilt bail is attached to the two front supporting "feet" at the bottom of the instrument. For use, the bail is pulled down to its supporting position.

2.3.2 The controls of the instrument are located on a keyboard which fits inside the instrument at the front panel when not in use. The keyboard pulls out when control entries are to be made and is hinged to allow the keyboard to slope down to the bench level for easy operation.

2.4 RACK MOUNTING.

2.4.1 The instrument can be mounted in a standard 19-inch rack with the option 60 rack-mounting flanges. To install the flanges, proceed as follows:

a. With instrument on its side, loosen the four captive Phillips head screws holding the bottom cover and remove cover. Remove screws holding feet (and bail) in place. Replace bottom cover.

b. Place one of the supplied screws through each of the two holes in the mounting flange (figure 2.1). Thread a securing nut onto each screw just enough to attach it to the screw (approximately one turn).

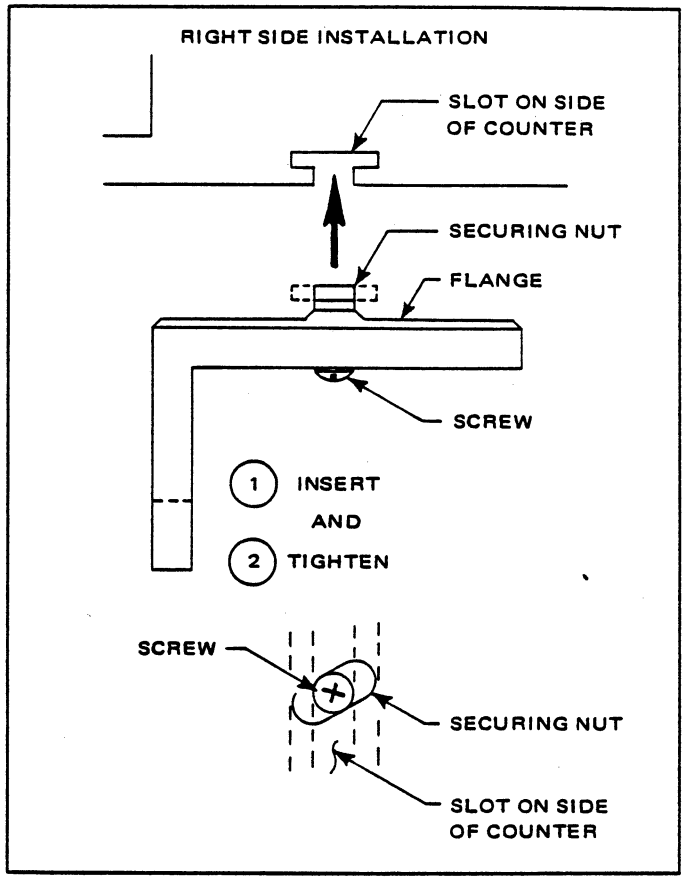


Figure 2.1 - Rack Mount Installation

c. Place the mounting flange onto the mounting slot in the instrument side panel so that the securing nuts fit entirely into the slot. Be sure the rack-mount slots on the flange are toward the front of the instrument.

d. Tighten screws. The securing nuts will rotate and hold the flange securely in place.

2.5 POWER CONNECTIONS.

2.5.1 Power is supplied to the counter through a standard 6-foot long detachable power cord. The ground pin (round) on the power plug is electrically connected to the case of the counter. It is important that this pin be connected to a good quality earth ground.

.2 The cord connects to the power connector module located on the rear panel which incorporates a fuse holder and power line voltage level selector. An additional line selector is internally located in instruments equipped with option 22 or 24 (see paragraph 2.5.5).

2.5.3 The fuse holder and power selector are accessible only when the power cable is removed. The power fuse is ejected by a lever marked FUSE PULL. The instrument uses a 1-1/4 amp fuse for 100 and 120 volt operation and a 3/4 amp fuse for 220 and 240 volt operation.

2.5.4 The instrument is made compatible with the available line voltage by the position of a small printed circuit board that fits into a slot in the module below the fuse. The board can be inserted into the slot in any one of four ways to provide for operation on the four available line voltage levels. The instrument is compatible with line frequencies from 48 to 63 Hz.

2.5.5 Instruments equipped with the option 22 or option 24 high stability reference oscillator have included an additional power supply. This supply provides power to the option as long as the power cord is connected, regardless of the position of the front panel power switch. The supply, located at J10 on the mainframe, has a line select switch which must be set to correspond to the line voltage. Access to the switch is gained by loosening the four captive corner screws and removing the bottom cover.

2.6 GROUNDING REQUIREMENTS.

2.6.1 To protect equipment operators from possible injury in the event of shorts or fault currents, the front panel and case of this instrument are grounded in accordance with MIL-T-28800A. A low impedance ground is maintained through one conductor of the three conductor power cable supplied with the instrument, when the cable is plugged into an appropriate, properly wired, receptacle.

2.7 STORAGE REQUIREMENTS.

2.7.1 The instrument can be stored at temperatures ranging from –40°C to +70°C at 75% relative humidity without damaging PCB's or components. The instrument must be brought to within the specified operating range (0°C to +50°C) before power is applied.

2.8 RESHIPMENT PACKAGING REQUIREMENTS.

2.8.1 The shipping carton with its molded plastic foam forms and plastic dust cover is specifically designed to provide the required support necessary for safe shipment. Whenever possible, these should be used for reshipment.

2.8.2 If the original packing materials are not available, proceed as follows:

a. Wrap instrument in plastic or heavy paper.

b. Place packing material around all sides of instrument and pack in cardboard box.

c. Place instrument and inner container in sturdy cardboard or wooden box. Mark box with appropriate precautionary labels.

2.9 CONTROLS, INDICATORS AND CONNECTORS.

2.9.1 The location, nomenclature and function of all controls, indicators and connectors are illustrated in Figures 2.2 thru 2.4 and described in Table 2.1.

2.9.2 Keyboard.

2.9.2.1 The keyboard consists of a drawer 5x7x.95 inches, with 32 pushbutton switches and six slide switches controlling all instrument operation except power on. The keyboard drawer is located at the lower center of the front panel and extends 7-1/2 inches from the front panel. A local reference for the keyboard operations is located in a slot on the keyboard module below the left edge of the keys.

2.9.2.2 With the drawer fully extended, a built-in hinge mechanism allows the drawer to swing down, providing easy access to the controls for both bench or rack use. When not in use, the drawer slides into the instrument, completely hiding all controls and eliminating the possibility of erroneous commands being entered.

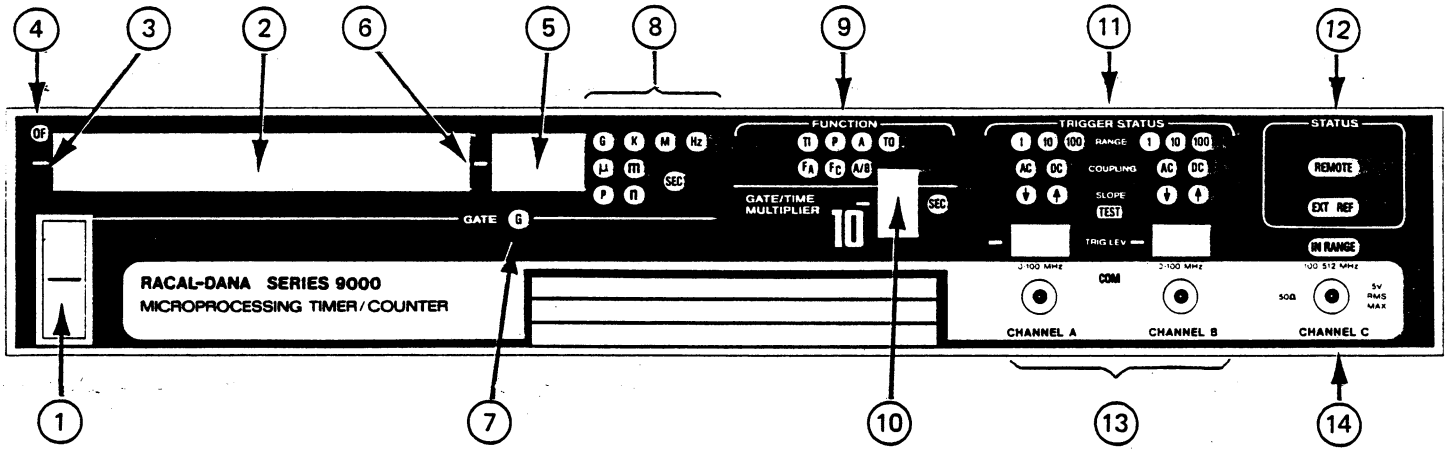


Figure 2.2 - Front Panel

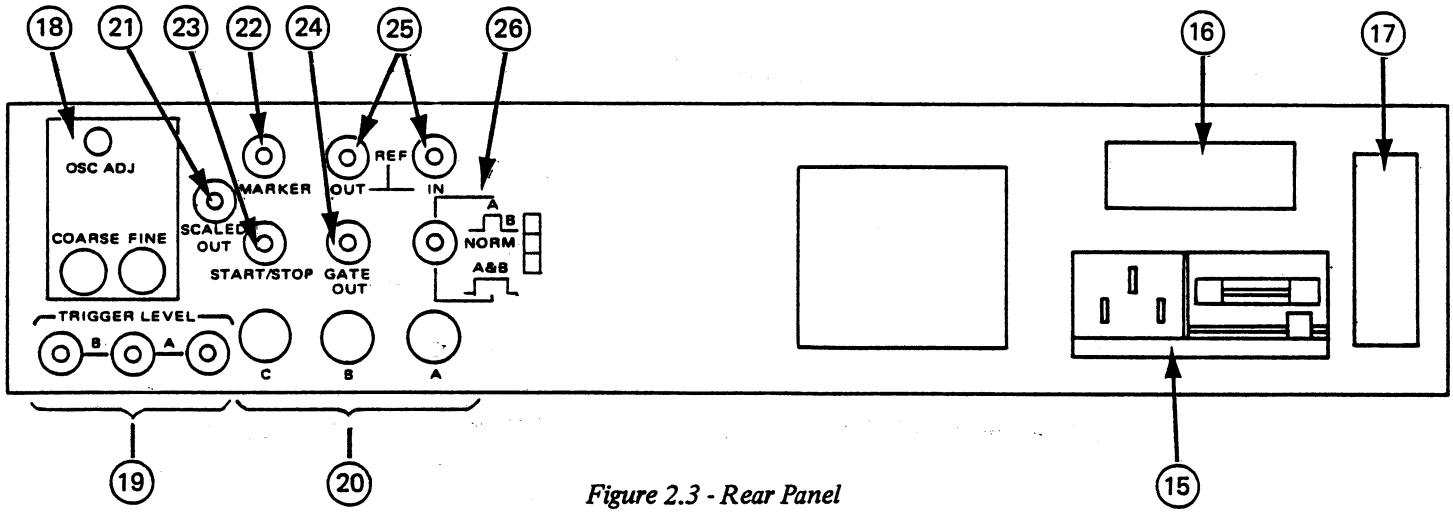
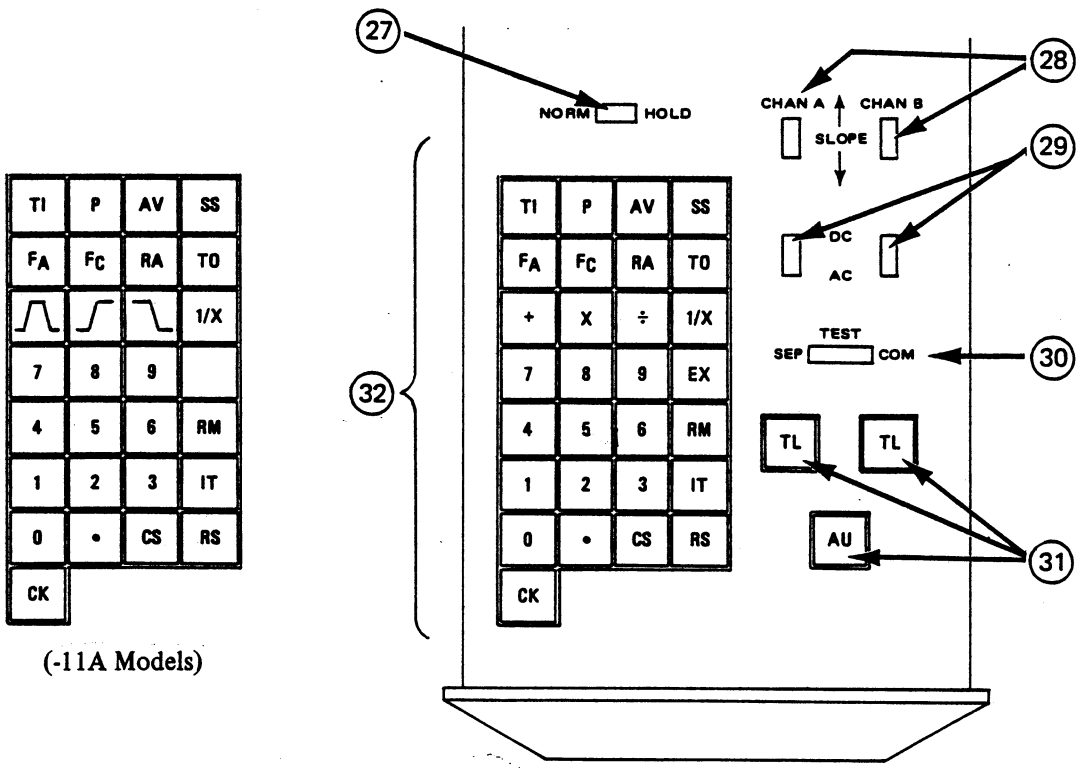


Figure 2.3 - Rear Panel



(-11A Models)

Figure 2.4 - Keyboard

Table 2.1 - Controls, Indicators and Connectors

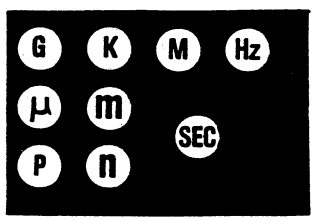
Reference	Item	Function
①	Power Switch/Indicator	Lights the switch and applies main AC power to the instrument when set to the ON position.
②	Mantissa Display LEDs	Nine 7-segment LEDs with a fixed decimal point. Used to display measurements, arithmetic entries and the results of arithmetic operations. Maximum display value is 999.999999.
③	Mantissa Sign Indicator	LED that illuminates when the mantissa display reading is a negative number.
④	Overflow Indicator	LED that illuminates when the mantissa display reading exceeds 999.999999.
⑤	Exponent Display LEDs	Two 7-segment LEDs. Used to indicate the exponent of arithmetic entries. Sometimes used in measurements as a non-exponential extension of the mantissa display.
⑥	Exponent Sign Indicator	LED that illuminates when the exponent of an arithmetic entry is negative.
⑦	Gate Indicator	LED that flashes to indicate the opening and closing of the gate. Internal circuitry stretches the gate pulse so that short gate times also produce a visible flash.
⑧	Measurement Unit Indicators	 LEDs that illuminate to indicate the measurement units indicated by the display LEDs. G : Giga K : Kilo M : Mega Hz : Hertz μ : Micro m : Milli P : Pico n : Nano SEC : Seconds

Table 2.1 - Controls, Indicators and Connectors continued

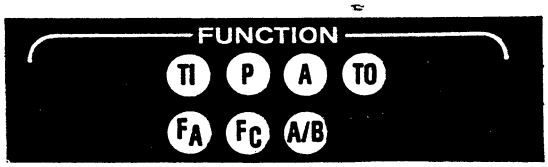
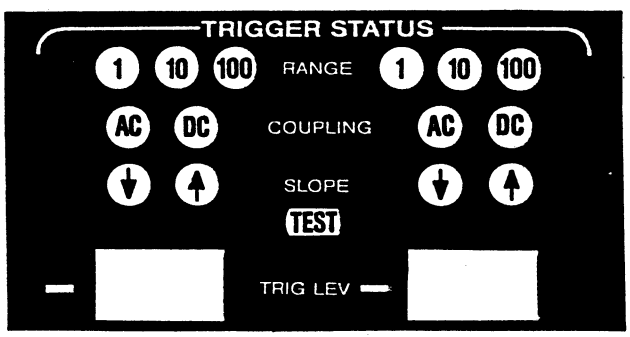
Reference	Item	Function
(9)	Function Indicators	 LEDs that illuminate to indicate the measurement function. TI : Time Interval P : Period A : Average (Used in conjunction with TI or P) TO : Totalize F_A : Frequency A (DC–100 MHz) F_C : Frequency C (100 MHz to 512 MHz – Model 9035A only.) A/B : Ratio (Channel A input divided by Channel B input)
(10)	Gate/Time Multiplier Indicators	 Single 7-segment LED with minus sign that indicates the exponent of the Gate/Time Multiplier. The SEC (seconds) LED illuminates during frequency, period and time interval measurements. Table 2.2 lists the available settings and effective resolutions for each function.
(11)	Trigger Status Indicators	 Identical sets of LED annunciators and three digit LED displays which indicate the trigger status of Channel A (left-hand set) and Channel B (right-hand set). The LED displays indicate the trigger levels; the minus signs are illuminated whenever the trigger level is at a negative voltage.

Table 2.1 - Controls, Indicators and Connectors continued

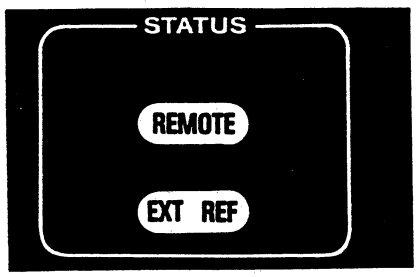
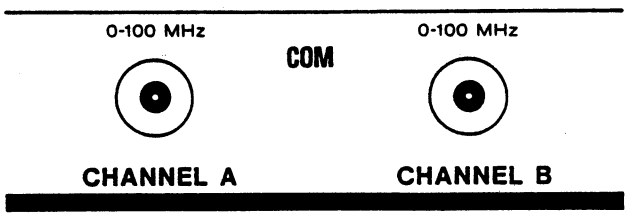
Reference	Item	Function
		1 : 1 volt range 10 : 10 volt range (divides input voltage by 10) 100 : 100 volt range (divides input voltage by 100) AC : AC coupled input DC : DC coupled input ↓ : Triggers on negative slope of input waveform ↑ : Triggers on positive slope of input waveform TEST : Illuminated when the instrument is placed in the test mode.
(12)	Status Indicators	 REMOTE : Illuminated when the instrument is in remote operation (eg: by a GPIB controller) EXT REF : Illuminated when an external reference (1, 5 or 10 MHz at 1V RMS) is applied to the rear panel REF IN connector.
(13)	Channel A and B Inputs	 BNC connectors. Channel A is used in all functions except Frequency C. Channel B is used, in conjunction with Channel A, for Ratio, Time Interval and Time Interval Average measurements. The COM indicator is illuminated whenever the common input mode is selected. The Common mode disconnects the Channel B input and couples the Channel A input signal to both the Channel A and Channel B signal conditioners.

Table 2.1 - Controls, Indicators and Connectors continued

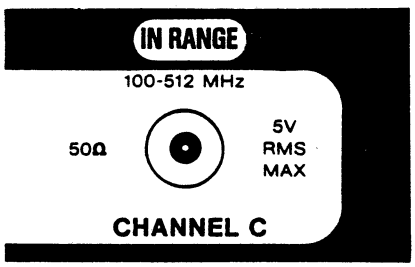
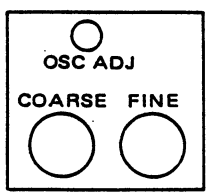
Reference	Item	Function
		NOTE If Rear Input Option 01 is installed, the front panel A, B and C channel input connectors are not connected. Input may be connected only through the rear panel connectors.
(14)	Channel C Input (Models 9035A, 9035/11A Only)	 BNC connector. Used to prescale high frequency inputs when Frequency C is selected. IN RANGE : Illuminated when an input signal of 100 MHz to 512 MHz, 15 mV to 1V RMS is connected.
(15)	Power Input Module	Connection for primary AC power line cord. Also contains the power fuse and line voltage select card.
(16)	GPIB Connector (Option 55) Computer Interface Connector (Option 56)	Provides for interface with IEEE-STD-488-1978 GPIB. One of two connectors used as an interface with computer systems.
(17)	GPIB Address Switch (Option 55) Computer Interface Connector (Option 56)	Used to set the GPIB talk and listen addresses. One of two connectors used as an interface with computer systems.
(18)	Reference Oscillator Adjust	 Provide access to oscillator frequency adjustment screws. The top opening is for standard reference oscillators, and the bottom two holes are for Option 22 or 24 reference oscillators. Adjustments are made with a non-inductive flat-blade tool.

Table 2.1 - Controls, Indicators and Connectors continued

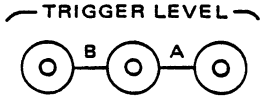
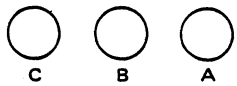
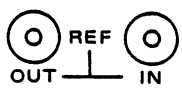
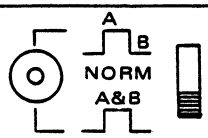
Reference	Item	Function
(19)	Trigger Level Outputs	 Three binding post outputs; center post is common. An analog equivalent of the trigger levels is made available for monitoring purposes.
(20)	Rear Panel Channel Inputs (Option 01)	 BNC channel input connectors. NOTE If Rear Input Option 01 is installed, the front panel A, B and C channel input connectors are not connected. Input may be connected only through the rear panel connectors.
(21)	Scaled Output Connector	BNC connector. Provides a TTL compatible output of the signal from the timebase divider circuit.
(22)	Marker Output Connector	BNC connector. The output swings to −12 volts when a pulse is received at the Channel A input. The output returns to +3 volts when a pulse is received at the Channel B input. This output is used in conjunction with an oscilloscope to provide an intensified display of a selected portion of an input waveform.
(23)	Start/Stop Connector	BNC connector. A TTL compatible input used for external gate control in the Totalize function. The first falling edge or closure to ground causes the gate to open and then next causes the gate to close.
(24)	Gate Output Connector	BNC connector. A negative-going TTL compatible equivalent of the gate signal.
(25)	Reference Input and Output Connectors	 BNC connectors. The output connector provides a TTL compatible output of the 10 MHz internal frequency reference. The input connector allows the use of an external frequency reference of 1, 5 or 10 MHz at 1V RMS.
(26)	External Gate Control Connector and Switch	 BNC connector. Refer to subsection 2.13 for a detailed description.

Table 2.1 - Controls, Indicators and Connectors continued

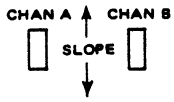
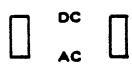
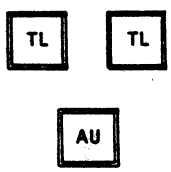
Reference	Item	Function
(27)	Normal/Hold Switch	The instrument operates normally until the switch is set to the Hold position. In this mode, the instrument will take one reading instead of continuous readings. A new reading may be taken by pressing the RESET key.
(28)	Slope Select Switches	 The ↑ position sets the appropriate channel to trigger on the positive slope of the input waveform. The ↓ position sets the appropriate channel to trigger on the negative slope of the input waveform.
(29)	Coupling Select Switches	 The DC position sets the appropriate channel to the DC coupled mode. The AC position sets the appropriate channel to the AC coupled position. The switch on the left is for Channel A and the switch on the right is for Channel B.
(30)	Separate/Test/Common Switch	The Separate mode couples the A and B input connectors to their respective signal conditioners. The Test mode connects the 10 MHz reference signal to both the A and B signal conditioners, and disconnects the input connectors. The Common mode disconnects the Channel B input and couples the Channel A input signal to both the Channel A and Channel B signal conditioners. The Common mode allows the instrument to make Time Interval and Time Interval Average measurements with a single signal input (when the Channel A and B slope switches are set to opposite polarities).
(31)	Trigger Level Switches	 The Trigger Level keys (Channel A on the left and Channel B on the right) allow the user to select the desired trigger level value. The trigger level is settable to ± 300% of the selected voltage range (ie: 1V, 10V or 100V range). Example: Press: Channel A TL (TL display goes blank) Enter: 2.00 (2.00 appears in Channel A trigger level display and the Channel A "1" range is indicated) Press: Channel A TL (data is entered)

Table 2.1 - Controls, Indicators and Connectors continued

Reference	Item	Function
		The AU (automatic) key is used to automatically select the optimum trigger level for inputs ≥ 400 Hz (≥ 75 for Option 12) and ≥ 50 mV RMS. Example: Press: Channel B TL (TL display goes blank) Press: AU (the input signal amplitude is measured, the 50% point of the amplitude is computed and the data is entered and displayed).
(32)	TI	Selects Time Interval function.
	P	Selects Period function.
	AV	Used in conjunction with Period or Time Interval to select Period Average or Time Interval Average.
	SS	Used in conjunction with Totalize. The first key press starts the count (opens the gate) and the next key press stops the counts (closes the gate).
	F_A	Selects Frequency A function.
	F_C	Selects Frequency C function (Models 9035A, 9035/11A only).
	RA	Selects Ratio function.
	TO	Selects Totalize function.
	+	Used to add constants to measurement values.
	X	Used to multiply measurement values by an entered constant.
	÷	Used to divide measurement values by an entered constant.
	1/X	Inverts measurement value. May be used to convert Period to Frequency, etc.
	Numeric Keys (0 thru 9)	Used to enter values for constants or to enter desired Gate/Time Multiplier for the function selected.
	EX	Used to enter an exponent as part of a constant in arithmetic operations.
	RM	Used to bring the instrument into local control when the 9000A's operating (through Option 55) on the GPIB bus. This return to local capability is inhibited if the remote controller sends a local lockout (LLO) command to the 9000A.

Table 2.1 - Controls, Indicators and Connectors continued

Reference	Item	Function
	IT	Causes the instrument to clear all registers and return to the home state (Time Interval, 10 nsec, trigger levels set to 0V RMS and 100V range).
	•	Used to insert decimal points when entering numeric values.
	CS	Used to change the sign of the following data entries: a. With a measurement function selected, the CS key selects the polarity of the timebase/multiplier value. b. With an arithmetic key selected, the CS key selects the polarity of the display data. c. With the exponent (EX) selected, the CS key selects the polarity of the exponent. d. With the channel A trigger level (TL) selected, the CS key selects the polarity of the channel A trigger level. e. With the channel B trigger level (TL) selected, the CS key selects the polarity of the channel B trigger level.
	RS	Used to clear the display to zero, reset the internal logic and initiate a new measurement.
	CK	Used to check the operation of the 7-segment display LED's. When pressed, it causes all 8's to appear.
		Selects Pulse Width function (-11A Models)
		Selects Rise Time function (-11A Models)
		Selects Fall Time function (-11A Models)

Table 2.2 - Gate/Time Multiplier

ıebase	TI Input: 1 Hz	Display Scale	P Input: 1 Hz	Display Scale	F_A Input: 50 MHz	Display Scale
+1					5 0 . 0 0 0 0 0 0 0 0	M Hz
0			1 .	sec	5 0 . 0 0 0 0 0 0 0	M Hz
−1	. 5	sec	1 . 0	sec	5 0 . 0 0 0 0 0 0	M Hz
−2	. 5 0	sec	1 . 0 0	sec	5 0 . 0 0 0 0	M Hz
−3	5 0 0 .	m sec	1 . 0 0 0	sec	5 0 . 0 0 0	M Hz
−4	5 0 0 . 0	m sec	1 . 0 0 0 0	sec	5 0 . 0 0	M Hz
−5	5 0 0 . 0 0	m sec	1 . 0 0 0 0 0	sec	5 0 . 0	M Hz
−6	5 0 0 . 0 0 0	m sec	1 . 0 0 0 0 0 0	sec	5 0 .	M Hz
−7	5 0 0 . 0 0 0 0	m sec	1 . 0 0 0 0 0 0 0	sec		
−8	5 0 0 . 0 0 0 0 0	m sec	1 . 0 0 0 0 0 0 0 0	sec		

Timebase	TIA Input: 1.MHz	Display Scale	PA Input: 2 MHz	Display Scale	A/B Input: 50 MHz
0	. 5 0	μ sec	. 5 0	μ sec	
+1	5 0 0 .	n sec	5 0 0 .	n sec	1 . 0
+2	5 0 0 . 0	n sec	5 0 0 . 0	n sec	1 . 0 0
+3	5 0 0 . 0 0	n sec	5 0 0 . 0 0	n sec	1 . 0 0 0
+4	5 0 0 . 0 0 0	n sec	5 0 0 . 0 0 0	n sec	1 . 0 0 0 0
+5	5 0 0 . 0 0 0 0	n sec	5 0 0 . 0 0 0 0	n sec	1 . 0 0 0 0 0
+6	5 0 0 . 0 0 0 0 0	n sec	5 0 0 . 0 0 0 0 0	n sec	1 . 0 0 0 0 0 0
+7	5 0 0 . 0 0 0 0 0 0	n sec	5 0 0 . 0 0 0 0 0 0	n sec	1 . 0 0 0 0 0 0 0
+8					1 . 0 0 0 0 0 0 0 0

NOTE: Shaded area denotes "Home State".

2.10 OPERATION.

2.10.1 The remainder of this section deals with the use of the instrument by means of the manual controls and various practical aspects of its various features. The operation of the instrument through the use of the electrical interface is covered in Section 3.

2.10.2 General Usage Instructions.

2.10.2.1 Applying power to the instrument causes the instrument to select the TI function at "home base". A separate "home base" exists for each function and consists of an internally programmed selection of the timebase/multiplier value.

2.10.2.2 The purpose of the home base is to select an appropriate timebase/multiplier for the function selected to make a fast, first measurement. A tabulation of the home states is given below.

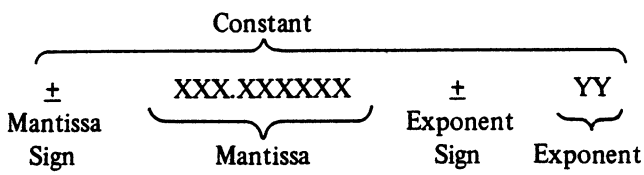
Function	Timebase/Multiplier	Scale
TI	10^{-8} sec (10 ns)	Sec
TIA	10^{1}	Sec
P	10^{-8} sec (10 ns)	Sec
PA	10^{1}	Sec
F_A	10^{-1} (.1 sec)	Hz
F_C	10^{-1} (.1 sec)	Hz
A/B	10^{1}	(Blank)

2.10.2.3 *Function Tables.* Tables 2.3 through 2.10 provide setup information and examples of measurements for each function.

2.10.3 Arithmetic Computation.

2.10.3.1 Arithmetic computation is a standard feature of the Series 9000A and permits a variety of direct conversions and manipulations of the measurement. Units such as radians, RPM, minutes, etc., can be displayed directly, either by local or remote programming, without the need of an external calculator/controller or computer.

2.10.3.2 The constant used in computation is shown below.



The mantissa may be any length from 1 to 9 digits. The exponent multiplies the mantissa by 10, raised to any power from –99 to 99. The constant appears in the display as it is entered. Once entered, the constant remains until a function key is pressed, an INT key is pressed, or until the constant is changed. Examples of operation, addition, subtraction, multiplication, division, and reciprocal are provided in tables 2.11 through 2.14.

2.10.4 Trigger Level.

2.10.4.1 The ability to accurately select the trigger levels of channels A and B, either manually or automatically, is a particular aid in making rapid and accurate measurements. The operation of the trigger level controls is covered in table 2.15.

2.10.5 Pulse Parameter (-11A Models).

2.10.5.1 The pulse parameter measurement is used in conjunction with TI and TIA modes and provides automatic measurements of pulse width, rise time and fall time.

2.10.5.2 The pulse measurements are selected on the ⎍, ⎍ and ⎲ keys, which replace the standard arithmetic keys (except reciprocal) and the exponent key. Examples of pulse measurements are shown in tables 2.16 through 2.18.

2.11 OPTION 56, HIGH SPEED INTERFACE.

2.11.1 Connection of the Series 9000A Counter to a minicomputer is made possible through use of the Option 56 High Speed Computer Interface. This accessory is an optional printed circuit board designed for installation within the Series 9000A counter. This interface provides the electrical interface necessary for controlling the function of the counter and for transferring measurement information from the counter to the computer.

2.11.2 The Option 56 interface is designed to provide high speed transfer of measurement information to minicomputers such as the Digital Equipment Corporation (DEC) PDP-11, Digital Computer Controls D-116 or the Data General NOVA series. Connection of the Series 9000A Counter to a computer or system as a peripheral device requires that an interface board be provided within the mainframe of the computer to transmit control signals and function control information to the counter and to receive status signals and measurement information from the counter.

2.11.3 The information presented herein is provided to enable the minicomputer user to design the necessary interface board or to modify a general purpose interface board for installation in the computer and to prepare the software necessary to operate the counter under computer program control.

2.12 HIGH-SPEED INTERFACE INSTALLATION.

2.12.1 The physical configuration of the high-speed interface board and its installation in the Series 9000A Counter is illustrated in figure 2.5. The interface board is mounted on and at a right-angle to the main printed circuit board of the counter. The electrical interface with the counter circuitry is accomplished through edge mounted female connectors on the interface board which mate with male connectors on the counter main printed circuit board.

2.12.2 The electrical interface connection between the high speed interface board and the computer is accomplished through two 36-line flat ribbon cables. These cables are permanently affixed to the interface board by solder connection to the component side of the board and the other ends of the cables are terminated at two 36-pin jacks located on the rear panel of the counter. In addition to the interface board and cables it is necessary to add one read-only-memory (ROM) module to the counter. The ROM is added to an existing socket (U8) located on the control board.

2.12.3 Field installation is a relatively simple task; the board is plugged into its location on the main counter board and the cable connectors are fastened in existing openings in the rear panel of the counter. Units already manufactured and in use in the field have cover plates in place over the connector holes. With the interface board and connectors installed the counter is ready for connection to a minicomputer system as a peripheral unit.

2.12.4 The electrical interface is described in Section 3 because it is closely related to programming considerations (paragraph 3.16.3).

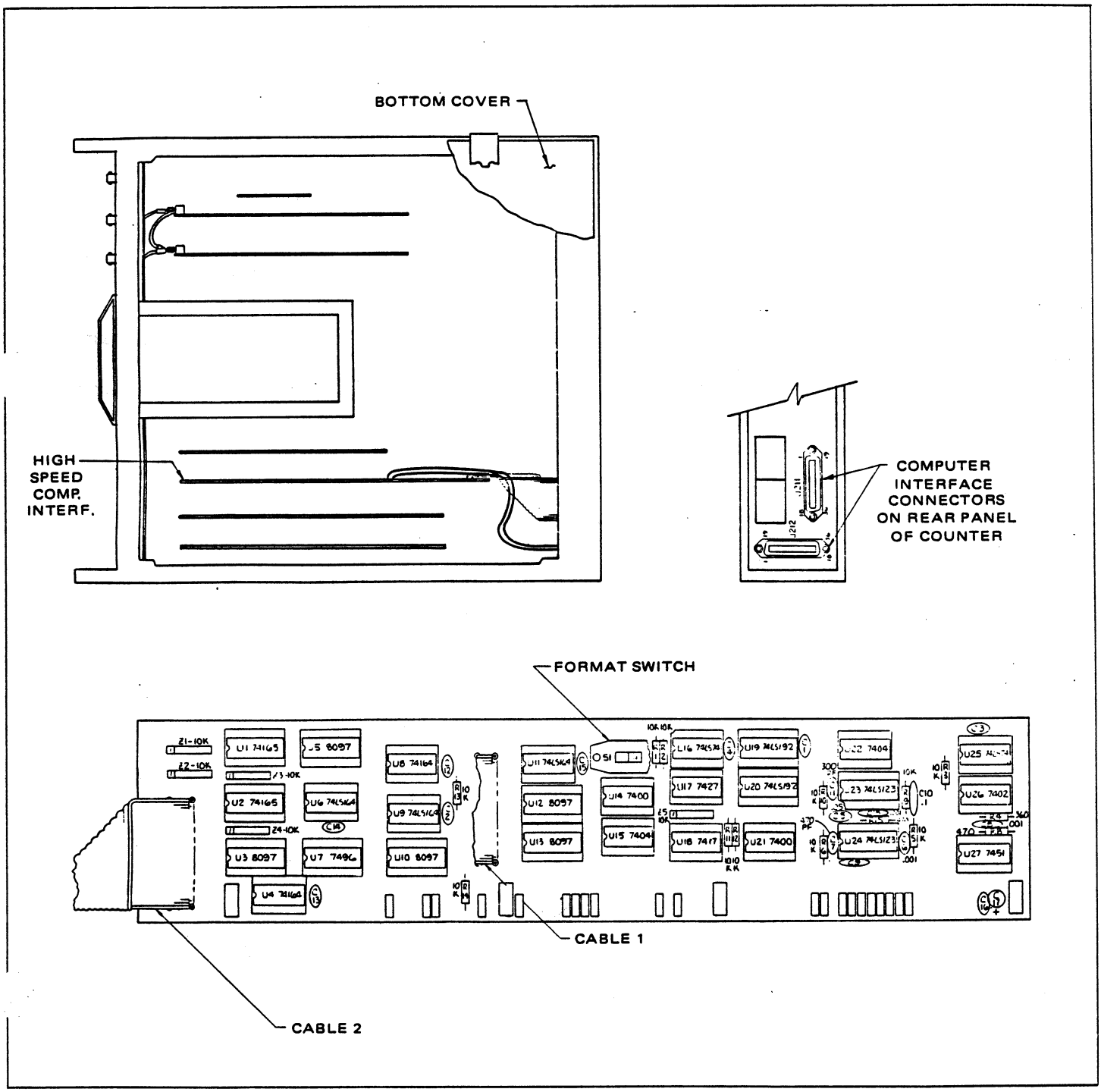
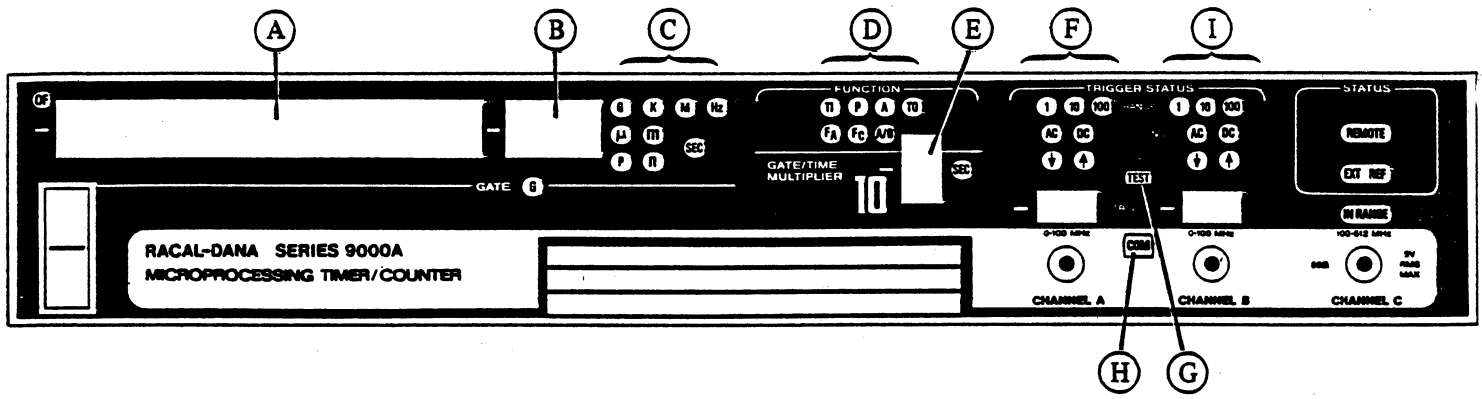


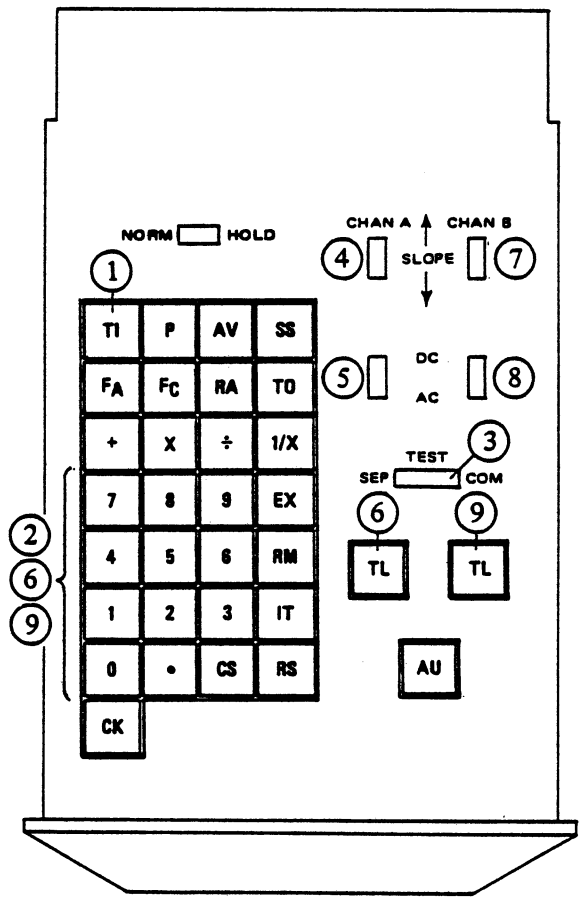
Figure 2.5 - High Speed Computer Interface

Table 2.3 - Time Interval Measurement



TIME INTERVAL

This function is used to measure the elapsed time between two separate inputs or the width of a common input pulse.



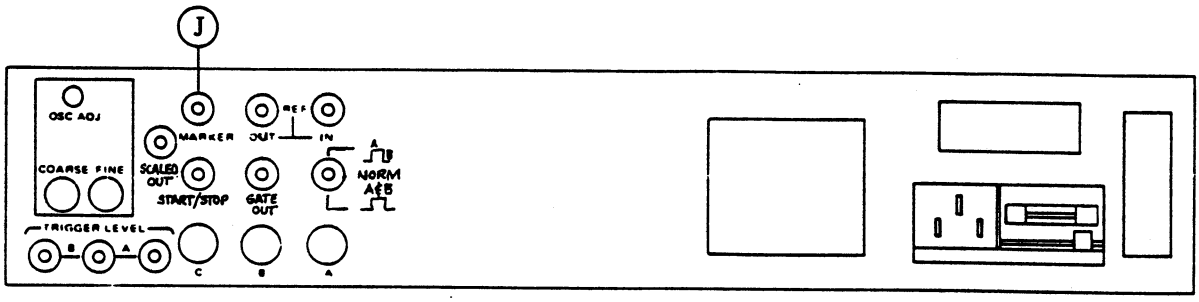
RANGE:	10 nanoseconds to 10^9 sec
INPUT SEPARATE MODE:	CH A Start and CH B Stop
COMMON MODE:	CH A Start and Stop

KEYBOARD

(1)	FUNCTION:	TI
(2)	RESOLUTION:	Select –8 (Home) to +1
(3)	MODE:	Select SEP or COM according to measurement
(4)	CH A SLOPE:	Select Slope of TI Start
(5)	CH A COUPLING:	Select Coupling of TI Start
(6)	CH A TRIGGER LEVEL:	TL 3-digit TL value with decimal point TL
(7)	CH B SLOPE:	Select Slope of TI Stop
(8)	CH B COUPLING:	Select Coupling of TI Stop
(9)	CH B TRIGGER LEVEL:	TL 3-digit TL value with decimal point TL

FRONT PANEL

(A)	Display:	Dependent on Input
(B)	Display:	Dependent on Input
(C)	Display Units:	Dependent on Input
(D)	Function:	TI
(E)	Resolution:	Selected
(F)	CH A Status:	Selected
(G)	Test:	Blank
(H)	Com:	Selected
(I)	CH B Status:	Selected



REAR PANEL

(J) MARKER

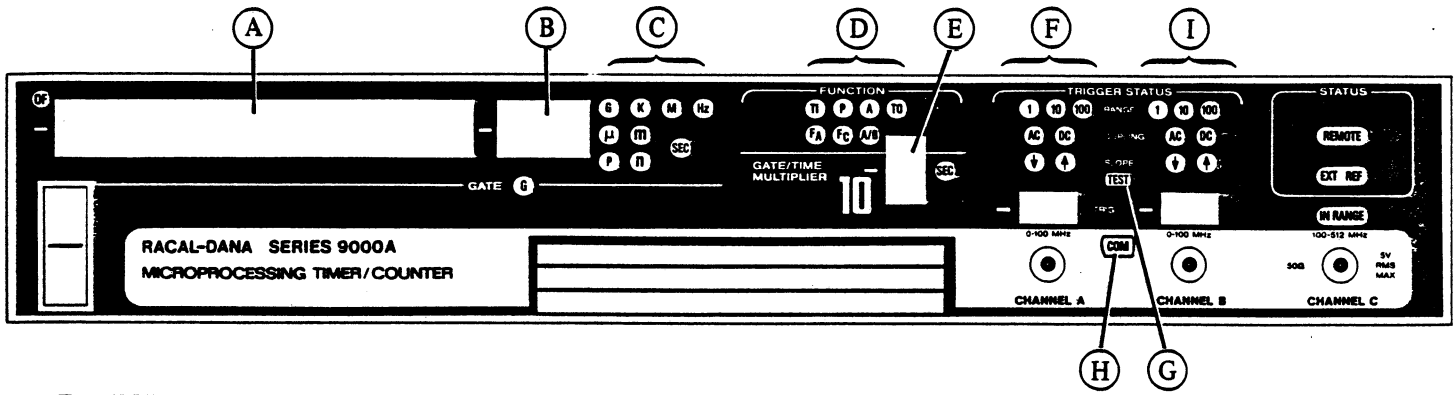
To use the marker, (J) on the rear panel, tee off of the input signal of channel A and connect to the vertical input of the oscilloscope. Connect MARKER output of counter to Z axis of oscilloscope. MARKER output voltage swing is from +3 to −12.

EXAMPLE

The Time Interval between the leading and falling edge of a 1 kHz, 5 volt square wave is to be read. The pulse is connected to the channel A input. A resolution of 10 ns (10^{-8}s) is required.

(1)	TI		(A)	500.00	
(2)	−8		(B)	Blank	
(3)	COM		(C)	μ, Sec	
(4)	↑		(D)	TI	
(5)	AC		(E)	−8	
(6)	TL		(F)	↑ AC	0.00 (±.01)
	AU		(G)	Blank	
			(H)	Com	
(7)	↓		(I)	↑ AC	0.00 (±.01)
(8)	AC				
(9)	TL				
	AU				

Table 2.4 - Time Interval Average Measurement



TIME INTERVAL AVERAGE

This function provides greater resolution than TI, when measuring repetitive inputs that are asynchronous with the counter's reference oscillator (100 MHz). If the input signal approaches a sub-harmonic of the reference frequency, a greater number of time intervals will have to be averaged to achieve good accuracy. The accuracy is found by the following equation.

$$\pm \text{Reference error} \pm 2 \text{ nsec} \pm \frac{(\text{Trigger error} \pm 10 \text{ nsec})}{\sqrt{\text{Number of Intervals Averaged}}}$$

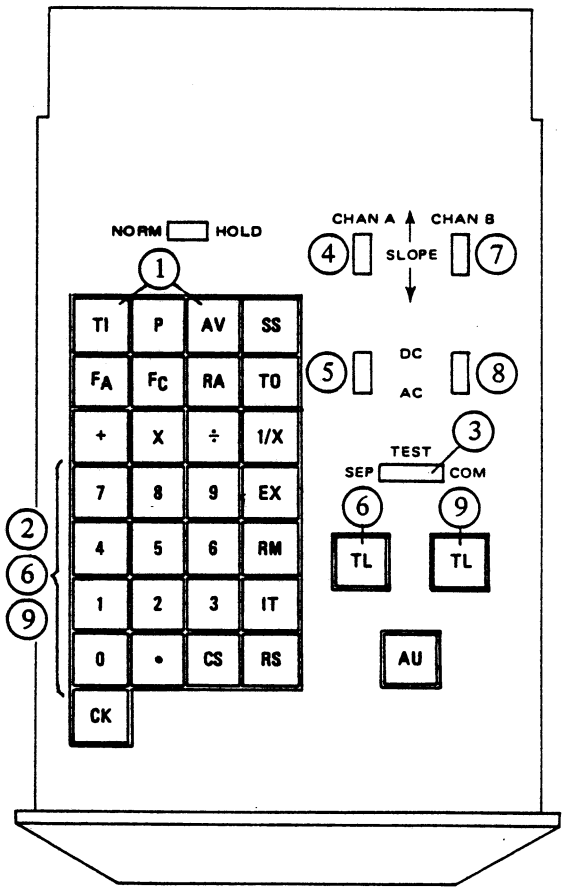
Where:

$$\text{Trigger error} = \frac{\leq 0.0025}{\text{Signal Slope (V/sec)}}$$

RANGE:	100 picosecond to 1 second
INPUT SEPARATE MODE:	CH A Start and CH B Stop
COMMON MODE:	CH A Start and Stop

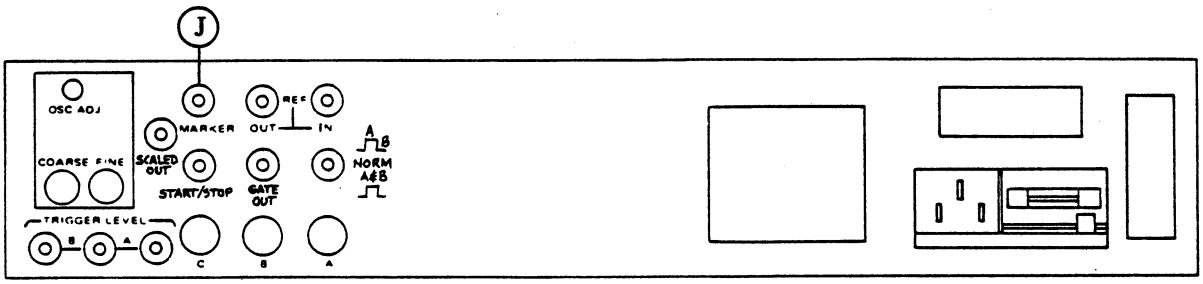
KEYBOARD

(1)	FUNCTION:	TI, AV
(2)	MULTIPLIER:	Select 1 to 9
(3)	MODE:	SEP or COM according to measurement
(4)	CH A SLOPE:	Slope of Start
(5)	CH A COUPLING:	Coupling of Start
(6)	CH A TRIGGER LEVEL:	TL 3-digit value with decimal TL
(7)	CH B SLOPE:	Slope of Stop
(8)	CH B COUPLING:	Coupling of Stop
(9)	CH B TRIGGER LEVEL:	TL 3-digit value with decimal TL



FRONT PANEL

(A)	Display:	Dependent on Input
(B)	Display:	Dependent on Input
(C)	Display Units:	Dependent on Input
(D)	Function:	TIA
(E)	Multiplier:	Selected
(F)	CH A Status:	Selected
(G)	Test:	Blank
(H)	Common:	Selected
(I)	CH B Status:	Selected



REAR PANEL

(J) MARKER

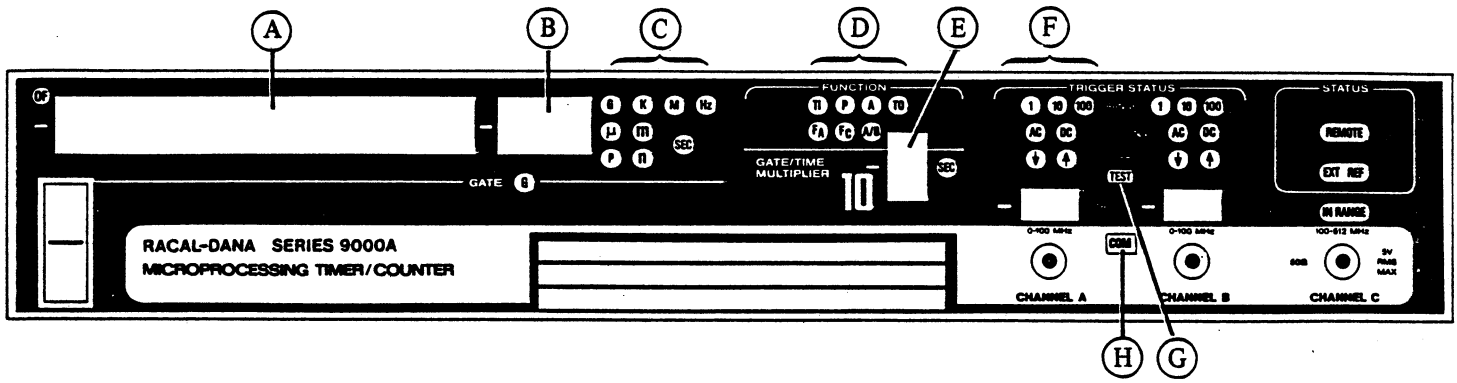
To use the marker, (J) on the rear panel, tee off of the input signal of channel A and connect to the vertical input of the oscilloscope. Connect MARKER output of counter to Z axis of oscilloscope. MARKER output voltage swing is from +3 to −12.

EXAMPLE

The Time Interval Average between the leading and trailing edge of a 1 volt, 1 kHz square wave signal over 10^2 periods.

(1)	TIA	(A)	500.0000
(2)	2	(B)	Blank
(3)	COM	(C)	μ, Sec
(4)	↑	(D)	TIA
(5)	AC	(E)	2
(6)	TL	(F)	↑ , AC, 0.00 (±.01)
	AU	(G)	Blank
(7)	↓	(H)	Com
(8)	AC	(I)	↓ , AC, 0.00 (±.01)
(9)	TL		
	AU		

Table 2.5 - Period Measurement

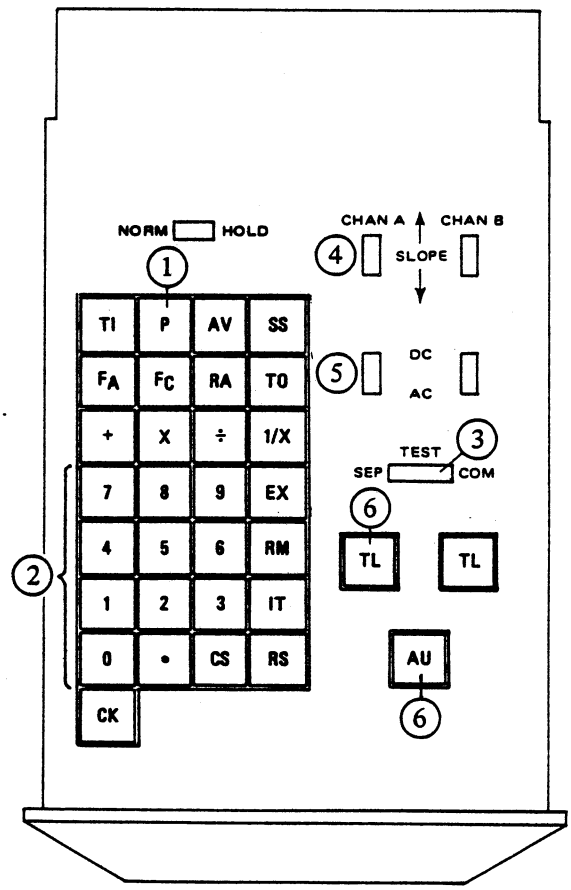


PERIOD

This function measures the period of time required for one complete cycle of an input signal and is the reciprocal of the frequency of the input. For low frequency measurements (≤10 kHz) more resolution can be obtained in a reasonable time by measuring the period of the signal and deriving the reciprocal (1/X) as described in table 2.13.

RANGE: 10 nanoseconds to 10^{10} second, 0 – 100 MHz Input

INPUT: Channel A



KEYBOARD

(1) FUNCTION: P
(2) RESOLUTION: Select –8 to +1
(3) MODE: Separate
(4) CH A SLOPE: ↑ or ↓
(5) CH A COUPLING: AC or DC
(6) CH A TRIGGER LEVEL: TL
Auto

FRONT PANEL

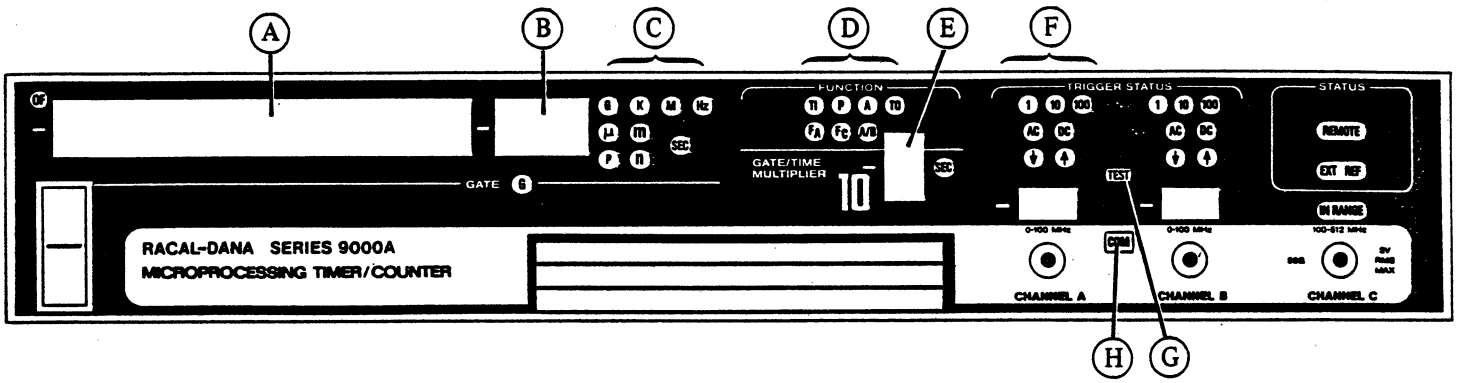
(A)	Display:	Dependent on Input
(B)	Exponent:	Dependent on Input
(C)	Display Units:	Dependent on Input
(D)	Function:	P
(E)	Resolution:	Selected
(F)	CH A Status:	Selected & Computed
(G)	Test:	Blank
(H)	Common	Blank

EXAMPLE

The Period of a 1 volt, 1 kHz square wave signal is desired.

(1)	P	(A)	1.00000 (999.99)
(2)	–8	(B)	Blank
(3)	SEP	(C)	m, SEC (μ, Sec)
(4)	↑	(D)	P
(5)	AC	(E)	–8
(6)	TL	(F)	↑, AC, 0.00 ± .01
	AU	(G)	Blank
		(H)	Blank

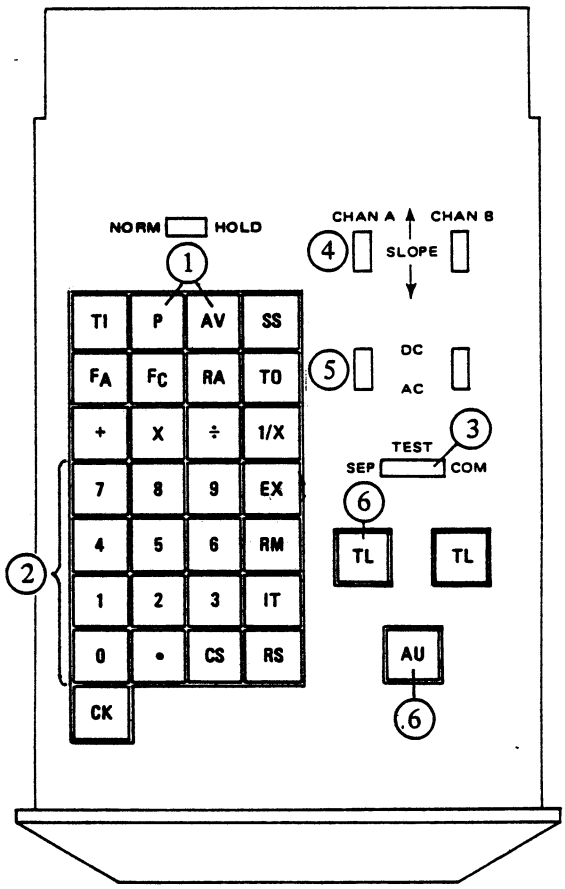
Table 2.6 - Period Average Measurement



PERIOD AVERAGE

This function permits the measurement of the period of repetitive, sinusoidal waveforms to higher resolution than can be achieved in Periodic measurement.

RANGE:	10 nanoseconds to 1 second
INPUT:	Channel A
INTERVALS AVERAGED:	1 to 10^8



KEYBOARD

(1)	FUNCTION:	P, AV
(2)	MULTIPLIER:	Selected, 1 to 8
(3)	MODE:	Separate
(4)	CH A SLOPE:	↑ or ↓
(5)	CH A COUPLING:	AC or DC
(6)	CH A TRIGGER LEVEL:	TL Auto

FRONT PANEL

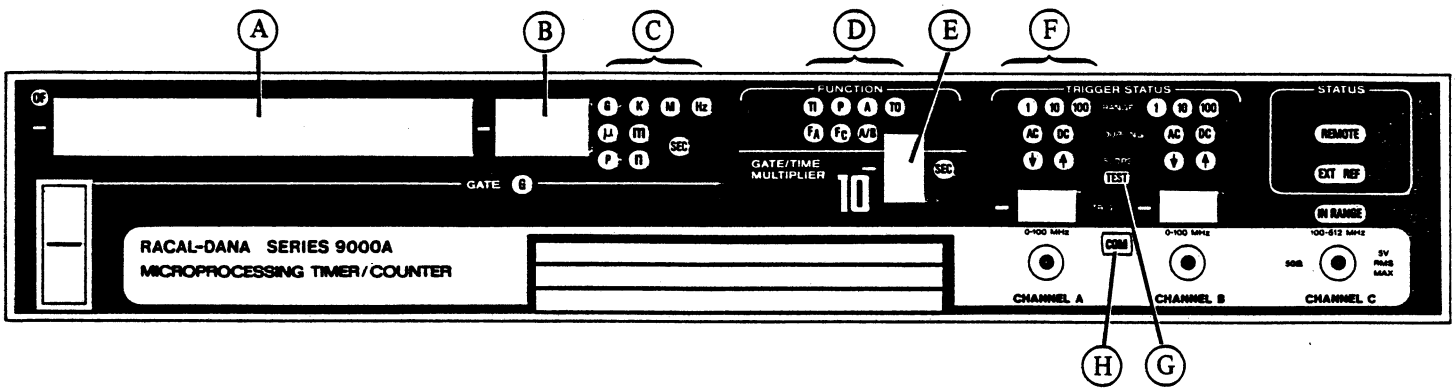
(A)	Display:	Dependent on Input
(B)	Exponent:	Dependent on Input
(C)	Units:	Dependent on Input
(D)	Function:	PA
(E)	Multiplier:	Selected
(F)	CH A Status:	Selected and Computed
(G)	Test:	Blank
(H)	Com:	Blank

EXAMPLE

The Period Average of a 1 volt, 2 kHz square wave is desired over 10^2 periods.

(1)	P, AV	(A)	0.5000000
(2)	2	(B)	0
(3)	SEP	(C)	msec
(4)	↑	(D)	PA
(5)	AC	(E)	2
(6)	TL	(F)	1, AC, ↑, 0.00 ± .01
	AU	(G)	Blank
		(H)	Blank

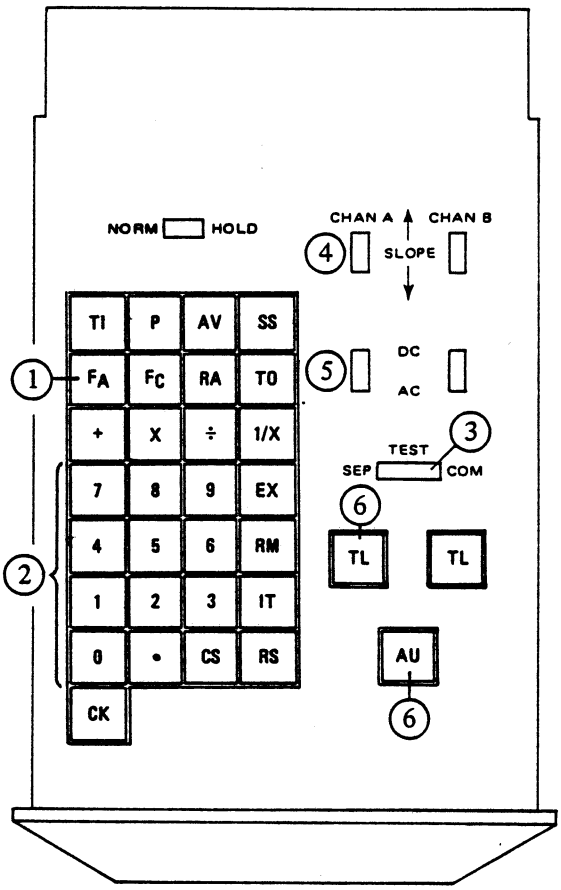
Table 2.7 - Frequency Measurement, 0 – 100 MHz (F_A)



F_A

This function allows measurement of input frequencies from near DC to 100 MHz.

RANGE:	1 μS to 10 sec
INPUT:	Channel A
GATE TIME:	1 μs to 10s



KEYBOARD

(1)	FUNCTION:	F_A
(2)	GATE TIME:	Selected –6 to 1
(3)	MODE:	Separate
(4)	CH A SLOPE:	↑ or ↓
(5)	CH A COUPLING:	AC or DC
(6)	CH A TRIGGER LEVEL:	TL Auto

FRONT PANEL

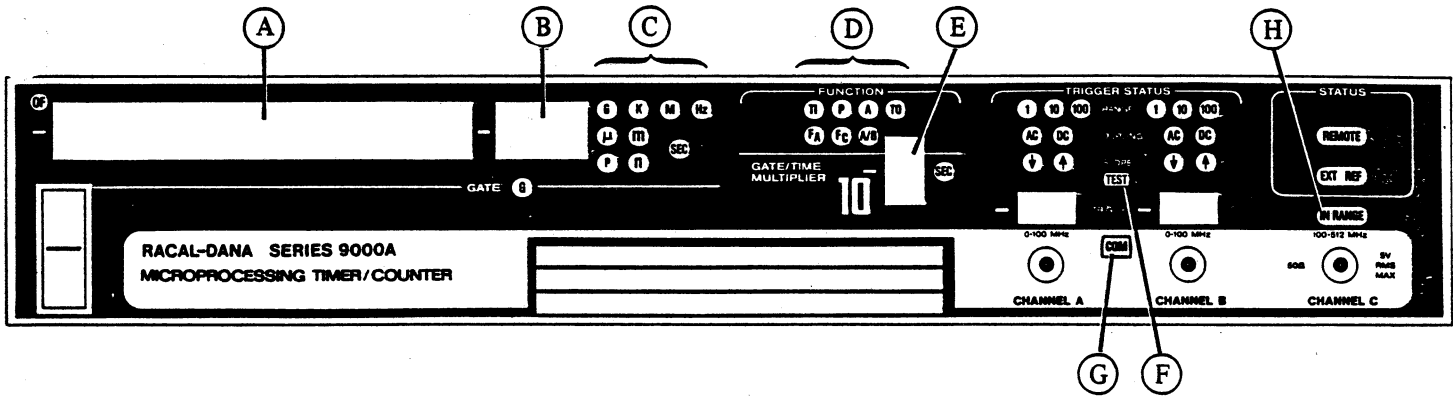
(A)	Display:	Dependent on Input
(B)	Exponent:	
(C)	Units:	Dependent on Input
(D)	Function:	F_A
(E)	Timebase:	Selected
(F)	CH A Status:	Selected & Computed
(G)	Test:	Blank
(H)	Com:	Blank

EXAMPLE

The frequency of a 1 volt, 2 kHz square wave is to be measured.

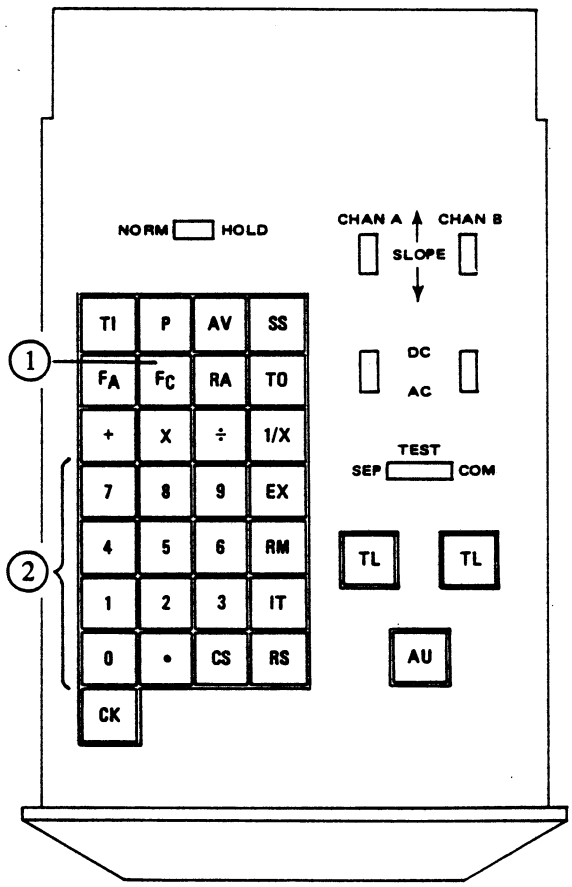
(1)	F_A	(A)	2.000
(2)	0	(B)	Blank
(3)	SEP	(C)	kHz
(4)	↑	(D)	F_A
(5)	AC	(E)	0
(6)	TL	(F)	1, AC, ↑, 0.00 (±.01)
	AU	(H)	Blank
		(G)	Blank

Table 2.8 - Frequency Measurement, 100 – 512 MHz (F_C), Models 9035, 9035/11A Only



F_C

This function allows measurement of RF signals of from 100 MHz to 512 MHz into 50Ω with signal levels down to 15 mV rms. The application of a suitable input (proper amplitude and frequency) is indicated by an IN-RANGE light above the channel C input connector.



KEYBOARD

(1)	FUNCTION:	F_C
(2)	GATE TIME:	Selected –6 to 1

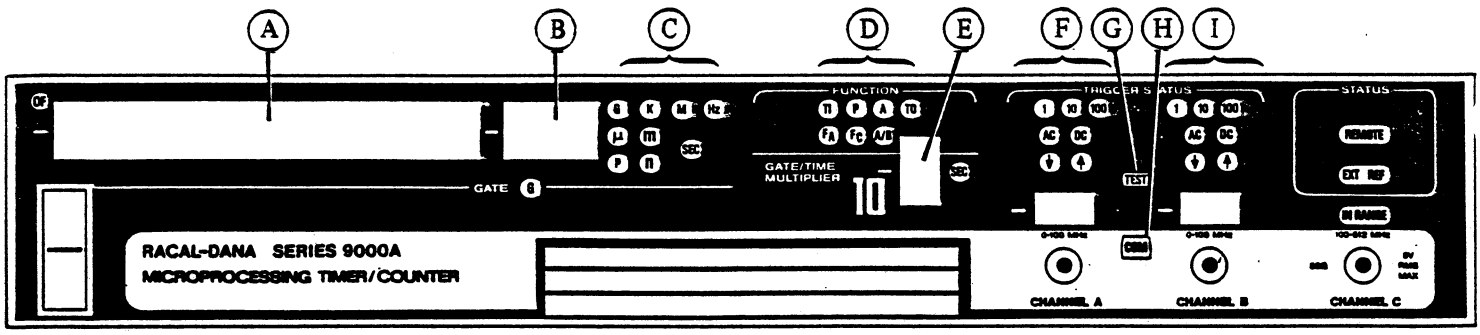
FRONT PANEL

(A)	Display:	Dependent on Input
(B)	Exponent:	Dependent on Input
(C)	Units:	Dependent on Input
(D)	Function:	F_C
(E)	Timebase:	Selected
(F)	Test:	Blank
(G)	COM:	N/A
(H)	Acceptable Input:	IN-RANGE

EXAMPLE

An input signal of about 400 MHz is to be measured.

(1)	F_C	(A)	417.0000
(2)	–1	(B)	Blank
		(C)	MHz
		(D)	F_C
		(E)	–1
		(F)	Blank
		(G)	Blank
		(H)	IN-RANGE



A/B RATIO

This function allows the user to directly measure the ratio between two frequencies with total slope, range, coupling and trigger level control for both signal and reference input.

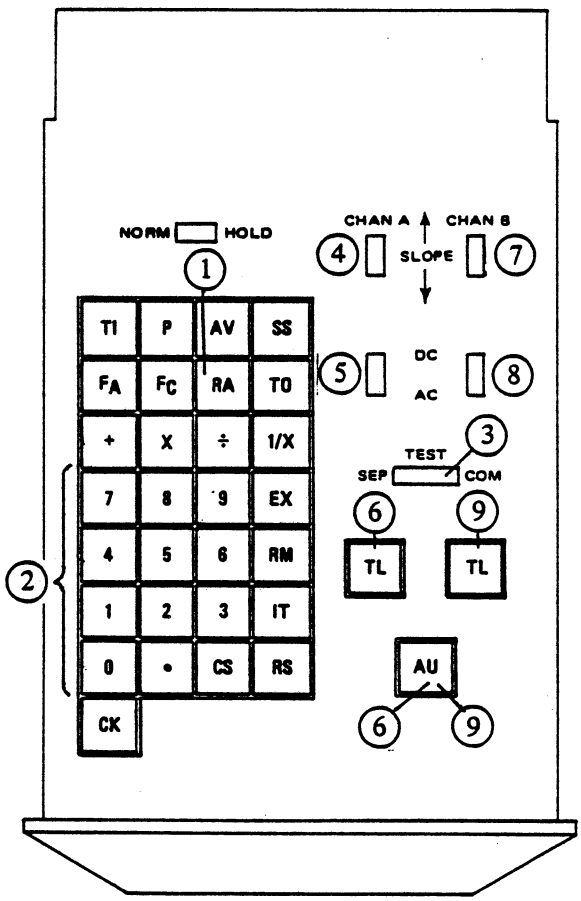
INPUT FREQUENCY RANGE:	0 – 100 MHz, both inputs
INPUT NUMERATOR:	CHANNEL A
DENOMINATOR:	CHANNEL B
MULTIPLIER:	10^0 to 10^9

KEYBOARD

(1)	FUNCTION:	RA
(2)	MULTIPLIER:	Selected, 10^0 to 10^9
(3)	MODE:	SEP
(4)	SLOPE:	↑ or ↓
(5)	COUPLING:	AC or DC
(6)	CH A TRIGGER LEVEL:	TL Auto
(7)	SLOPE:	↑ or ↓
(8)	COUPLING:	AC or DC
(9)	CH B TRIGGER LEVEL:	TL Auto

FRONT PANEL

(A)	Display:	Dependent on Input
(B)	Exponent:	Dependent on Input
(C)	Display Units:	Dependent on Input
(D)	Function:	RA
(E)	Multiplier:	Selected
(F)	CH A Status:	Selected & Computed
(G)	Test:	Blank
(H)	Mode:	Selected
(I)	CH B Status:	Selected, Computed

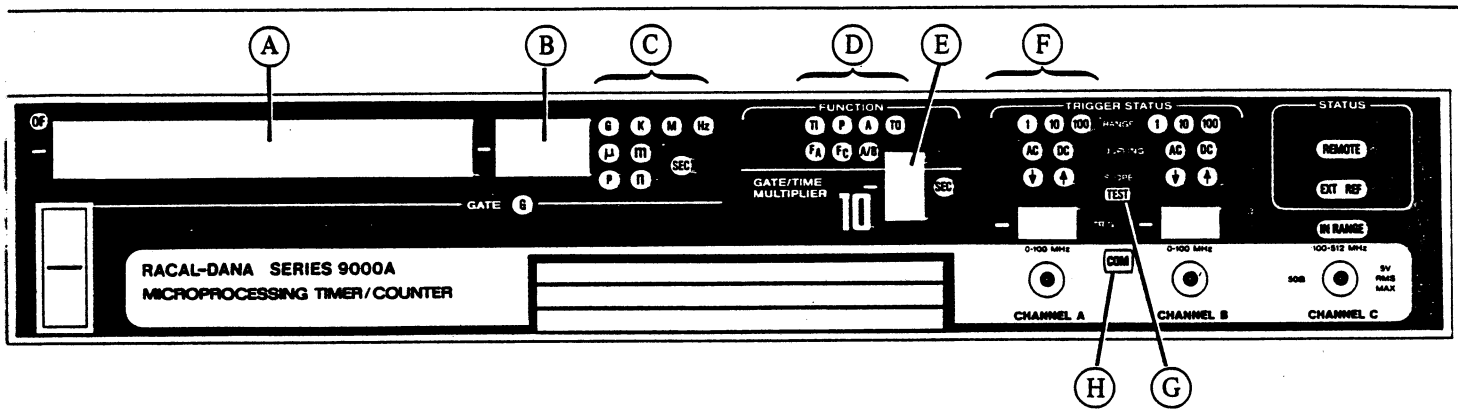


EXAMPLE

The ratio of two frequencies is desired; a 1 volt, 1 kHz square wave is to be compared with a 1 volt RMS, 1.1 kHz sinewave.

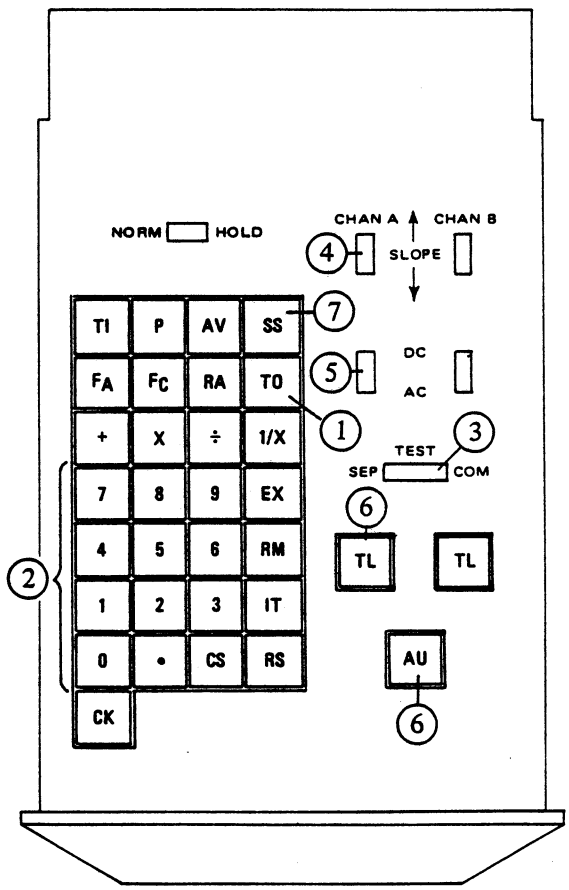
(1)	RA	(A)	909.
(2)	3	(B)	Blank
(3)	SEP	(C)	m
(4)	↑	(D)	RA
(5)	AC	(E)	3
(6)	TL AU	(F)	1, AC, ↑, 0.00 (±.01)
(7)	↑	(G)	Blank
(8)	AC	(H)	Blank
(9)	TL AU	(I)	1, AC, ↑, 0.00 (±.01)

Table 2.10 - Totalize



TOTALIZE

In this function, the instrument registers the aggregate of a series of input pulses, over a time period initiated by the user. The time period is controlled manually by the START/STOP key on the keyboard or electrically through the START/STOP BNC (I) on the rear panel. The input signal can also be scaled in this function from 10^0 to 10^9. The output is available at the SCALED OUT BNC (J) on the rear panel.

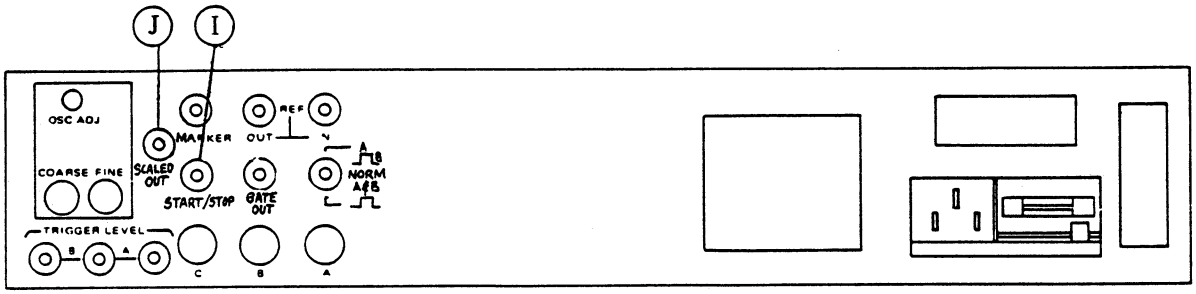


YBOARD

(1)	FUNCTION:	TO
(2)	SCALING FACTOR:	0 to 9
(3)	MODE:	SEP
(4)	CH A SLOPE:	↓ or ↑
(5)	CH A COUPLING:	AC or DC
(6)	CH A TRIGGER LEVEL:	TL Auto
(7)	START/STOP:	Press to Start, press to Stop

FRONT PANEL

(A)	Display:	Dependent on Input
(B)	Exponent:	
(C)	Units:	Dependent on Input
(D)	Function:	TO
(E)	Factor:	Selected, 10^0 to 10^9
(F)	CH A Status:	Selected, Computed
(G)	Test:	Blank
(I)	Com:	Blank



REAR PANEL

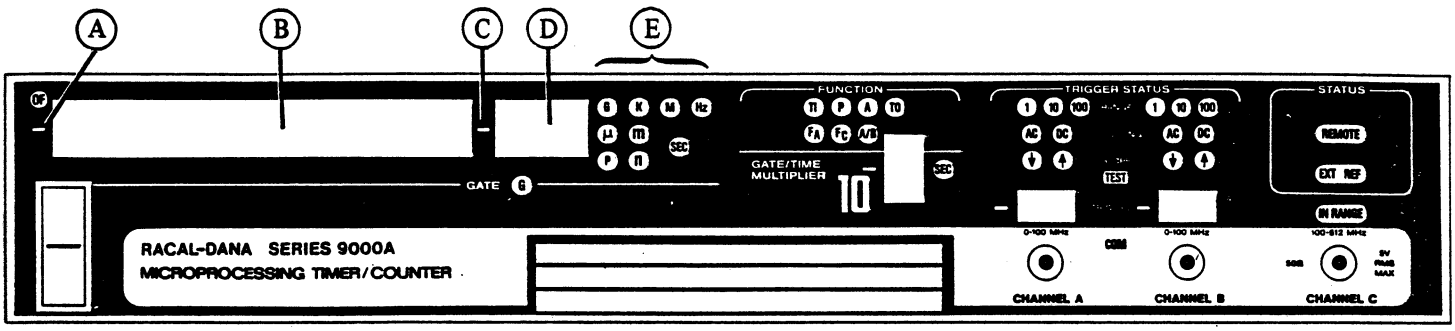
(I) START/STOP

(J) SCALED OUT

EXAMPLE

The operation of a 1 Volt pulse, 12-bit word generator is to be checked.

(1)	TO	(A)	12
(2)	1	(B)	Blank
(3)	SEP	(C)	m
(4)	↑	(D)	TOT
(5)	DC	(E)	1
(6)	TL	(F)	1, DC, ↑ .500
	.500	(G)	Blank
	TL	(H)	Blank
(7)	SS		
	Trigger Generator		
	SS		

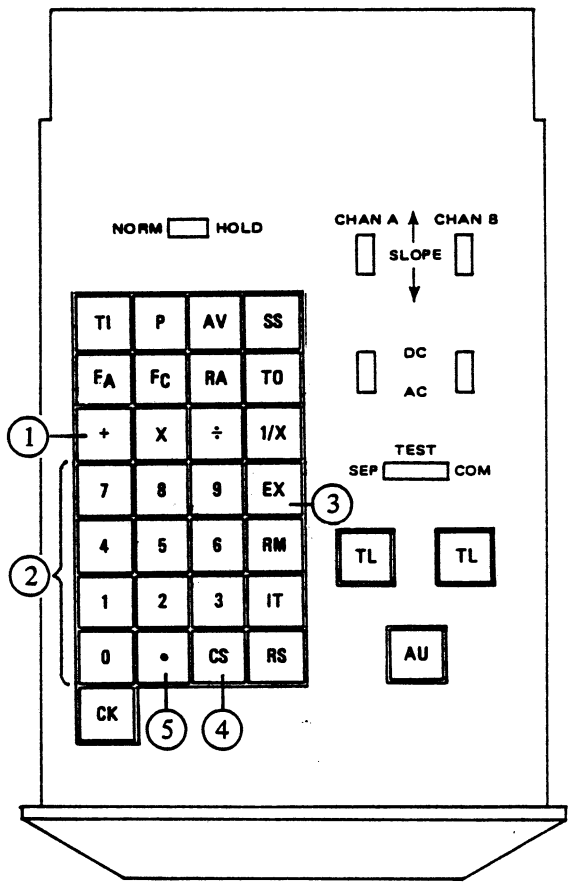


ADDITION

This operation, selected with the + key on the keyboard, allows the user to add or subtract a constant from any measurement. The mantissa of the constant can be either + or – and have from 1 to 9 digits. The exponent can be from ±0 to ±99.

The constant must be within the resolution of the measurement; any portion of the constant outside the measurement resolution is ignored.

The results of the addition or subtraction must be within the maximum allowable for the display (greater than 1 pico less than 10 Giga).



KEYBOARD

(1)	ARITHMETIC FUNCTION:	+
(2)	MANTISSA:	Any number 1 to 9 digits long
(3)	EXPONENT:	Exponent can be any number 1 to 99
(4)	CHANGE SIGN:	Changes sign of constant or exponent
(5)	DECIMAL:	Decimal point for constant

FRONT PANEL

(A)	Polarity of Display:	Dependent on input
(B)	Display:	Dependent on input
(C)	Polarity of Exponent:	Dependent on input
(D)	Exponent:	Dependent on input
	Display Units:	Hz and SEC blanked

OPERATION		ACTION
1.	Depress + key	μP is signalled and previously entered constant is displayed
2.	Enter constant	Constant is entered on the display
3.	Depress + key	Arithmetic operation is performed

EXAMPLE

37.45 milliseconds is to be added to the period measurement of a 1 Hz signal.

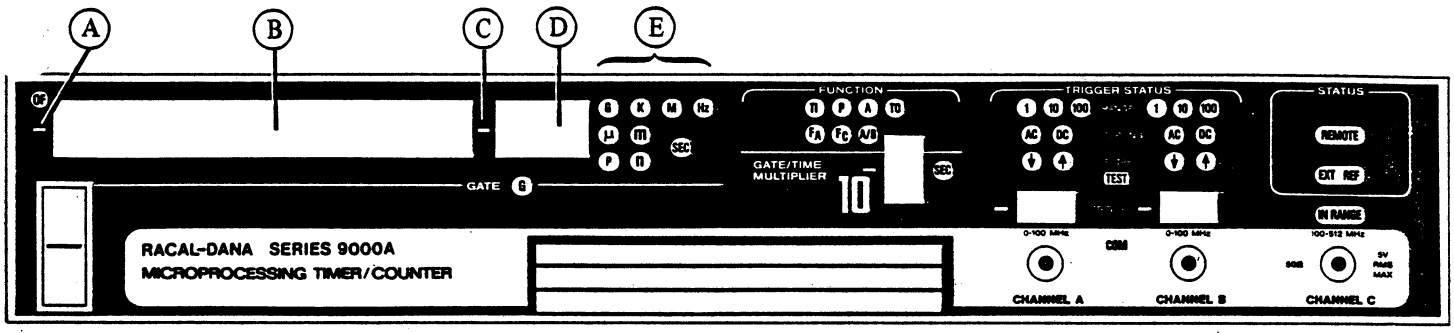
Measure the period of a 1 second pulse at a resolution of 10^{-4}s (see table 2.4).

(1)	+	(A)	Blank (Positive)
(2)	37.45	(B)	1.0375
(3)	EX	(C)	Blank
(4)	–	(D)	Blank
(2)	3	(E)	Blank
(1)	+		

EXAMPLE

The deviation of a 10 MHz frequency to 10 Hz resolution is to be monitored. 10,000,000 will be subtracted from the measurement. Measure the frequency (F_A) of a 10 MHz signal at a gate time of 10^{-1}s (see table 2.6).

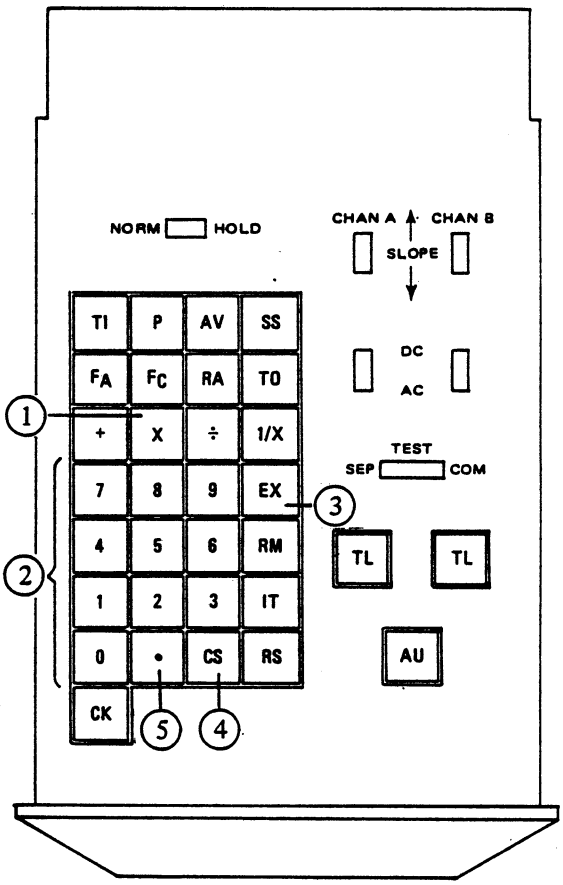
(1)	+	(A)	Dependent on Deviation
(4)	–	(B)	Blank or difference (amount of deviation)
(2)	10	(C)	Blank
(3)	EX	(D)	Blank
(2)	6	(E)	Blank
(1)	+		



MULTIPLICATION

This operation, selected with the x key on the keyboard, allows the user to multiply the measurement by a constant. The mantissa of the constant can be either + or – and have from 1 to 9 digits. The exponent can be from ±0 to ±99.

The product must be within the maximum allowable for the display (greater than 1 pico and less than 10 Giga).



KEYBOARD

(1)	ARITHMETIC FUNCTION:	x
◡	MANTISSA:	Any number, 1 to 9 digits long
(3)	EXPONENT:	Number can be raised to any power 1 to 99
(4)	CHANGE SIGN:	Changes sign of constant or exponent
(5)	DECIMAL:	Decimal point for constant

FRONT PANEL

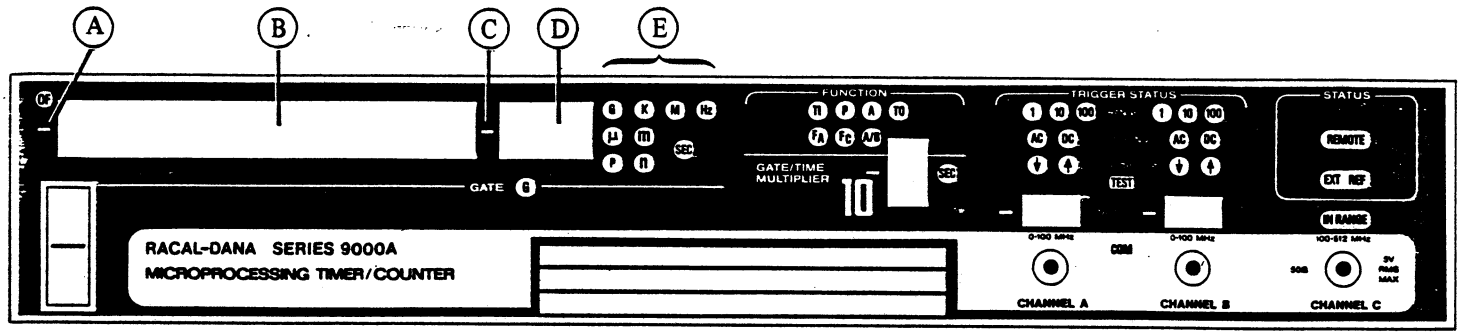
(A)	Polarity of Display:	Dependent on input
(B)	Display:	Dependent on input
(C)	Polarity of Exponent:	Dependent on input
(D)	Exponent:	Dependent on input
(E)	Display Units:	Hz and SEC Blanked

OPERATION		ACTION
1.	Depress x key	μP is signalled and previously entered constant is displayed
	Enter constant	Constant is entered on the display
3.	Depress x key	Multiplication is performed

EXAMPLE

10 MHz is to be converted to radians to 7 place accuracy. Measure the frequency (F_A) of a 10 MHz signal at a gate time of 10^{-1}s (see table 2.6).

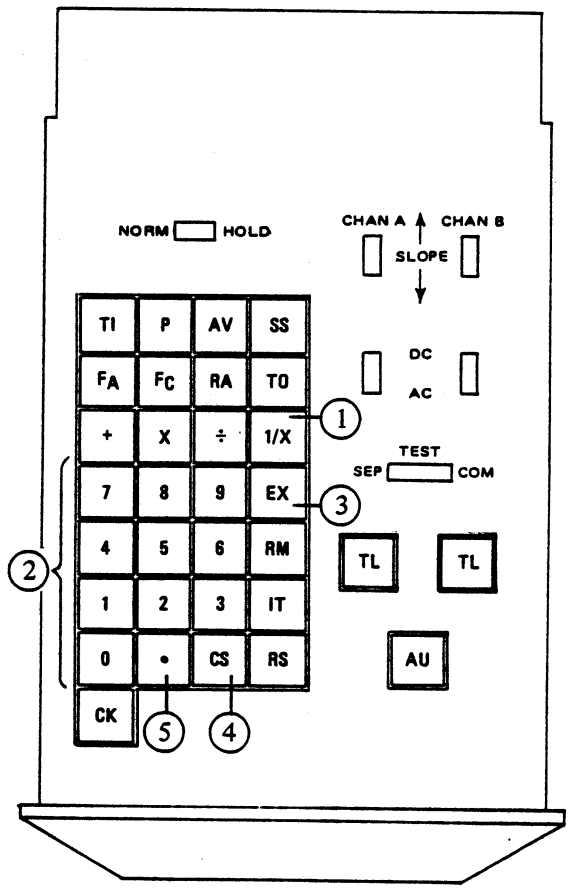
(1)	x	(A)	Blank
(2)	6.283185	(B)	62.83185
(1)	x	(C)	Blank
		(D)	Blank
		(E)	M



DIVISION

This operation, selected with the ÷ key on the keyboard, allows the user to divide the measurement by a constant. The mantissa of the component can be either + or – and have from 1 to 9 digits. The exponent can be from ±0 to ±99.

The quotient must be within the maximum allowable for the display (greater than 1 pico and less then 10 Giga).



KEYBOARD

(1)	ARITHMETIC FUNCTION:	÷
(2)	MANTISSA:	Any number, 1 to 9 digits long
(3)	EXPONENT:	Number can be raised to any power 1 to 99
(4)	CHANGE SIGN:	Changes sign of constant or exponent
(5)	DECIMAL:	Decimal point for constant

FRONT PANEL

(A)	Polarity of Display:	Dependent on input
(B)	Display:	Dependent on input
(C)	Polarity of Exponent:	Dependent on input
(D)	Exponent:	Dependent on input
(E)	Display Units:	Hz and SEC Blanked

EXAMPLE

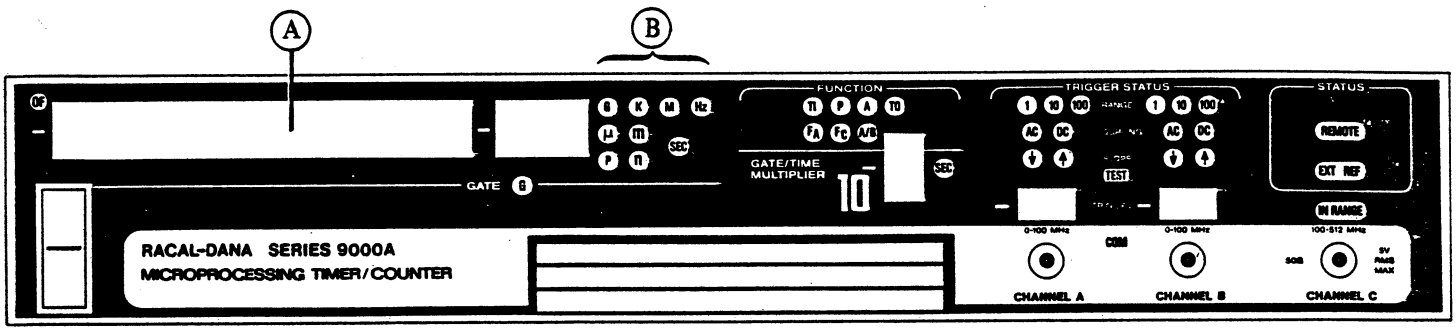
10 MHz is to be divided by 50. Measure the frequency (F_A) of a 10 MHz at a resolution of 10 Hz (see table 2.6).

OPERATION		ACTION
1.	Depress ÷ key	μP is signalled and previously entered constant is displayed
2.	Enter constant	Constant is entered on the display
3.	Depress ÷ key	Division is performed

(1)	÷
(2)	50
(1)	÷

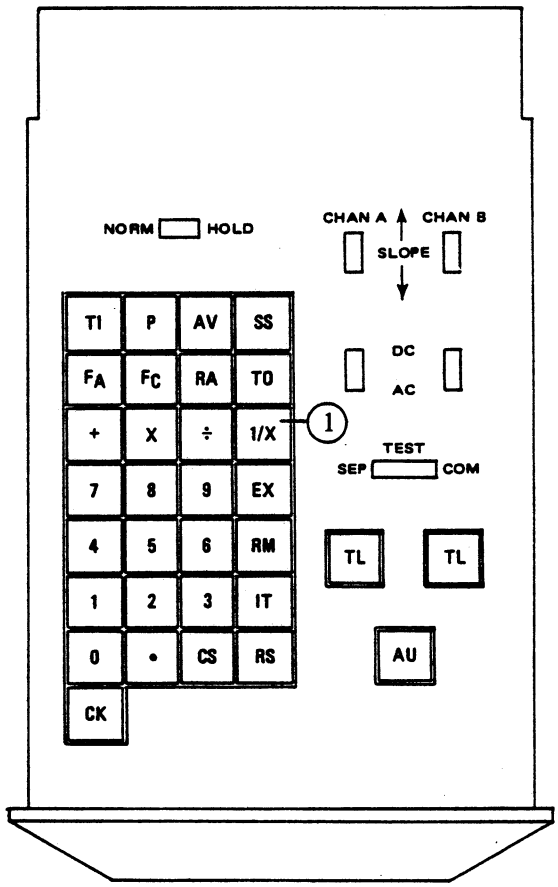
(A)	Blank
(B)	200.0000
(C)	Blank
(D)	Blank
(E)	K

Table 2.14 - Arithmetic Computation, Reciprocal



RECIPROCAL

This operation, selected with the 1/X key on the keyboard, allows the user to take the reciprocal of the measured value. This permits the accurate measurement of low frequencies by taking the reciprocal of a period or period average measurement. High resolution period measurements can also be made by taking the reciprocal of a frequency measurement.



KEYBOARD

(1) ARITHMETIC
FUNCTION: 1/X

FRONT PANEL

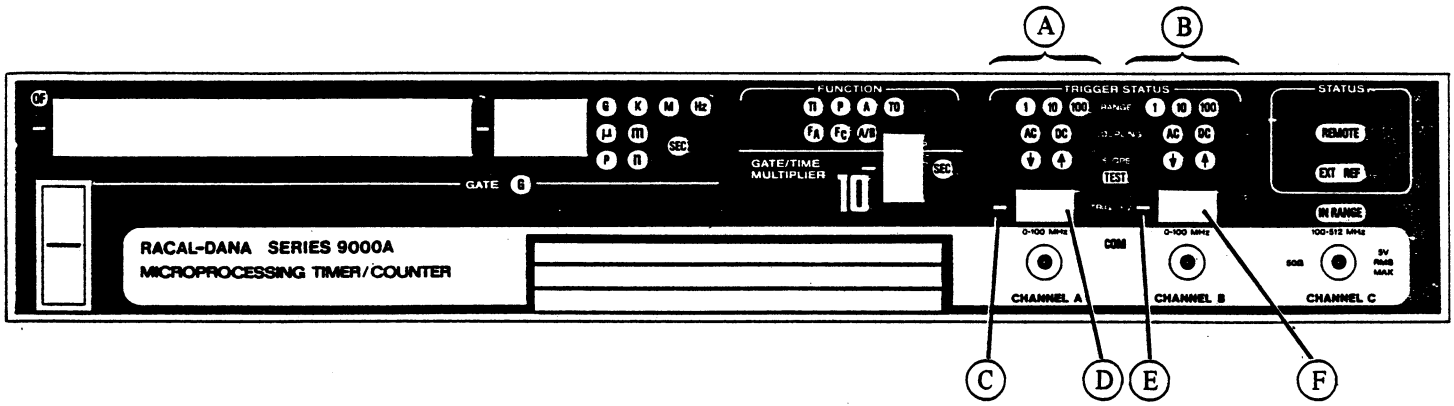
(A) Display: Dependent on input
(B) Display Units: Dependent on input

EXAMPLE

The frequency of a 5 kHz signal is desired. Measure the period (P) of a 5 kHz signal at a resolution of 10 ns (see table 2.6).

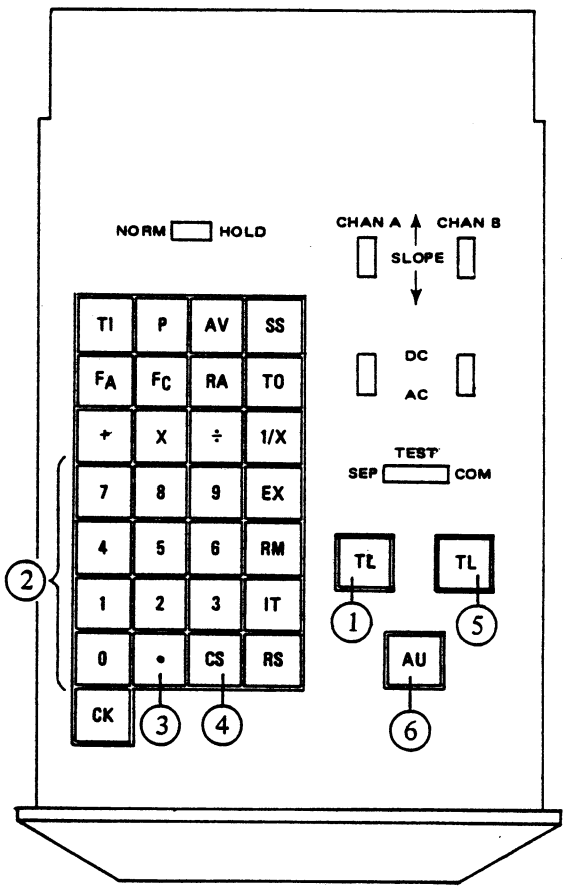
1. 1/X
   (A) 5.0000
   (B) kHz

Table 2.15 - Trigger Level



TRIGGER LEVEL

Both the channel A and channel B signal conditioning circuits contain a nine bit DAC, capable of providing stable trigger levels from –3.00V to +3.00V in 12.5 millivolt steps. Range attenuators in each circuit also permits trigger level settings from +30.0V to –30.0V and from +300V to –300V. The level of each channel is set individually, either manually or automatically. The numeric value of the trigger settings is displayed in volts on the instrument front panel. The range of the trigger level is determined by the placement of the decimal in manual range and automatically computed in auto range. In manual selection, inputs greater than the allowable for each range span are rejected.



KEYBOARD

(1)	TRIGGER LEVEL:	Selects Trigger Level A
(2)	TRIGGER LEVEL VALUE:	3-digit Trigger Level value for manual selection
(3)	DECIMAL:	Selects TL range in manual selection
(4)	CHANGE SIGN:	Selects TL polarity
(5)	TRIGGER LEVEL:	Selects Trigger Level B
(6)	AUTO:	Automatically selects Trigger Level and Range

FRONT PANEL

(A)	Range:	Indicates channel A range
(B)	Range:	Indicates channel B range
(C)	Polarity:	Indicates channel A TL polarity
(D)	Trigger Level:	3-digit display of channel A TL
(E)	Polarity:	Indicates channel B TL polarity
(F)	Trigger Level:	3-digit display of channel B TL

Table 2.15 - Trigger Level continued

MANUAL OPERATION		ACTION
1.	Depress TL of desired channel	μP is signaled and trigger display is blanked.
2.	Enter TL value	DAC is programmed and value displayed
3.	Depress TL of desired channel	Value is set and μP is released from TL entry operation

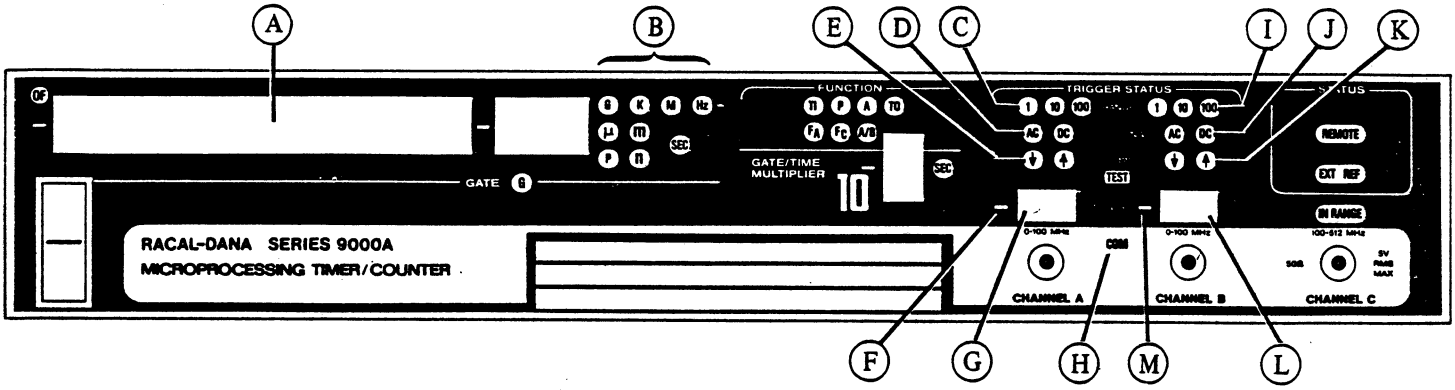
AUTO OPERATION		ACTION
1.	Depress TL of desired channel	μP is signaled and trigger display is blanked.
2.	Depress AUTO	μP measures the p-p value of the input signal, computes the 50% point of the waveform and programs the DAC to the 50% level. Level is set and displayed on the front panel readout. The μP is then released from the TL entry operation

EXAMPLE

The channel A and channel B trigger levels are to be set to accommodate a 1V square wave for TIA measurement.

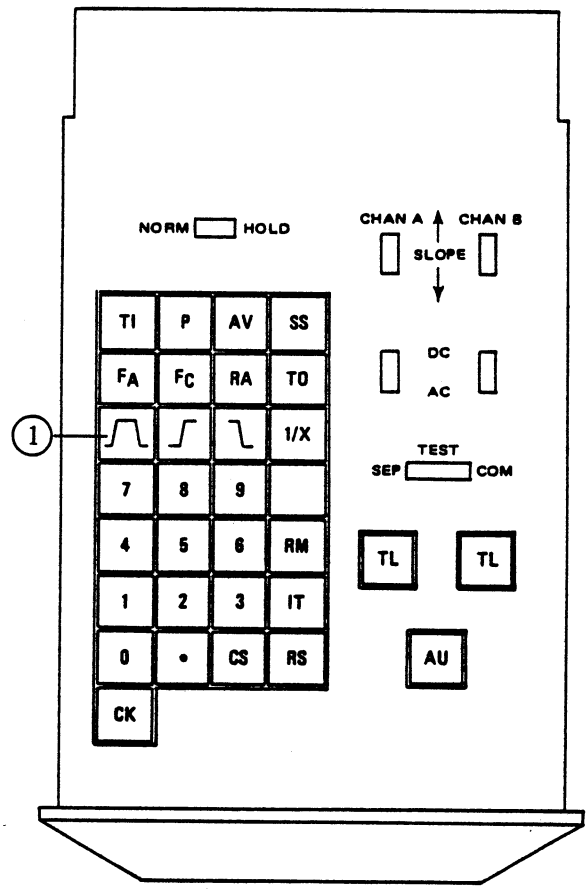
(1)	TL of channel A	(A)	1
(2)	0	(B)	1
(3)	.	(C)	Blank
(2)	11	(D)	0.11
(1)	TL of channel A	(E)	–
(5)	TL of channel B	(F)	0.51
(4)	CS		
(2)	0		
(3)	.		
(2)	51		
(5)	TL of channel B		

Table 2.16 - Pulse Width (-11A Models Only)



PULSE WIDTH

This operation, selected with the ⎍ key on the keyboard, allows the user to automatically take pulse width measurements in the Time Interval and Time Interval Average modes. The selection of the pulse width key automatically selects DC coupling on both channels, common, + slope on channel A, – slope, on channel B. It measures the minimum and maximum peak values of the input signal, sets the proper trigger levels for both channels at the 50% points of the waveform and displays the time interval of the positive portion of the input signal on the display.



KEYBOARD

(1) PULSE WIDTH: ⎍

FRONT PANEL

(A)	Display:	Value of input pulse width
(B)	Display Scale:	Dependent on input
(C)	Channel A Range:	Dependent on input
(D)	Channel A Coupling:	DC
(E)	Channel A Slope:	↑
(F)	Channel A TL Polarity:	Dependent on input
(G)	Channel A TL Value:	Dependent on input
(H)	COM:	COM
(I)	Channel B Range:	Dependent on input
(J)	Channel B Coupling:	DC
(K)	Channel B Slope:	↓
(L)	Channel B TL Polarity:	Dependent on input
(M)	Channel B TL Value:	Dependent on input

OPERATION	ACTION
1. Select ⎍ key (TI or TIA only)	All trigger status controls are automatically set to measure the positive portion of an input pulse at the 50% level

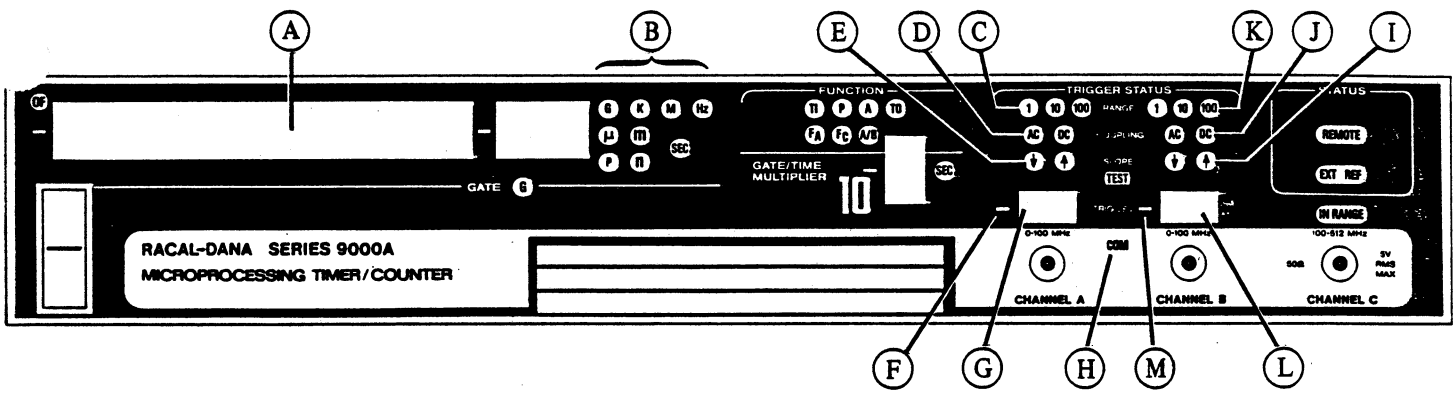
EXAMPLE

The pulse width of a 1 kHz 1V square wave is to be measured. Select TIA at 10^2.

(1) ⎍

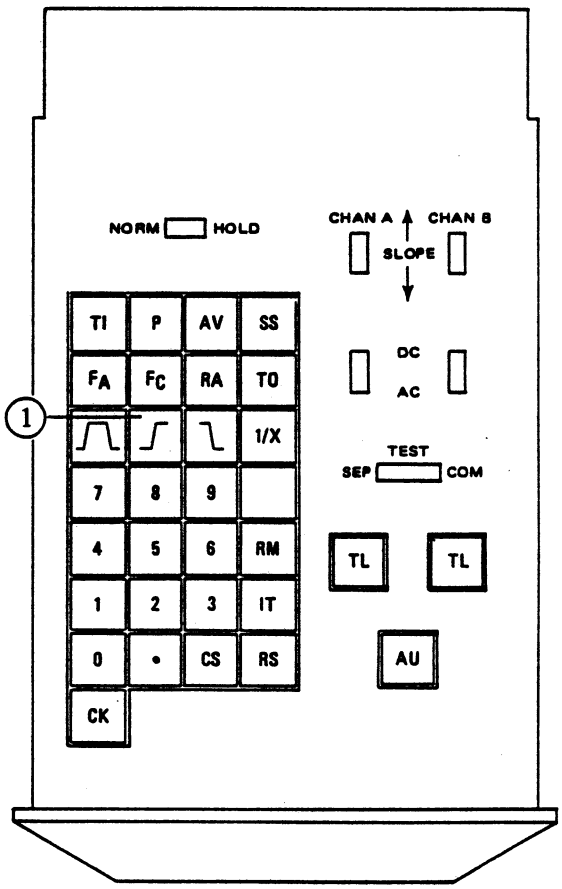
(A)	501.2955	(H)	COM
(B)	μsec	(I)	1
(C)	1	(J)	DC
(D)	DC	(K)	↓
(E)	↑	(L)	0.49
(F)	Blank	(M)	Blank
(G)	0.49		

Table 2.17 - Rise Time (-11A Models Only)



RISE TIME

This operation, selected with the ⎍ key on the keyboard, provides automatic rise time measurements in the Time Interval and Time Interval Average modes. The selection of the rise time key selects DC coupling and + slope on both channels and common. It measures the minimum and maximum peak values of the input signal and, from these values, sets the channel A trigger to the 10% level and channel B trigger to the 90% level. The interval between channels A and B is measured and appears in the display. Since the trigger level settings are calculated from the absolute peaks of the signal, overshoot and undershoot will affect the measurement.



KEYBOARD

(1) RISE TIME: ⎍

FRONT PANEL

(A)	Display:	Dependent on input
(B)	Display Scale:	Dependent on input
(C)	Channel A Range:	Dependent on input
(D)	Channel A Coupling:	DC
(E)	Channel A Slope:	↑
(F)	Channel A TL Polarity:	Dependent on input
(G)	Channel A TL Value:	Dependent on input
(H)	COM:	COM
(I)	Channel B Range:	Dependent on input
(J)	Channel B Coupling:	DC
(K)	Channel B Slope:	↑
(L)	Channel B TL Value:	Dependent on input
(M)	Channel B TL Polarity:	Dependent on input

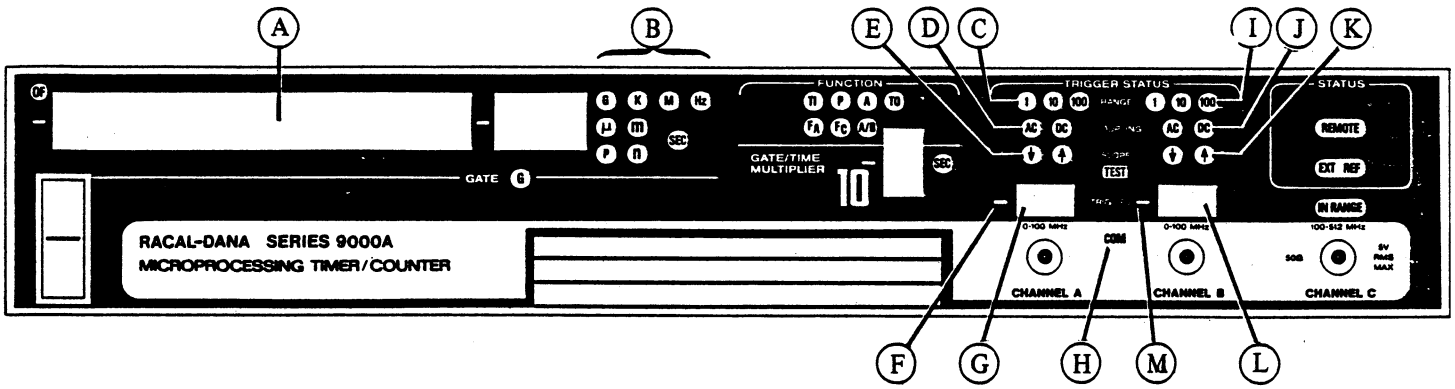
EXAMPLE

The rise time of a 1V, 1 kHz square wave is to be measured. Select TIA to 10^3.

(1) ⎍

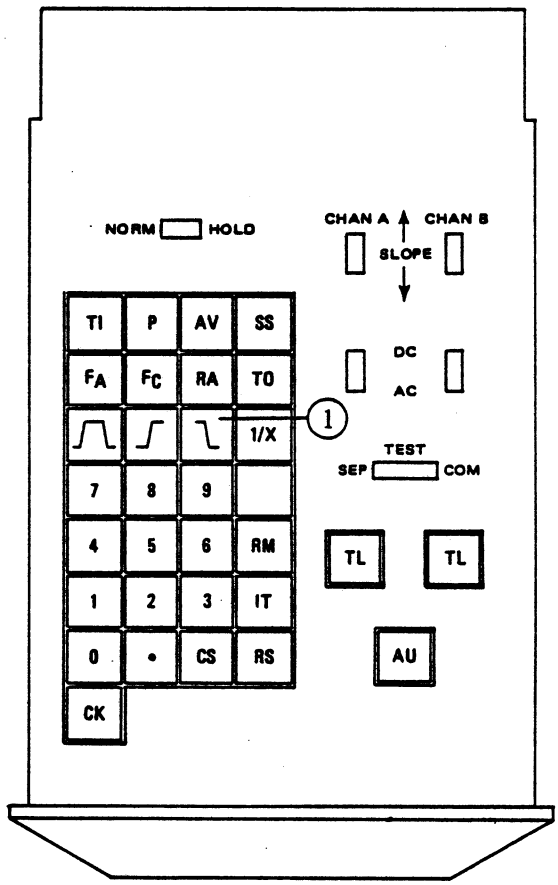
(A)	507.10	(H)	COM
(B)	nsec	(I)	1
(C)	1	(J)	DC
(D)	DC	(K)	↑
(E)	↑	(L)	0.86
(F)	Blank	(M)	Blank
(G)	0.10		

Table 2.18 - Fall Time (-11A Models Only)



FALL TIME

This operation, selected with the ⎣ key on the keyboard, provides automatic fall time measurements in the Time Interval and Time Interval Average modes. The selection of the fall time key selects DC coupling and – slope on both channels and common. It measures the minimum and maximum peak values of the input signal and, from this value, sets the channel A trigger to the 90% level and channel B trigger to the 10% level. The interval between channels A and B is measured and appears in the display. Since the trigger level settings are calculated from the absolute peaks of the signal, overshoot and undershoot will affect the measurement.



KEYBOARD

(1) FALL TIME: ⎣

FRONT PANEL

(A)	Display:	Dependent on input
(B)	Display Scale:	Dependent on input
(C)	Channel A Range:	Dependent on input
(D)	Channel A Coupling:	DC
(E)	Channel A Slope:	↓
(F)	Channel A TL Polarity:	Dependent on input
(G)	Channel A TL Value:	Dependent on input
(H)	COM:	COM
(I)	Channel B Range:	Dependent on input
(J)	Channel B Coupling:	DC
(K)	Channel B Slope:	↓
(L)	Channel B TL Value	Dependent on input
(M)	Channel B TL Polarity:	Dependent on input

EXAMPLE

The fall time of a 1V, 1 kHz square wave is to be measured. Select TIA to 10^3.

(1) ⎣

(A)	1.61710	(H)	COM
(B)	nsec	(I)	1
(C)	1	(J)	DC
(D)	DC	(K)	↓
(E)	↓	(L)	0.10
(F)	Blank	(M)	Blank
(G)	0.89		

2.13 EXTERNAL GATE CONTROL

2.13.1 The External Gate Control features of the Series 9000A Counter enables the user to control the counters measurement gate so that the measurement window can be focused on a time-discrete portion of the input signal. Thus the counter can measure the parameters of a selected portion of a composite or complex wavetrain. The gate delay function operates in three modes: (1) the NORMAL or gate delay mode, (2) Selective Gate Control mode and (3) the Synchronous Window Control Mode. The mode is selected by setting a rear panel switch to the desired mode position. The gate signal is applied to the counter through an input connector which is also located on the rear panel of the counter. A view of the rear panel illustrating the gate delay mode switch and gate delay input connector is shown in Figure 2.6. The switch settings and modes are shown in Table 2.19. A description of the counter function in each of these modes is presented in the following paragraphs along with examples of applications for each mode.

13.2 Normal Mode.

2.13.2.1 This mode of operation is more descriptively referred to as the gate close delay mode. When the mode switch is set to the NORM position a high level signal at the gate delay input prevents the counter gate from closing. For example, assume that the input signal is fed to both channels A and B (common channel mode) and that the rising edge of the signal at channel A opens the gate and the falling edge at channel B closes the gate (A ↑ B ↓). Without a gate delay signal the counter gate will open on the rising edge of the input signal and close on the falling edge. When a gate delay signal is applied to the counter the measurement gate is forced to remain open even though the input signal falls. Thus the user can hold the measurement gate

Table 2.19 - Mode Switch Operation

Position	Switch Marking	Mode
Up	A B	Selective Gate Control
Center	NORM	Gate Delay
Down	A & B	Synchronous Window Control

open for any length of time desired. The timing relationships of the input signal, gate delay and measurement gate for a typical application are illustrated in Figure 2.7.

2.13.3 Selective Gate Control Mode.

2.13.3.1 This mode is designed to give the user absolute control over both the opening and closing of the measurement gate. Simply stated the measurement gate cannot open on the transition of the input signal unless the gate delay signal is high and once opened the measurement gate cannot close until after the gate delay signal goes low. This means the user can define the timing and period of the measurement gate with the gate delay signal. Typical timing relationships are shown in Figure 2.8. Note that the measurement gate opening and closing is *controlled* by the input signal and *conditioned* by the gate delay signal.

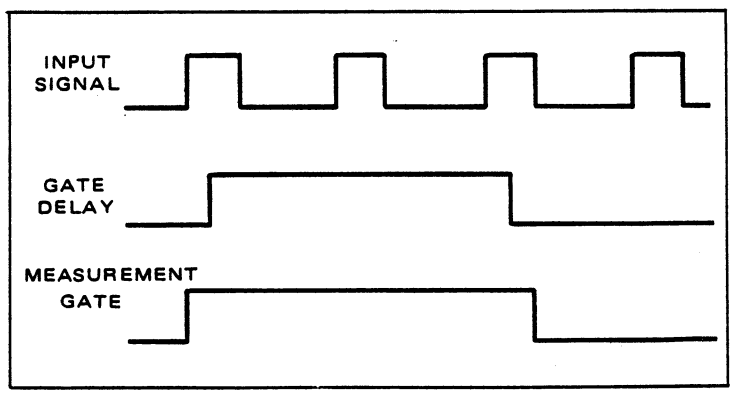


Figure 2.7 - Normal Mode Measurement Gate Timing

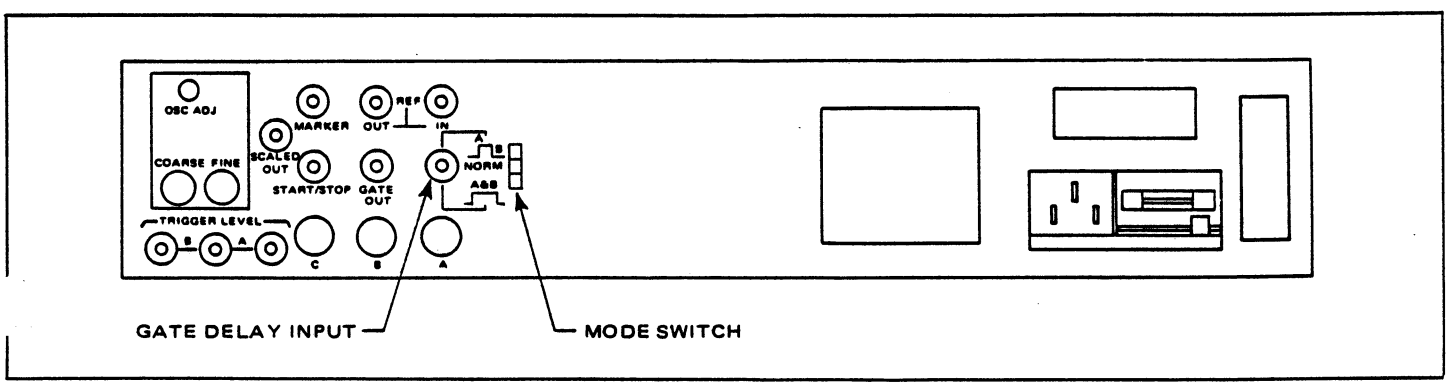


Figure 2.6 - Gate Delay Input Connector and Mode Switch

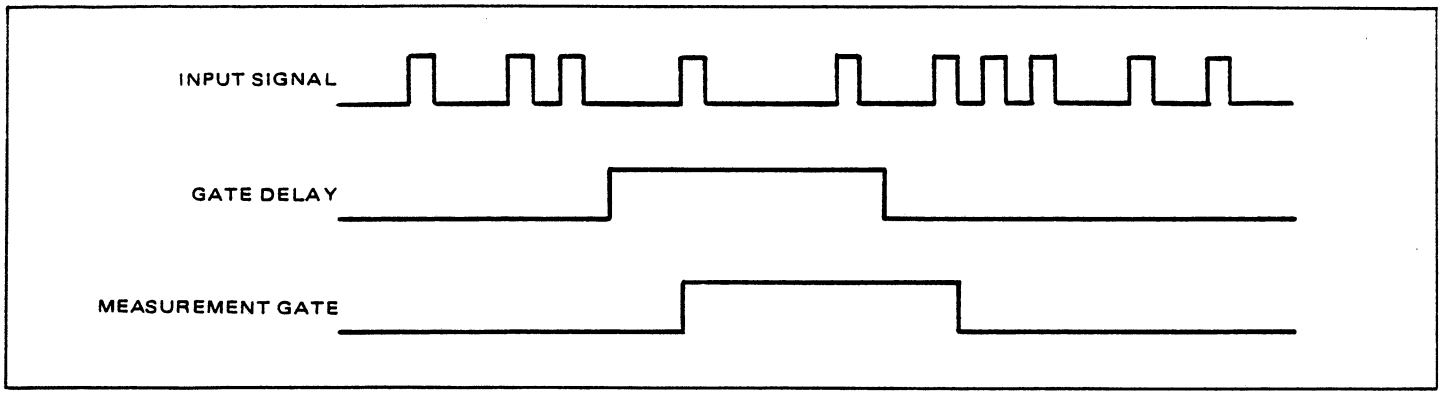


Figure 2.8 - Selective Gate Control Mode Timing

2.13.4 Synchronous Window Control.

2.13.4.1 In order to select a discrete pulse or group of pulses out of a wavetrain for measurement it is necessary to be able to synchronize the measurement gate with the pulse to be measured. The Synchronous Window Control mode provides this capability. In addition, it enables the user to use the auto trigger and pulse parameter features of the Series 9000A Counter when measuring a selected pulse. In this mode the measurement gate will not open until the gate delay control signal is true. When the gate delay is enabled the measurement gate will open and close under control of the measurement signal as shown in Figures 2.9 and 2.10. Figure 2.9 illustrates a gate delay encompassing a single pulse while Figure 2.10 shows the gate delay set to pulses. The counter can be controlled in this mode to select any number of pulses. Note that each time the gate closes a measurement is made. This mode is used only with the Time Interval Average function. The amplitude of the gate delay input signal must be at least +1 volt and no greater than +5 volts.

2.13.5 Programmable Arming Modes (Option 06PA).

2.13.5.1 This option allows programming of normal operation, synchronous window mode or selective gate mode through the GPIB option. It also provides 1 Megohm or 50 ohm input impedance on channels A or B.

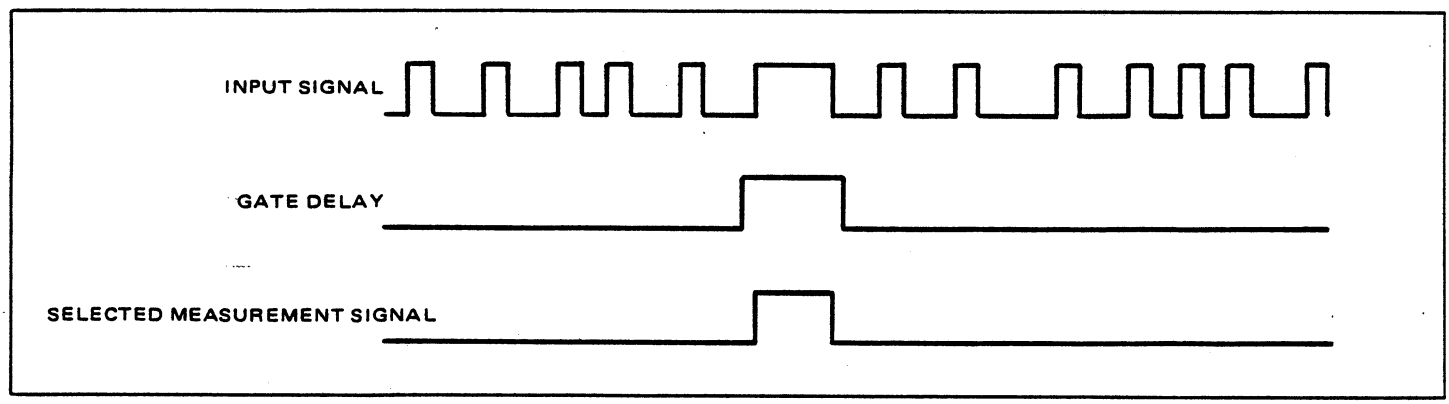


Figure 2.9 - Synchronous Window Control Mode, Single Pulse Window

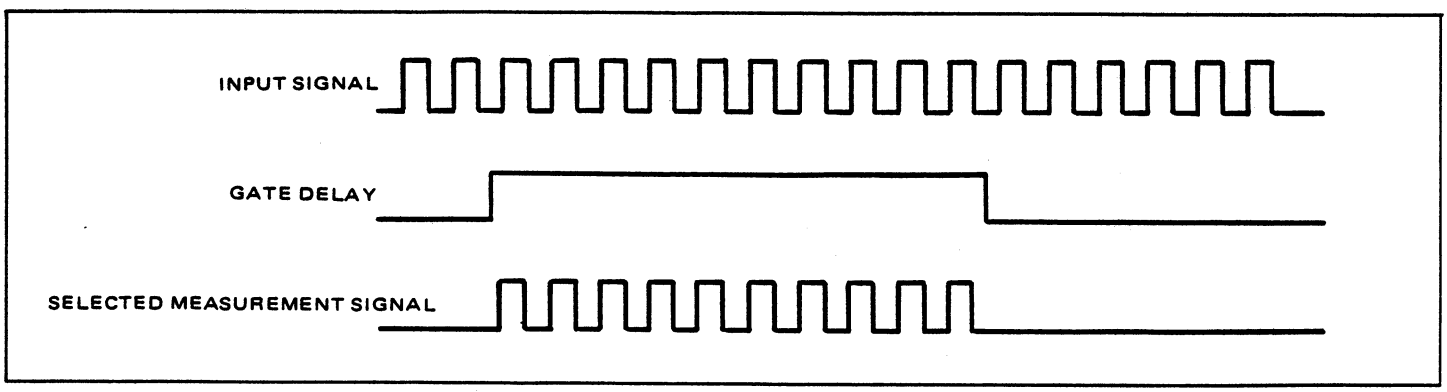


Figure 2.10 - Synchronous Window Control, Multiple Pulse Window

SECTION 3 SYSTEMS INTERFACE

3.1 GENERAL.

3.1.1 This section covers the operation and provides hookup information for the Option 55 and Option 56.

3.2 OPTION 55 GENERAL PURPOSE INTERFACE BUS.

3.2.1 The Interface Board provides remote programming of all controls and digital output data defining all front panel indicators. Inputs and outputs for the option are on a bi-directional bus via a 24 pin connector on the rear panel. The pin location, line identification, and operation of the option are in compliance with IEEE standard 488-1978, "IEEE STANDARD DIGITAL INTERFACE FOR PROGRAMMABLE INSTRUMENTATION". The Interface Board provides interface capability with other instruments and a controller also utilizing the "interface bus" structure as shown in Figure 3.1. Connector contact signal assignments are shown in Table 3.1. The IEEE-STD-488-1978 subsets available in the 9000A are listed in Table 3.2.

Table 3.1 - Connector Contact Assignments

Contact	Signal Line	Contact	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd, (6)
7	NRFD	19	Gnd, (7)
8	NDAC	20	Gnd, (8)
9	IFC	21	Gnd, (9)
10	SRQ	22	Gnd, (10)
11	ATN	23	Gnd, (11)
12	SHIELD	24	Gnd, LOGIC

NOTE: Gnd (n) refers to the signal ground return of the referenced contact.

Table 3.2 - IEEE-STD-488-1978 Standard Interface Subset Capability

Subset Mnemonic	Function	Capability
SH1	Source Handshake	Complete
AH1	Acceptor Handshake	Complete
T5	Talker	Complete
TE0	Extended Talker	None
L4	Listener	All except listen only
LE0	Extended Listener	None
SR1	Service Request	Complete
RL1	Remote/Local	Complete
PP0	Parallel Poll	None
DC1	Device Clear	Complete
DT1	Device Trigger	Complete
C0	Controller	None

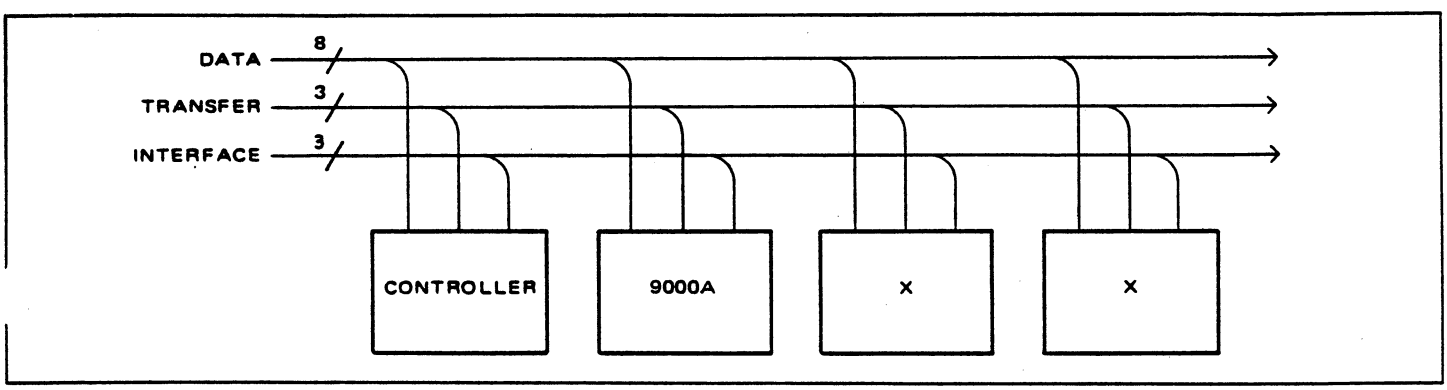


Figure 3.1 - Series 9000A - GPIB System Relationship

3.2.2 By assigning an available address to the 9000A, it can be "called up" by the controller or another device on the bus without interfering with any other unit on the bus. Switches located on the rear panel of the 9000A permit the programming of the instrument address. The coding used for the address on the option board is ASCII (hexadecimal). Any one of 31 codes can be used for the address of an instrument; a total of 15 is the maximum number of devices that can be used on one bus. Address assignment instructions are presented in paragraph 3.2.5.

> **NOTE**
> System errors may result if AC power is removed from a 9000A that is connected to the GPIB.

3.2.3 Bus Description.

3.2.3.1 The relationship of the 9000A to the GPIB is shown in Figure 3.1. Of the twenty-four lines available at the connector (shown in Table 3.1) seven are grounds, one is a shield, and the remaining 16 lines are the data bus lines. All of the data bus lines are either input or output lines and have the following characteristics:

Logic Levels:	1 = Low = $\leq$ .8V; 0 = Hi = $\geq$ 2.0V
Input Loading:	Each input = one TTL load
Output:	The output is capable of driving 15 interface bus loads. It consists of an open collector driver and is capable of sinking 48 mA at:<0.5 volts. See IEEE 488 Electrical Specifications.

3.2.3.2 The data bus lines as shown in Figure 3.1 consists of three functionally separate sets: Data, Handshake and Interface. The distribution and connector assignment of these lines is shown in Table 3.3.

3.2.3.3 *Data.* The data lines consist of lines DIO-1 through DIO-8. These lines are the lines over which data flows between all instruments on the bus in bit parallel, byte serial form.

3.2.3.4 *Handshake.* The transfer lines consist of: DAV (data valid), NDAC (not data accepted), and NRFD (not ready for data). These lines provide communication between the instrument that is talking and the instruments that are listening to synchronize the flow of information across the eight data lines. These lines derive their nomenclature from their meaning in the low or one state, e.g., when NRFD is low the device is Not Ready For Data.

a. DAV. Signifies that valid information is available on the data lines.

b. NRFD. Signifies instrument ready to accept information.

c. NDAC. Signifies information is accepted by the acceptor.

3.2.3.5 *Interface.* The five interface lines coordinate the flow of information on the bus.

a. IFC. Places the 9000A in the IDLE state (Untalk, Unlisten).

Table 3.3 - Distribution and Assignment of Interface Signal Lines

PIN		
1	DIO-1	DATA LINES ARE USED TO TRANSFER DATA FROM ONE INSTRUMENT TO ANOTHER
2	DIO-2	
3	DIO-3	
4	DIO-4	
13	DIO-5	
14	DIO-6	
15	DIO-7	
16	DIO-8 †	
6	DAV (DATA VALID)	HANDSHAKE LINES OPERATE IN A PROPER TIME SEQUENCE FOR COMPLETE COMMUNICATION BETWEEN INSTRUMENTS
7	NRFD (NOT READY FOR DATA)	
8	NDAC (NOT DATA ACCEPTED)	
5	EOI †	INTERFACE LINES ARE USED TO PROVIDE AN ORDERLY FLOW OF INFORMATION BETWEEN UNITS
9	IFC (INTERFACE CLEAR)	
10	SRQ	
11	ATN (ATTENTION)	
17	REN (REMOTE ENABLE)	

†NOT USED WITH 9000A AND OPTION 55

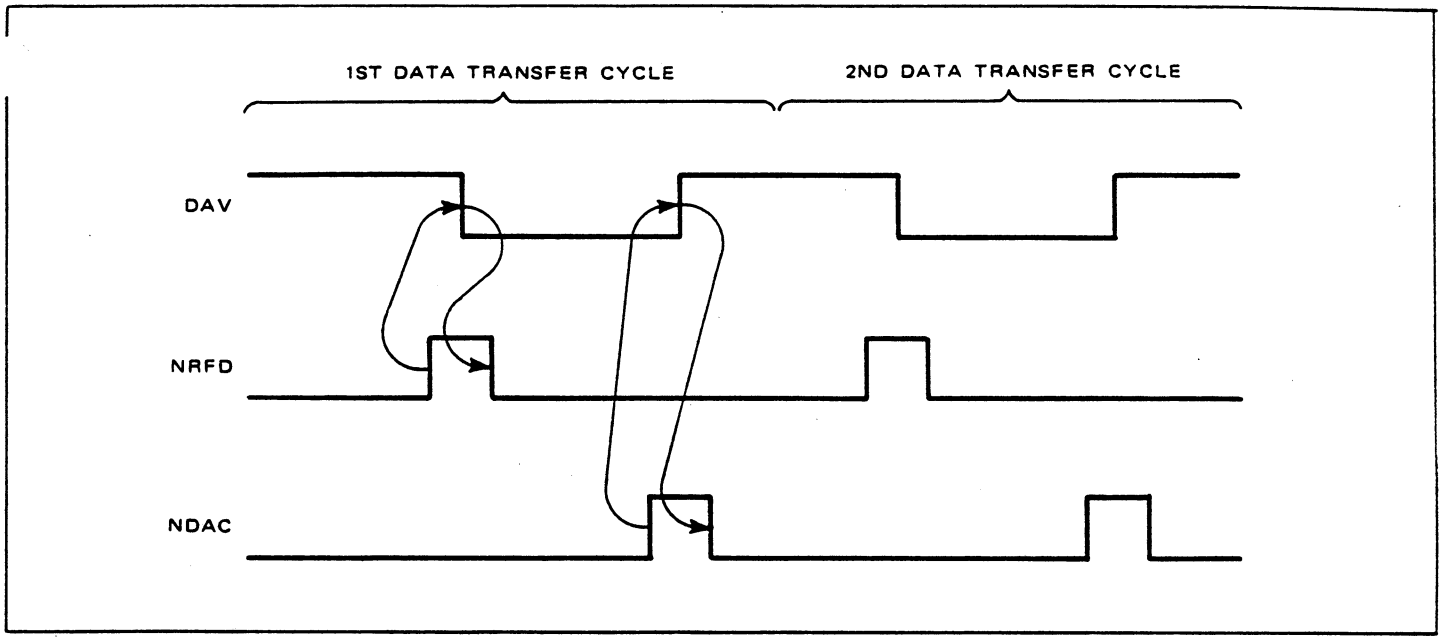


Figure 3.2 - Handshake Sequence

b. ATN. Indicates the nature of information on data lines during a handshake transfer sequence. Low indicates data lines carry interface commands; high indicates that the data lines carry data.

c. REN. Arms instrument to select Remote operation, when addressed as a listener. (Low for Remote.)

d. SRQ. Service request signal line that signals the controller that a peripheral or bus member wants attention for such purposes as transmitting measurement, status or condition information to the bus controller.

e. EOI. End or Identify signal. Used for two purposes: (1) to signify the end of a message and (2) to signal bus peripherals to set the I/O bit assigned for parallel poll identification process. This signal is not used in the Series 9000A.

3.2.4 Handshake.

3.2.4.1 The handshake is the process by which each data byte is transferred from the source to the acceptor.

3.2.4.2 Shown in Figure 3.2 is the sequential relationship between the DAV, NRFD, and NDAC lines, used to transfer data bytes. Figure 3.3 illustrates the handshake flow chart. The handshake sequence is illustrated and described in further detail in a subsequent subsection entitled *Bus Operation Sequence.*

3.2.5 Address Assignment.

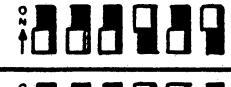
3.2.5.1 The 9000A Counter/Timer, when used as a system instrument, must be assigned an address as a bus member. The instrument is equipped with an address switch located on the rear panel which enables the user to assign it one of 31 decimal addresses. The decimal addresses available are the numbers 00 through 31.

3.2.5.2 Table 3.4 contains all of the information required for setting the instruments address and determining the talk and listen address codes for use in programming the controller. The use of this information is described in the following paragraphs.

3.2.5.3 Refer to Table 3.4 and note that the top line shows the decimal addresses available for assignment to the 9000A. The segment titled "Address Switch Setting" illustrates the positions of the switches for each decimal address. To set the address on the instrument select the desired decimal address, refer to Table 3.4, and set the switches on the address switch to the pattern shown in the "address switch" column of the table.

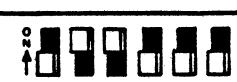
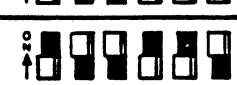
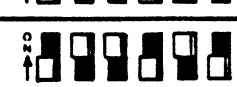
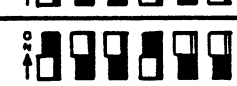
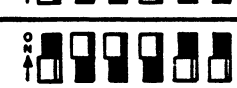
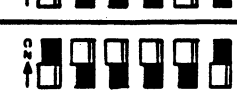
3.2.5.4 Once the instrument has been assigned an address and the address switch has been set, the controller may address the instrument as a talker or as a listener by transmitting the appropriate ASCII character on the data lines. The "Data Lines" portion of Table 3.4 shows the 7 bit binary code required for each talk and listen address assigned to the instrument. These are the codes the controller must transmit to establish the talker-listener condition of the counter. Note that there are 2 address codes

Table 3.4 - Series 9000A GPIB Address Assignment

ASCII CHARACTERS		DATA LINES							ADDRESS SWITCH SETTING	DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	** TALK ONLY / A5 A4 A3 A2 A1	
TALK	LISTEN	TALK	LISTEN	ADDRESS						
				16	8	4	2	1		
	SP	0	1	0	0	0	0	0		00
@		1	0	0	0	0	0	0		
	!	0	1	0	0	0	0	1		01
A		1	0	0	0	0	0	1		
	"	0	1	0	0	0	1	0		02
B		1	0	0	0	0	1	0		
	#	0	1	0	0	0	1	1		03
C		1	0	0	0	0	1	1		
	$	0	1	0	0	1	0	0		04
D		1	0	0	0	1	0	0		
	%	0	1	0	0	1	0	1		05
E		1	0	0	0	1	0	1		
	&	0	1	0	0	1	1	0		06
F		1	0	0	0	1	1	0		
	' (APOSTROPHE)	0	1	0	0	1	1	1		07
G		1	0	0	0	1	1	1		
	(	0	1	0	1	0	0	0		08
H		1	0	0	1	0	0	0		
	)	0	1	0	1	0	0	1		09
I		1	0	0	1	0	0	1		
	*	0	1	0	1	0	1	0		10
J		1	0	0	1	0	1	0		
	+	0	1	0	1	0	1	1		11
K		1	0	0	1	0	1	1		
	,	0	1	0	1	1	0	0		12
L		1	0	0	1	1	0	0		
	-	0	1	0	1	1	0	1		13
M		1	0	0	1	1	0	1		
	.	0	1	0	1	1	1	0		14
N		1	0	0	1	1	1	0		
	/	0	1	0	1	1	1	1		15
O		1	0	0	1	1	1	1		

**The "Talk Only" switch is set to "ON" when used with a printer or other "listen only." device.

Table 3.4 - Series 9000A GPIB Address Assignment continued

ASCII CHARACTERS		DATA LINES							ADDRESS SWITCH SETTING	DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	** TALK ONLY 1 / 0; A5 A4 A3 A2 A1	
TALK	LISTEN	TALK	LISTEN	ADDRESS						
				16	8	4	2	1		
	Ø	0	1	1	0	0	0	0		16
P		1	0	1	0	0	0	0		
	1	0	1	1	0	0	0	1		17
Q		1	0	1	0	0	0	1		
	2	0	1	1	0	0	1	0		18
R		1	0	1	0	0	1	0		
	3	0	1	1	0	0	1	1		19
S		1	0	1	0	0	1	1		
	4	0	1	1	0	1	0	0		20
T		1	0	1	0	1	0	0		
	5	0	1	1	0	1	0	1		21
U		1	0	1	0	1	0	1		
	6	0	1	1	0	1	1	0		22
V		1	0	1	0	1	1	0		
	7	0	1	1	0	1	1	1		23
W		1	0	1	0	1	1	1		
	8	0	1	1	1	0	0	0		24
X		1	0	1	1	0	0	0		
	9	0	1	1	1	0	0	1		25
Y		1	0	1	1	0	0	1		
	:	0	1	1	1	0	1	0		26
Z		1	0	1	1	0	1	0		
	;	0	1	1	1	0	1	1		27
[		1	0	1	1	0	1	1		
	<	0	1	1	1	1	0	0		28
\		1	0	1	1	1	0	0		
	=	0	1	1	1	1	0	1		29
]		1	0	1	1	1	0	1		
	>	0	1	1	1	1	1	0		30
^		1	0	1	1	1	1	0		
NONE		ILLEGAL							NONE	31

**The "Talk Only" switch is set to "ON" when used with a printer or other "listen only" device.

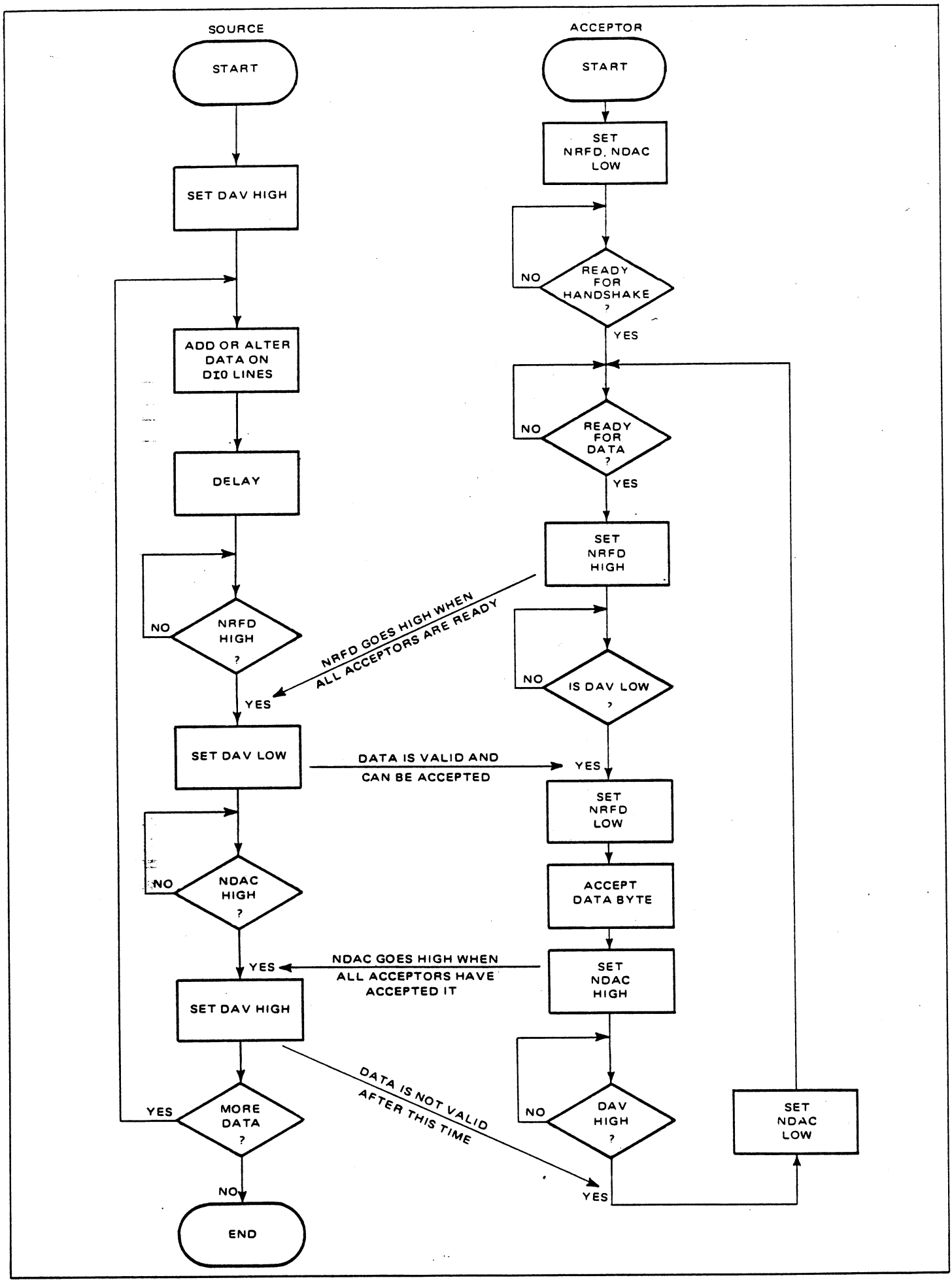


Figure 3.3 - Handshake Flow Chart

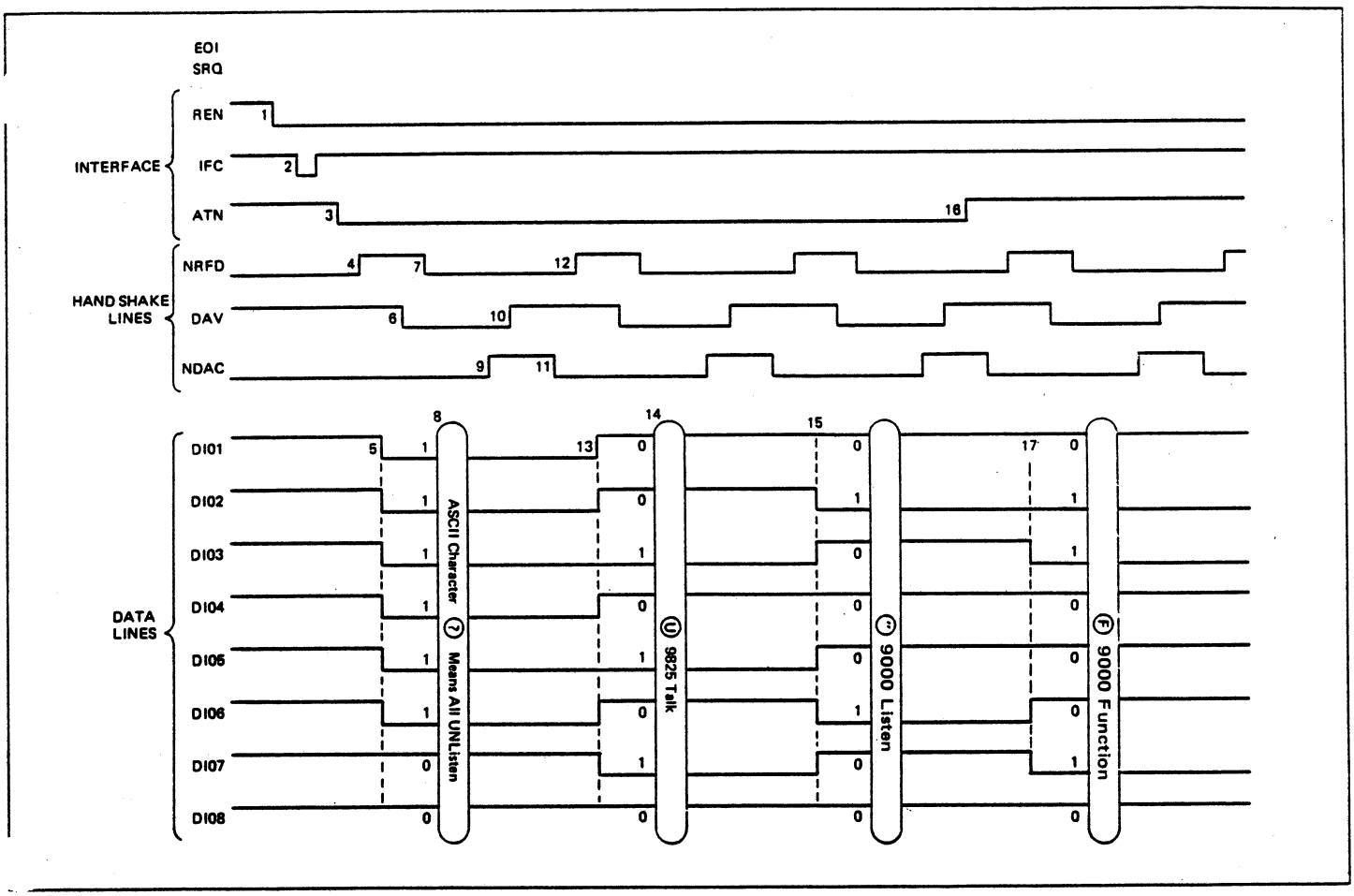


Figure 3.4 - Handshake Timing

used for each decimal address. Each of these address codes constitutes a different ASCII character. For example, if it is desired to use the decimal address 02 the address switch on the rear panel of the instrument is set to the pattern shown in Table 3.4 and as shown in the table, the talk address is the ASCII character B and the listen address is the ASCII character ". Note that the only difference in the binary code in each case is the state of data lines D6 and D7.

3.2.5.5 Table 3.4 illustrates the data line code in binary form for each decimal address. Again using the example for decimal address 02 note that bits D1 through D5 are the same for both talk and listen address and that the only difference is in bits D6 and D7.

3.2.6 Bus Operation Sequence.

3.2.6.1 The transmission of programming instructions to 9000A and the subsequent transmission of measurement data to the controller is accomplished by transmitting programming instructions as outlined in the bus operation sequence in Table 3.5. Table 3.5 and the accompanying timing chart (Figure 3.4) illustrates the sequence of the transmission of device dependent messages to the counter to cause it to measure the frequency of a measurement signal applied to channel A and transmit the resultant measurement data to the controller by the interface bus.

3.2.6.2 Note that the left hand column of the table contains line numbers. These are used for reference purposes throughout the following description of the bus operation sequence. The column titled "Handshake Lines" indicates the high/low condition of the handshake lines at various points throughout the two-way transmission of information over the bus. In a similar fashion the columns titled "Interface Lines" and "Data Lines" contain entries reflecting the state of the interface lines and data lines during operation. The column titled "Meaning or Function" contains entries explaining the purpose of each operational step during the data transfer.

3.2.6.3 A timing chart (Figure 3.4) is included to illustrate the condition of each individual bus line at each stage of the data transfer operation. Note that the timing chart includes numbers adjacent to each level change; these numbers refer to the individual line entries of the table. The

Table 3.5 - Bus Operation Sequence

	HANDSHAKE LINES	INTERFACE LINES	DATA LINES	MEANING OR FUNCTION
1		REN Lo		Puts the 9000A into the remote mode.
2		IFC		Stops activity on the bus.
3		ATN Lo		Signifies that data byte will be a "Bus Message".
4	NRFD Hi			Counter says ready for data.
5			?	UNL (Unlisten) message (ASCII character ?) on data bus by controller means "all bus peripherals unlisten".
6	DAV Lo			Controller says data is now valid.
7	NRFD Lo			Counter says its not ready for new data; do not change data lines while counter is accepting data.
8				Counter reads data lines.
9	NDAC Hi			Counter says it has read data.
10	DAV Hi		?	Controller says data no longer valid.
11	NDAC Lo			Counter removes data accepted flag.
12	NRFD Hi			Counter says it's ready for next data byte.
13				Controller removes or changes data on bus.
14			U	"I talk" controller becomes talker (controller talker address).
15			"	"You listen", addressed peripheral becomes listener (In this case it is the 9000A Counter set to decimal address 02; see table 3.4).
16		ATN Hi		Signifies that data byte will be a "Device Dependent Message" as opposed to a "Bus Message".
17			F	Function
18			0	Frequency A
19			G	Exponent
20			–	Exponent sign negative
21			1	1 (10 Hz resolution)
22			A	Channel A Slope and Coupling
23			+	Positive Slope
24			D	DC coupled
25			C	Configuration
26			0	Separate channels
27			L	Level of triggering
28			A	Channel A
29			A	Automatic
30			CR	End of transmission by controller. This is ignored by the 9000A Counter.
31			LF	
32		ATN Lo		Byte to follow is a Bus Message.
33			?	UNL (unlisten) bus message.
34			B	"You talk", 9000A talk address (Decimal Address 02).

Table 3.5 - Bus Operation Sequence continued

	HANDSHAKE LINES	INTERFACE LINES	DATE LINES	MEANING OR FUNCTION
35			5	"I listen", HP9825 listen address.
36		ATN Hi		Message to be transmitted by counter is Data.
37			+	Measurement data transmitted by counter.
38			.	
39			2	
40			7	
41			1	
42			3	
43			5	
44			3	
45			4	
46			E	Exponent Indicator means X 10^N
47			+	Sign of exponent.
48			0	Exponent. Here it indicates 10^8.
49			8	
50			CR	End of 9000A data message.
51			LF	

command programming and subsequent data transfer operation are described in the following paragraphs.

3.2.6.4 The measurement operation used for the example of bus operation in Table 3.5 is a simple frequency measurement using channel A of the 9000A Counter. The measurement parameters are as follows: Function: Frequency A; resolution: 5(or 10 hertz), channel A coupling: DC, input configuration: Separate, channel A triggering: Automatic. Note that lines 17 through 27 of the table contain the Device Dependent Messages required to program the instrument for this operation and that the program string is F0G–1A+DC0LAA (alpha characters may be upper or lower case).

3.2.6.5 For purposes of this example, it is assumed that the Series 9000A has been assigned the decimal address 02 and that the controller is a Hewlett-Packard 9825 calculator with the talk address U. It is further assumed that both the controller and the counter are a system connected, turned on and operational.

3.2.6.6 Table 3.5 shows the sequence of bus operation. Lines 1 through 13 show the detailed operation of the bus for one handshake cycle; the transmission of one ASCII character as a bus message. Lines 14 through 50 do not indicate the detail of each handshake cycle. They indicate only the transmission of the characters required for the programming commands and the subsequent transmission of the data by the counter. Each transmission by the controller or the counter shown in lines 14 through 50 requires the handshake cycle illustrated by the line entries 1 through 13 of the table.

3.2.6.7 Refer to Table 3.5, line 1, and note that the first operation performed is the setting of the Remote Enable (REN) line to the low state. As explained in the table, this operation arms the 9000A Counter to go into remote mode (as soon as its listen address is received). The controller then transmits the interface clear (IFC) signal which stops bus activity and the attention (ATN) line is set low indicating that the next data byte placed on the bus by the controller will be a Bus Message. Note in the timing chart that when the ATN line is set low (3) that the counter responds by setting the NRFD line high (4). This response by the counter indicates that it is now ready to accept data.

3.2.6.8 When the counter transmits the ready for data signal by setting the NRFD line high (line 4 of Table 3.5) the controller puts the bus message UNL on the data lines. As shown in line 5 of the table this is the ASCII character ?.

The unlisten message is a universal message understood by all bus members as the command "unlisten". Having placed the data character on the lines the controller now says the data is valid by setting the DAV line low (6). The counter then says "I'm going to accept the data now on the data lines; don't change the data lines". The counter then reads the data lines (8) and acknowledges acceptance of the data by setting the NDAC line high (9). The controller then removes the data valid signal (10) and the counter removes the data accepted signal from the bus (11). At this point one ASCII character has been transmitted by the controller to the counter and the counter is now ready to accept a new data byte. It indicates this (12) by setting the NRFD line high. The controller now puts the next character on the data line and the handshake cycle for the transfer of the character is repeated. The next character transmitted by the controller is the ASCII character U which is the talk address of the controller. As indicated in Table 3.5, by transmission of this character the calculator is making itself a talker. The next character transmitted is the quotation mark which is the listen address of the 9000A counter when it has been assigned the decimal address 02. At this point the instrument will go into its remote mode.

3.2.6.9 Lines 16 through 29 of the table illustrate the sequence of transmission of the program string which instructs the counter to make the channel A frequency measurement. Lines 30 and 31 of the table indicate the end of transmission characters CR (carriage return) and LF (line feed). Note that at line 16 of the table the controller sets the ATN line high indicating that the program string to follow in lines 17 through 31 are device dependent messages.

3.2.6.10 Having transmitted the program string of device dependent messages to the counter the controller then sets the ATN line low indicating that the characters to follow in lines 33 through 35 are bus messages. These bus messages change the talker/listener relationship of the controller and counter; the counter is made a talker and the controller becomes a listener.

3.2.6.11 Lines 37 through 50 illustrate the sequence of the transmission of data by the counter. The handshake sequence is the same when the counter is transmitting data as that outlined in lines 1 through 13 of the table except that the counter is controlling the DAV line.

3.2.6.12 Upon completion of the data transmission the 9000A transmits a carriage return (CR) and line feed (LF) to indicate the end of the data transmission.

3.2.7 Interface Message Repertoire.

3.2.7.1 The Series 9000A counter/timer is equipped with a standard GPIB interface which conforms to the specifications contained in IEEE-STD-488-1978. The specification includes the definition of multi-line interface messages and this definition divides the messages into two groups; the primary command group and the secondary command group. The information content of the secondary command group is simply the lower alphabet and a few characters such as parenthesis and a colon. The 9000A includes none of the secondary command group in its interface message repertoire.

3.2.7.2 The primary command group of interface messages is further broken down into four lower categories: (1) the listen address group, (2) the talk address group, (3) the universal command group and (4) the addressed command group. The 9000A is designed to include in its interface message repertoire 31 listen addresses and 31 talk addresses. The only interface message in the listen address group is the unlisten message which is included in the 9000A's repertoire. The only interface message in the talk address group is the untalk message to which the 9000A responds. The listen and talk address group to which the Series 9000A may be configured by its address switch to respond are listed in Table 3.4. An explanation of the use of this table is included in an accompanying paragraph.

3.2.7.3 The interface messages to which the 9000A counter/timer is designed to respond are listed in Table 3.6 along with their decimal equivalent, hex equivalent, meaning and data line code. The function of the 9000A in response to each of these commands is described in the following paragraphs.

3.2.7.4 GO TO LOCAL (GTL).

3.2.7.4.1 As shown in Table 3.6, the GTL command means go to local and the decimal and hex equivalent are both 01. Upon on receipt of this interface message the 9000A, if previously programmed for remote, will return to its local operational state. This means that the instrument will then perform the function according to the settings of the front panel controls on the instrument until such time as it returns to remote control. The 9000A must be in its listener addressed state to execute this command.

3.2.7.5 SELECTED DEVICE CLEAR (SDC).

3.2.7.5.1 Upon receipt of the SDC command the 9000A will go to the home state which is defined in Table 3.7. The

Table 3.6 - Interface Messages Used With Series 9000A Counter/Timer

Message	Meaning	HEX CODE	Decimal Equiv.	DATA LINE CODE						
				7	6	5	4	3	2	1
GTL	Go To Local	01	1	0	0	0	0	0	0	1
SDC	Selected Device Clear	04	4	0	0	0	0	1	0	0
GET	Group Execute Trigger	08	8	0	0	0	1	0	0	0
LLO	Local Lock Out	11	17	0	0	1	0	0	0	1
DCL	Device Clear	14	10	0	0	1	0	1	0	0
SPE	Serial Poll Enable	18	24	0	0	1	1	0	0	0
SPD	Serial Poll Disable	19	25	0	0	1	1	0	0	1
UNL	Unlisten	3F	63	0	1	1	1	1	1	1
UNT	Untalk	5F	9	1	0	1	1	1	1	1

Table 3.7 - Home State Condition

Operating Parameter	Home State Condition
Trigger Level A	Zero (LA + 000)
Trigger Level B	Zero (LB + 000)
Mode	J0
Channel A	A+D
Channel B	B–D
Channel A+B Trigger Range	100V
Input Configuration	Common (C0)
Function	Time Interval (F4)
T/B	–8 (G-8)
Arming	Inhibit (N0)
Input Impedance	1MΩ (E0)
Auto Trigger Speed	400 Hz (T0) or 75 Hz (T1) if Option 12 is installed
Display	No Display (D0)
Trigger Output	Don't Transmit Trigger Levels (H0)

decimal and hex equivalent are both 04. The instrument must be in its addressed listener state to execute this command.

3.2.7.6 GROUP EXECUTE TRIGGER (GET).

3.2.7.6.1 As shown in Table 3.6, the decimal and hex equivalents of the GET command are both 08. Upon receipt of the GET interface message the 9000A will start a measurement and issue SRQ when completed. The use of the group execute trigger command is to cause the simultaneous execution of a number of functions by a number of bus members at the same time. To use this command, two or more bus members are programmed to perform a function on receiving the GET interface message or a trigger command. Subsequently the controller will transmit the GET command and all bus members previously programmed will begin execution on receipt of the command.

3.2.7.7 LOCAL LOCK OUT (LLO).

3.2.7.7.1 After the 9000A has gone into remote operation it will stay in remote operation under control of the bus controller until either the bus controller gives the command go to local (GTL). Return-to-local (RTL) operation via the front panel RM button may be prevented by the bus controller by the transmission of the interface message LLO.

3.2.7.8 DEVICE CLEAR (DCL).

3.2.7.8.1 The decimal equivalent of the DCL command as shown in Table 3.6 is 20, the hex 14. This command is identical in operation to the SDC command except that the counter does not need to be in its listener addressed state.

When this command is transmitted on the bus all devices on the bus which respond to the DCL will clear.

3.2.7.9 SERIAL POLL ENABLE (SPE).

3.2.7.9.1 As shown in Table 3.6, the decimal equivalent of this interface command is 24; the hex equivalent 18. The function of this command is to cause all bus members responding to the SPE command to ready their status word. Thus, when a bus member has transmitted a service request (SRQ), the bus controller can transmit the serial poll enable command, sequentially command each bus member to transmit its status byte and thus identify the bus member requesting attention. The 9000A, upon receipt of the SPE interface message, immediately prepares to respond to a status request from the controller. If the 9000A has previously transmitted an SRQ, it will set bit 7 of the status byte to 1. The 9000A makes a service request whenever it has data ready for the controller (J1 or GET). In the case of the overflow the status byte, bit 1 will be set to the 1 state; if data is ready, bit 2 of the status byte will be set to the 1 state. Thus the serial poll allows a bus member to set the service request line to the 1 state indicating to the controller that it wants attention and the controller may sequentially interrogate each bus member to determine which bus member has requested service and the purpose for the request.

3.2.7.10 SERIAL POLL DISABLE (SPD).

3.2.7.10.1 As shown in Table 3.6 the decimal equivalent to the SPD command is 25; the hex equivalent is 19. The function of this command is to return the bus members to their original states after the serial poll transaction has been completed. The 9000A Counter must be in the "untalk" state when SPD is sent.

3.2.7.11 UNLISTEN (UNL).

3.2.7.11.1 As shown in Table 3.6 the decimal equivalent of this command is 63; the hex equivalent is 3F. This command is also a universal interface message understood by all members of the bus as a command to go to the unlisten state. When this command is transmitted all bus members previously in the listen state will return to the unlisten state.

3.2.7.12 UNTALK (UNT).

3.2.7.12.1 The untalk command is the counterpart of the TALK Command: it causes the instrument to leave the talk mode. The 9000A Counter is automatically removed from the talk mode whenever a talk address other than its own is received.

3.2.7.12.2 As shown in Table 3.6 the hex code is 5F and the decimal equivalent is 95. Like the Unlisten message it is universal and when transmitted on the bus by a controller all bus members go to the untalk condition.

3.2.8 Status Byte.

3.2.8.1 To inform the controller of its status the Series 9000A assembles and transmits a status message referred to as the status byte. The controller generates the serial poll enable cycle in order to find out which bus member has requested service. When the instrument receives the serial poll enable command it transmits the status byte to the controller after having been made a talker.

3.2.8.2 The status byte is shown in Figure 3.5. Note that it contains 3 bits that convey specific information. Bit 1 when set to a 1 indicates that the instrument has overflowed. Bit 2 when set to the 1 state indicates that the instrument has completed a measurement and has data ready for transmission on the bus to the controller. Bit 7 indicates that the 9000A has transmitted a service request (SRQ).

3.2.8.3 SERIAL POLL PROCEDURE.

ATN Low
Controller Listen Address
Serial Poll Enable
Instrument No. 1 Talk Address
ATN High

Instrument No. 1 Sends Status Byte
ATN Low
Instrument No. 2 Talk Address (Instrument No. 1 automatically leaves its TALK mode).
ATN High

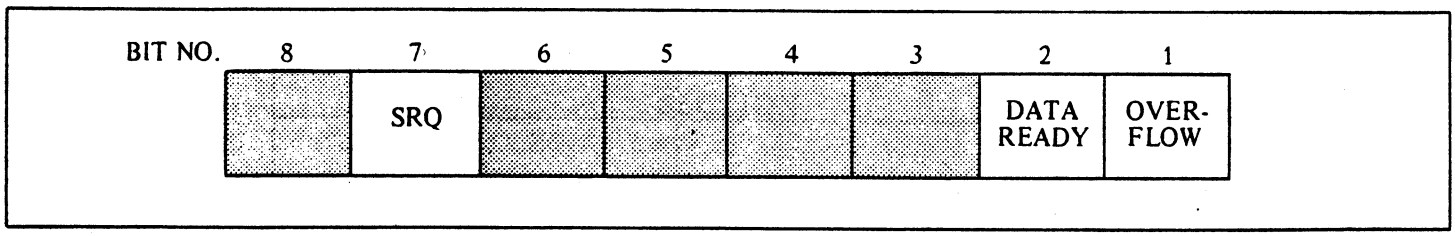


Figure 3.5 - Status Byte Format

Instrument No. 2 Sends Status Byte (Every instrument is polled as shown above).

.
.

ATN Low
UNL
UNT

Serial Poll Disable
ATN High

3.2.9 Device Dependent Messages.

3.2.9.1 The messages which control the operation of the 9000A timer/counter when in system operation are referred to as device dependent messages. These messages are simply combinations of ASCII characters which the instrument recognizes as specific instructions. ASCII alpha characters may be upper or lower case. To program the instrument for a specific operation the operator programs the controller to transmit a sequence of these messages referred to as a *program string*. The program string is variable in length and has no fixed format. The only format requirements are that an individual command be transmitted as a pair of characters or in some cases three characters. Individual commands may be transmitted in any order and require no delineators or spacing for the instrument to understand.

3.2.9.2 The device dependent messages are listed in Table 3.8 along with the 9000A operation and any special notes that apply. The table lists the function of each message, along with the equivalent keyboard pushbutton and the ASCII instruction character or combination of characters used for programming the instrument. In general, the various commands cause the instrument to perform the same functions as the front panel control settings do as outlined in the section on bench operation. There are special cases however, where there are extra functions available under remote control which are not available in the bench operation mode. The following paragraphs describe the function of each of the device dependent messages and the presentation of any special considerations applicable to the various individual messages.

3.2.9.3 FUNCTION COMMANDS.

3.2.9.3.1 There is a function command equivalent for every manual operation. Refer to Table 3.8 and note that the first entry is the measurement of the frequency in channel A. This is shown in the Operation column as Frequency A. The manual operation is shown under the Keyboard Equivalent column as the pushbutton FA. The GPIB message column shows the device dependent message required to program the instrument as F0. The Note column of the table indicates the measurement operation that the GPIB message will perform. In this case, F0 selects frequency channel A 0 to 100 MHz.

3.2.9.4 GATE/TIME MULTIPLIER.

3.2.9.4.1 Control of the Gate/Time Multiplier is accomplished via the bus by transmitting 3 characters as follows: the identifier is the letter G, the second character is a minus sign or a plus sign to indicate the polarity of the time base exponent and a numeric character indicating the value of the gate time exponent. Table 3.8 shows the interface message G-3. This programs the instrument for a 1 millisecond gate or a resolution of 1 kilohertz.

3.2.9.5 INPUT CONFIGURATION.

3.2.9.5.1 The input configuration switch is illustrated in the keyboard equivalent column of Table 3.8 and as shown the switch may be set to separate (SEP), test or common (COM) positions. The operation is identical in both local and remote modes. For example, if it is desired to connect channel A and B inputs in common, the program string should contain the GPIB message C1.

3.2.9.6 CHANNEL SLOPE AND COUPLING.

3.2.9.6.1 The GPIB messages used for controlling the channel slope and coupling are 3 character messages. The first is an alphabetic character indicating the channel and must always be an A or B. The second is the slope indicator and is the plus or minus character. The only legal characters for the third characters are the alphabetic characters A and D; A sets the indicated channel for AC coupling while the character D will configure the channel for DC coupling.

3.2.9.7 TRIGGER LEVEL INSTRUCTIONS.

3.2.9.7.1 Just as in the bench operation mode the 9000A may be set to set its own trigger levels automatically or the trigger levels may be set to some specific desired level before the instrument is put into operation. Further, the trigger levels may be changed while the instrument is in operation by transmitting additional trigger control commands.

3.2.9.7.2 The simplest method of operation, of course, is to use the auto trigger mode. Like the input configuration, the trigger levels must be programmed for each channel. To set the channel A into auto trigger mode the controller transmits the ASCII characters LAA. This mneumonic comes from the words Level A Auto. There is a similar command for channel B, LBA from the words Level B Auto.

3.2.9.7.3 It is sometimes useful to have the instrument trigger at predetermined signal levels. For example, in making a rise time measurement the peaks of the signal can be measured through the use of a scope or the 9000A counter. The trigger levels can then be set to any desired level to measure the time interval between the two channel triggers. In remote operation this is accomplished by simply transmitting the message identifier L followed by the channel identifier A or B, the trigger level polarity sign plus or minus and 3 digits indicating the trigger level voltage desired. In the example shown in Table 3.8 the GPIB message is programming channel A trigger level for a positive 1.5 volts. Note that the GPIB message is LA+1.50 as indicated in Table 3.8.

3.2.9.7.4 Figure 3.6 illustrates a waveform and the voltage levels used for a time interval measurement.

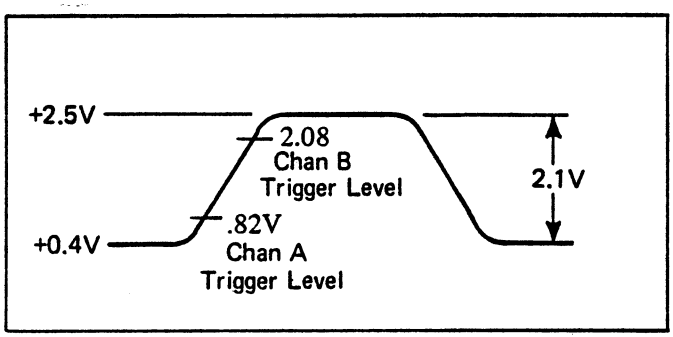


Figure 3.6 - Rise Time Measurement

3.2.9.7.5 Assume that it is desired to measure the slew rate of the pulse shown. Note that the pulse starts at .4 volts and rises to a peak of 2.5 volts. Assume further that it is desired to measure the time that it takes for the level to rise from the 20 percent to the 80 percent point of the pulse. Channel A trigger level would be programmed for .82 volts while channel B would be programmed to trigger at 2.08 volts.

3.2.9.8 CONSTANT.

3.2.9.8.1 On the instruments equipped with the arithmatic option the controller may add, multiply or divide the measurement by constants transmitted over the GPIB. Table 3.8 illustrates the GPIB messages required for these constant functions. In the Operation column note that the example used is add 38.5 to the measurement multiplied by the constant 15 and divide by 300. The GPIB message column shows the characters required for transmission of the constant to the instrument. The sequence of the constant message is as follows: first the message identifier, the alphabetic character K, then the numeric value of the constant which may contain up to 9 digits and a decimal point. Note that the decimal point may be located in anyone of 4 positions as shown in Table 3.8. The last character in the constant message is the alphabetic character indicating the arithmetic operation add (A), multiply (M) or divide (D).

3.2.9.9 PULSE PARAMETER.

3.2.9.9.1 On -11A Models the controller may call for pulse parameter measurements. The measurement operations, keyboard equivalent pushbuttons and GPIB messages are shown in Table 3.8.

3.2.9.10 MEASUREMENT OPERATION.

3.2.9.10.1 The instrument may be instructed to perform 3 different measurement sequences as shown in Table 3.8. The normal or home state is the J0 state in which the instrument is cleared and armed to measure when addressed to talk. Note that as shown in Table 3.8 the instrument returns to the J0 mode after execution of either the J1 or J2 modes. This means that after execution of the J1 mode, for example, if it is desired to perform another J1 operation sequence, the J1 must be transmitted again. The J3 mode allows the 9000A to make continuous measurements. The measurements will be sent out when the 9000A is made into a talker. The 9000A will remain in the J3 mode till a J0, J1, or J3 is sent.

3.2.9.11 INVERT.

3.2.9.11.1 The invert instruction as shown in Table 3.8 is the alphabetic character I. This operation causes the instrument to divide the measurement result into one (1/X where X = measurement). The invert operation is cancelled by a function command.

3.2.9.12 TRIGGER OUTPUT.

3.2.9.12.1 The instrument may be commanded to transmit the trigger levels via the GPIB to the controller. To cause the instrument to transmit trigger levels the program string should contain the GPIB message H1 as shown in Table 3.8. In this mode the instrument will transmit trigger levels as a part of the measurement message. The format of the output message is shown in Table 3.3 included in the discussion of the data output format.

3.2.9.13 DISPLAY.

3.2.9.13.1 Table 3.8 shows the GPIB messages for controlling the display on the front panel of the instrument. To operate the instrument in remote mode without displaying measurements simply include D0 in the program string. In the D1 display mode, measurements are displayed after the external controller has received the data. In the D2 display mode, measurements are displayed upon completion of the measurement, whether the external controller has received the data or not.

3.2.9.14 INPUT IMPEDANCE (OPTION 06PA).

3.2.9.14.1 For instruments equipped with 06PA the GPIB messages E0 and E1 select 1 megohm or 50 ohms input impedances respectively as shown in Table 3.8.

CAUTION

The maximum input voltage with 50 ohm input must be limited to less than 5 volts rms.

3.2.9.15 EXTERNAL GATE CONTROL.

3.2.9.15.1 For instruments equipped with option 06PA a series of GPIB messages is available for remotely programming the operation of the external gate signals applied to the rear connector. The instrument operates in the same manner described in the operating instructions of Section 2 of this manual. There are no keyboard equivalent operations since the external gate control is a function of the rear panel switch and the signal applied through the BNC connector on the rear panel of the instrument.

3.2.9.15.2 *External Arm Inhibit.* To operate the counter normally the GPIB message N0 is transmitted. The N0 command can be used to take the instrument out of the selective gate, synchronous window or gate delay mode.

3.2.9.15.3 *Selective Gate.* As shown in Table 3.8 transmission of the GPIB message N1 causes the instrument to go into the selective gate mode of operation. This mode of operation is described in Section 2 of this manual.

3.2.9.15.4 *Synchronous Window.* To remotely program the instrument for synchronous window mode of operation the GPIB message N2 is transmitted over the bus.

3.2.9.15.5 *Gate Delay.* To use the gate delay feature while in remote operation transmit the GPIB message N4 over the interface.

3.2.9.16 RESET.

3.2.9.16.1 The instrument may be reset to its home state via the alphabetic character R (reference Table 3.8). The condition of the various internal circuits of the instrument (in the home state) is shown in Table 3.7.

3.2.9.17 AUTO TRIGGER SPEED.

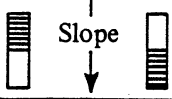
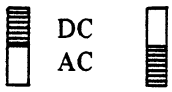
3.2.9.17.1 The trigger level speed of the 9000A may be programmed for optimum performance via the alpha-numeric characters T0 thru T3 (reference Table 3.8). Keyboard equivalents of these commands are not available, therefore, in manual operation, the minimum trigger frequency for the Series 9000A will be 75 Hz with Option 12 and 400 Hz without Option 12. (Option 12 available only with -11A Models).

Table 3.8 - 9000A Device Dependent Messages

OPERATION	KEYBOARD EQUIVALENT	GPIB MESSAGE	NOTES
Function Frequency A	FA	FØ	Selects frequency Channel A, 0-100 MHz
Frequency C	FC	F1	Selects frequency Channel C, 512 MHz (9035A only)
Period	P	F2	Selects period mode for Channel A.
Period Average	P AV	F3	Selects period average mode for Channel A.
Time Interval	TI	F4*	Selects time interval mode.
Time Interval Average	TI AV	F5	Used in conjunction with input configuration, slope and coupling.
Totalize	TO	F6	Selects totalize mode, Channel A only. Used with S command (start-stop).
Ratio	RA	F7	Selects ratio mode Channel A&B.
Start-Stop	SS	S	Must be transmitted as the last character of the program string. The first S will open the measurement gate and the second S will close the gate when in totalize mode. (must be used in J1 or J2 mode).
Gate/Time Multiplier	CH 3	G-3 (G-8)*	Depending on the function selected i.e., FØ, F5. Gate time/multiplier has a range of 6^{+9} to 6^{-8}.
Input Configuration Separate	Test Sep ▮▮▯ Com	CØ	Channel A&B separate
Common	Test Sep ▯▮▮ Com	C1*	Channel A&B common Input impedance A: 500 KΩ or 50Ω B: Open or 50Ω See E0 and E1 commands
Test	Test Sep ▯▮▮▯ Com	C2	Internal 10 MHz applied to both Channel A&B input connectors NOTE: Because of internal firmware, these commands are not needed for automatic pulse parameter measurements.

*Reset or Home State

Table 3.8 - 9000A Device Dependent Messages continued

OPERATION	KEYBOARD EQUIVALENT	GPIB MESSAGE	NOTES
Channel Slope and Coupling A pos slope DC coupled	Cha A ↑ Cha B  Slope	A+D*	
B neg slope AC coupled	 DC AC	B–A (B-D)*	NOTE: Because of internal firmware these commands are not needed for automatic pulse parameter measurements.
Trigger Level Instructions Trigger Level A Positive 1.5V	A A TL 1 . 5 TL	LA+1.50 (LA+000) (LB+000)	NOTE: These commands are not needed for automatic pulse parameter measurements except if triggering at some level other than 10% & 90% point. Format and Ranges X1: LA ± 0.00 to +3.19, –3.20 X10: LA ± 00.0 to +31.9, –32.0 X100: LA ± 000 to +319, –320 Leading zeroes or spaces must be transmitted for a total of three digits. Notice that the decimal point determines the range in the X1 and X10 volts ranges. Positive sign may be omitted.
Trigger Level B Auto	B TL AU	LBA	
Constant Add 38.5	+ 3 8 . 5 +	K38.5A	(Models 9015A, 9035A Only)
Multiply by 15	X 1 5 X	K15M	The decimal point may appear in one of four places as shown below.
Divide by 300	÷ CS 3 EX 2 ÷	K-3E2D	.N.N.N.NNNNNN ENN up to six digits may follow the decimal point. The mantissa may contain up to nine digits.
Pulse Parameter Rise Time		MØ	
Fall Time		M1	(-11A Models Only)
Pulse Width		M2	

*Reset or Home State

OPERATION	KEYBOARD EQUIVALENT	GPIB MESSAGE	NOTES
Measurement Clear, Arm to measure when addressed to talk	None	JØ*	Measurement is made and sent when 9000A is made a talker. NOTE: The instrument returns to JØ mode after execution of either J1 or J2 modes.
Clear, measure, SRQ & then transmit when addressed to talk	None	J1	Measurement is made at the time when J1 is received. SRQ is sent at completion of the measurement. This mode is also initiated by GET command (see 3.2.7.4).
Clear, measure & then transmit when addressed to talk	None	J2	Measurement is made at the time J2 is received.
Clear, measure continuously	None	J3	Measurements are continuously made and sent out on the bus when the 9000A is made a talker.
Invert	I/X	I	Invert operation is cancelled when a function is programmed after the command I.
Trigger Output Don't transmit trigger levels	None	HØ*	
Transmit trigger levels	None	H1	Format and Ranges X1 ±0.00 to +3.19, –3.20 X10 ±00.0 to +31.9, –32.0 X100 ±000. to +319., –320. CRLF follows output of each trigger level.
Display Don't display measurement on front panel	None	DØ*	
Display measurement on front panel	None	D1	Measurement is displayed only after controller accepts measurement data.
	None	D2	Measurement is displayed upon completion of reading.
Input Impedance	None	EØ*	1 megohm input impedance.
		E1	50 ohm input impedance. NOTE: For use with 9000A's equipped with Options Ø6PA. Both Channels A&B are internally terminated with 50 ohm or 1 megohm. The maximum input voltage with 50 ohm input impedance must be limited to less than 5 volts rms.

*Power on State

Table 3.8 - 9000A Device Dependent Messages continued

OPERATION	KEYBOARD EQUIVALENT	GPIB MESSAGE	NOTES
Reset	INT	R	Sends 9000A to TI, G-8, TLA and TLB to 100 volt range.
External Arm Inhibit	None	NØ	Counter operates normally. Signal on External Gate Control BNC connector has no effect.
Selective Gate	None	N1	NOTE: For use with 9000A's equipped with Option Ø6PA only.
Synchronous Window	None	N2	
Gate Delay	None	N4	
Auto Trigger Speed 400 Hz Minimum Frequency	None (Standard 9000)	TØ	Minimum Auto-Trigger frequency may be selected for optimum Auto-Trigger speed.
75 Hz Minimum Frequency	None (Option 12)	T1	
40 Hz Minimum Frequency	None	T2	
2 KHz Minimum Frequency	None	T3	

3.2.10 Trigger Level And Measurement Data Output Messages.

3.2.10.1 The instrument transmits measurement and trigger level information via the GPIB to the controller. A discussion of the message formats is presented in the following paragraphs.

3.2.10.2 TRIGGER LEVEL OUTPUT.

3.2.10.2.1 When the command H1 is programmed, the counter will output both trigger levels A&B in that order following the following format:

± D.D.D.CRLF ± D.D.D.CRLF *

Exactly three digits are transmitted with the decimal point indicating X1, X10 or X100 input range. The measurement ' 'a, if any, will follow the trigger level output provided . the counter is left as a talker. Re-addressing of the counter as a talker will result in the trigger levels being transmitted again from the start.

*In the J0 mode the CRLF must be taken by the controller in order for the 9000A to initiate a subsequent reading.

3.2.10.3 MEASUREMENT DATA OUTPUT.

3.2.10.3.1 The measurement data will be transmitted by the counter when addressed as a talker if the counter has been programmed to the H0 output mode; otherwise, it will follow the trigger level data.

3.2.10.4 MEASUREMENT DATA FORMAT.

3.2.10.4.1 The measurement data is processed by the 9000A to eliminate all leading and trailing non-significant zeroes. It is output in exponential format with leading decimal point. In case of overflow, the ASCII character "O" will precede the measurement data. See last example below for maximum number of output characters.

Examples,

Measurement	Data Output
1.000 KHz (1 Hz resolution)	+.1ØØØE+Ø4 CRLF *
OF 10 nsec (1 nsec resolution)	O+.1ØE−11 CRLF
OF (exact overflow)	O CRLF
0. Hz	CRLF
OF 100.000000 mSec	O+.1ØØØØØØØØE+ØØCRLF

3.2.11 Programmable External Gate Control (Option 06PA).

3.2.11.1 The Option 06PA feature of the Series 9000A Counter provides the user with remote control of the External Gate Control features when Option 55 has been installed. The primary difference between the standard model and 06PA is that the gate control may be selected by the controller. A simplified block diagram of the 06PA option is shown in Figure 3.7. The controller transmits commands as part of the program string. In the 9000A Counter these commands come up randomly when power is applied thus they must be included in the power-up initialization routine. The commands and their effect are shown in Table 3.9.

3.2.11.2 The following paragraphs present examples of counter programming using option 06PA. In the following description and examples, it is assumed that the trigger level output commands (H0, H1) and the display commands (D0, D1, D2) have been previously programmed.

Table 3.9 - Program Commands

GPIB Command	Description
N0	Inhibit. Counter operates normally. Signal on External Gate Control BNC connector has no effect.
N1	Selective Gate A→B
N2	Synchronous Window A&B
N4	Gate Delay (NORM)
E0	1 megohm input impedance
E1	50 ohm input impedance

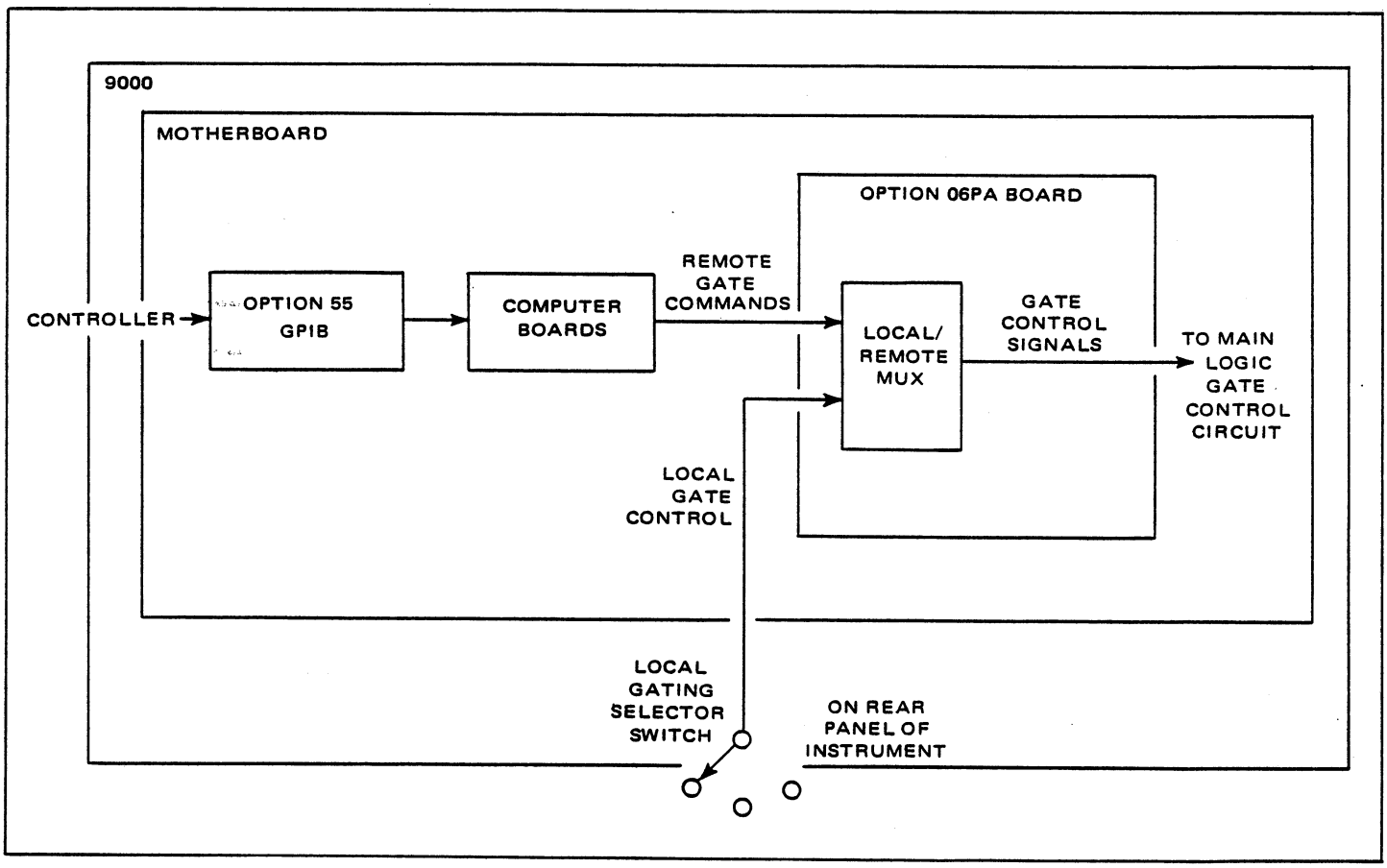


Figure 3.7 - Option 06PA Simplified Block Diagram

3.2.11.3 SELECTIVE GATE.

3.2.11.3.1 This mode of operation is mainly used to measure time intervals between an arbitrary number of pulses or events in a train of pulses.

3.2.11.3.2 *Example 1.* To measure the time-interval between the rising edge of the first pulse and the falling edge of the 5th pulse in a pulse train the counter is programmed as follows:

Time Interval Function	F4
Selective Gate Mode	N1
Common Input Channels	C1
A Positive Slope DC Coupled	A + D
B Negative Slope DC Coupled	B – D
Trigger Level A Automatic	LAA
Trigger Level B Automatic	LBA
Clear, Measure, SRQ, and Xmit on Talk	J1

3.2.11.3.2.1 If the input and control waveforms shown below are applied to the counter, the resultant time interval measured will be as shown in Figure 3.8.

3.2.11.3.2.2 In this mode of measurement, the rising edge of the control waveform causes the counter to be armed to start a measurement. Once the measurement starts, it cannot terminate until the level of the control waveform turns low.

3.2.11.3.2.3 This mode of measurement can be used with all functions except TOTALIZE. In each case, the counter is armed with the rising edge of the control waveform and the measurement is not allowed to be completed until the level returns low.

3.2.11.3.3 *Example 2.* To measure number of events in a Sec window the counter is programmed as follows:

Frequency A	F0
Selective Gate Mode	N1
Exponent = 1 Sec Gate Time	G0
Inputs Separate	C0
Channel A Positive Slope, DC Coupled	A + D
Trigger Level Channel A Automatic	LAA
Clear, Measure, SRQ, Transmit when Talked	J1

3.2.11.3.3.1 When programmed as shown above and provided with a control waveform with a length greater than one second but less than two seconds the counter will keep the measurement gate open for two seconds as shown in Figure 3.9.

3.2.11.3.4 *Example 3.* To measure the time between five waveform cycles program the counter as follows:

Period	F2
Selective Gate Mode	N1
Input Separate	C0
Channel A Positive Slope, DC Coupled	A + D
Trigger Level Channel A Automatic	LAA
Clear, Measure, SRQ, Transmit when Talked	J1

3.2.11.3.4.1 When programmed as shown and when provided with a control waveform with a length greater than five measurement waveform cycles, the counter will measure the period between the leading edges of the first and sixth measurement waveform cycles as shown in Figure 3.10.

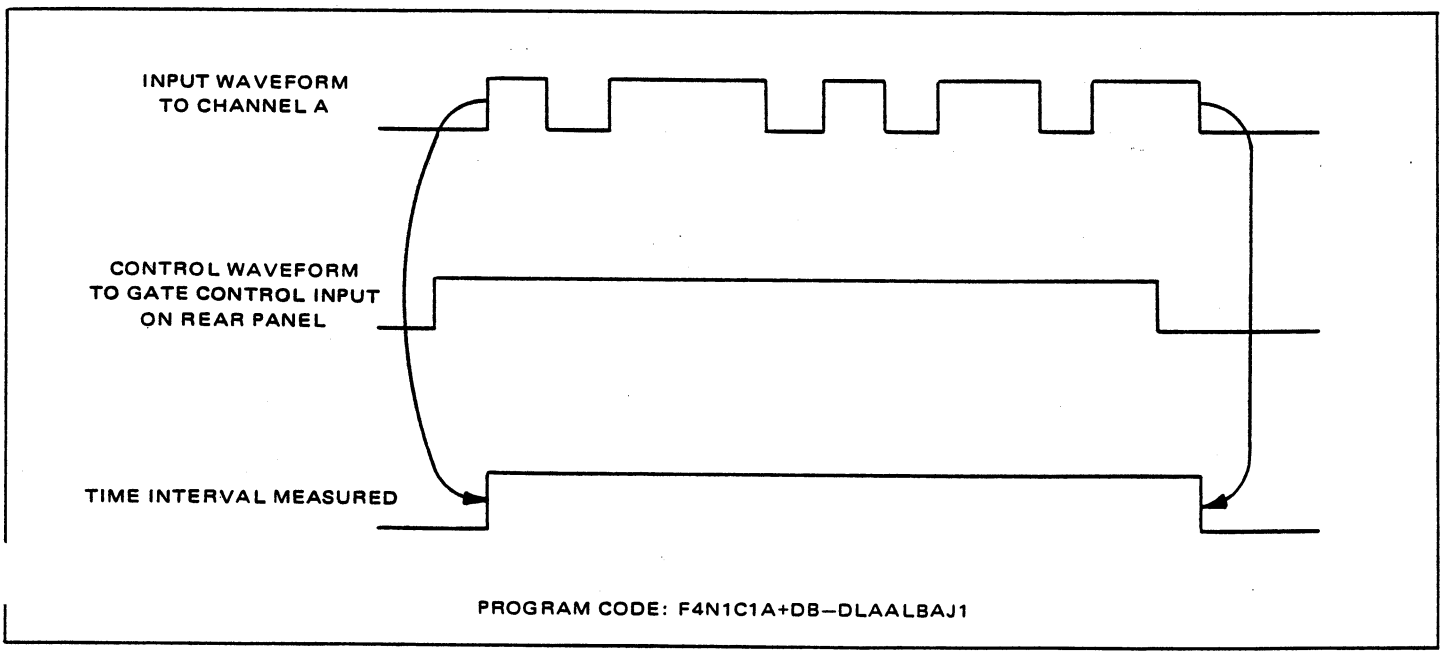


Figure 3.8 - Selective Gate Example 1

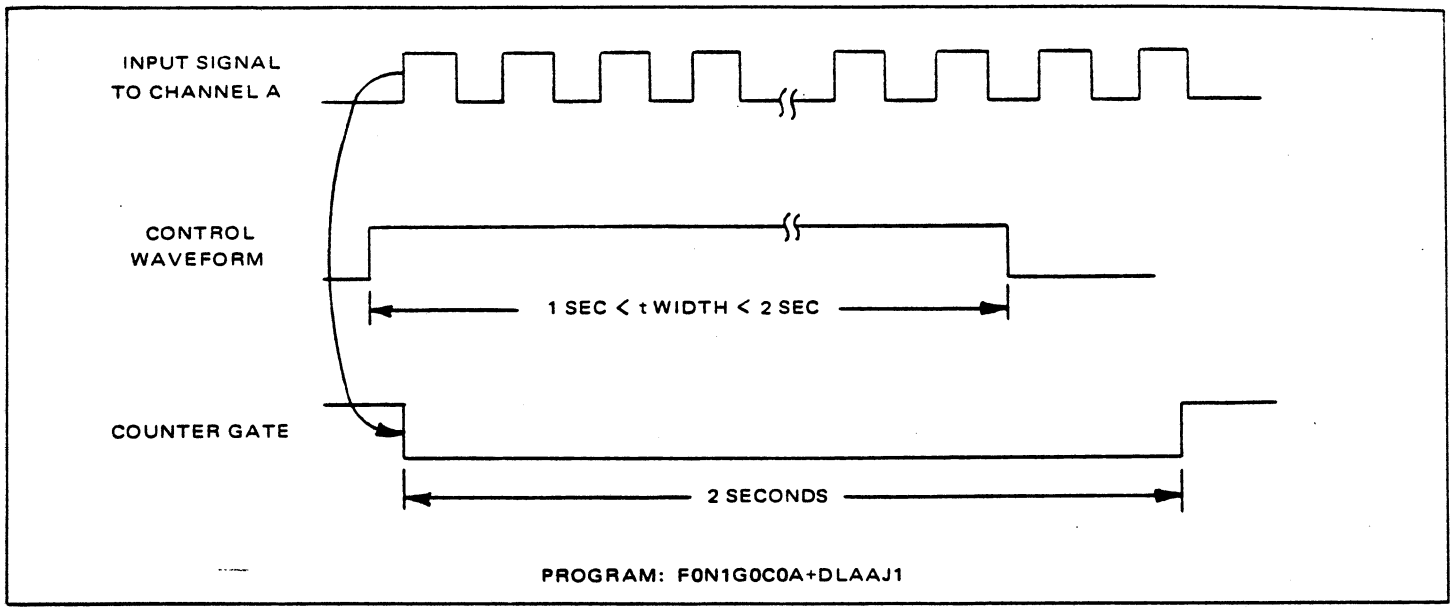


Figure 3.9 - Selective Gate Example 2

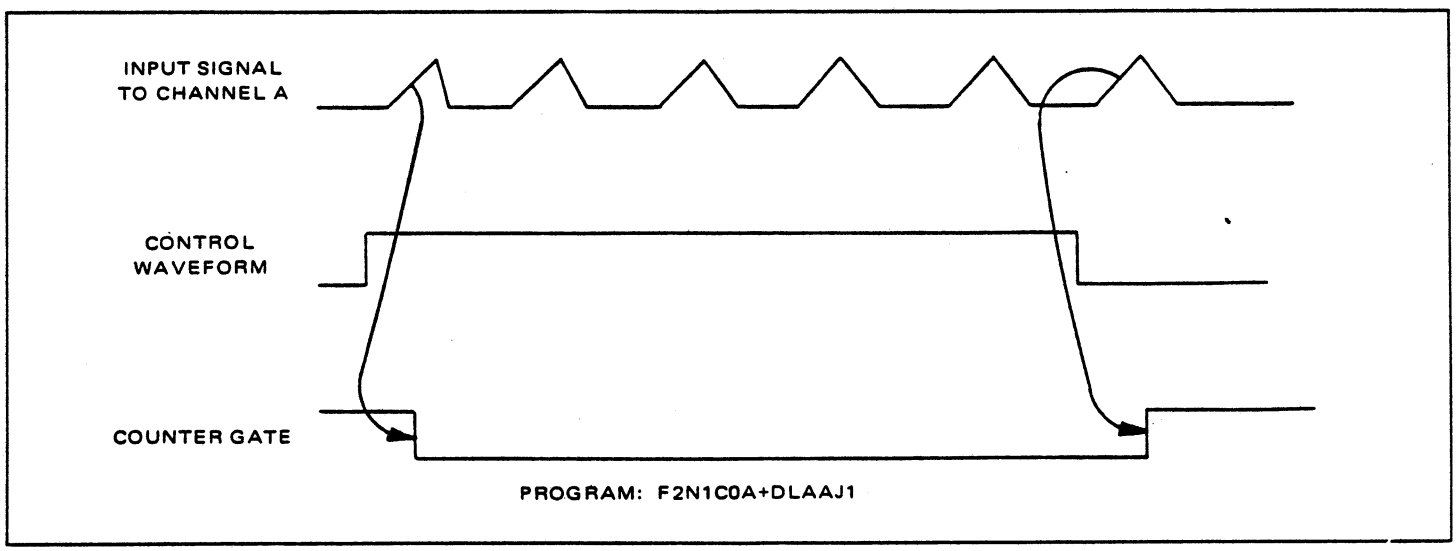


Figure 3.10 - Selective Gate Example 3

3.2.11.4 SYNCHRONOUS WINDOW.

3.2.11.4.1 This mode of operation is used when it is desired to select a portion of a waveform to analyze. It is only used with the Time Interval Average function, and it causes the counter to "see" only the part of the input signal which is "bracketed" by the control waveform.

3.2.11.4.2 *Example 1.* To measure rise time of the second pulse in a pulse train (with -11A Models) program the counter as follows:

Time Interval Average	F5
Synchronous Window Mode	N2
Exponent = Average 1000	G + 3
Rise Time	M0
Clear, Measure, SRQ, and Transmit when Talked	J1

3.2.11.4.2.1 When programmed as shown and provided with a control waveform which brackets the pulse to be measured as shown below the counter will measure and calculate the average rise time of the bracketed pulse for 1000 measurements as shown in Figure 3.11.

3.2.11.4.3 *Example 2.* Given two pulse trains, to measure the time between the rising edges of the second pulse in both waveforms program the counter as follows:

Time Interval Average	F5
Synchronous Window Mode	N2
Inputs Separate	C0
Exponent = Average 1000	G + 3
Channel A Positive Slope, DC Coupled	A + D
Channel B Positive Slope, DC Coupled	B + D
Channel A Trigger Level Automatic	LAA
Channel B Trigger Level Automatic	LBA
Clear, Measure, SRQ, and Transmit when Talked	J1

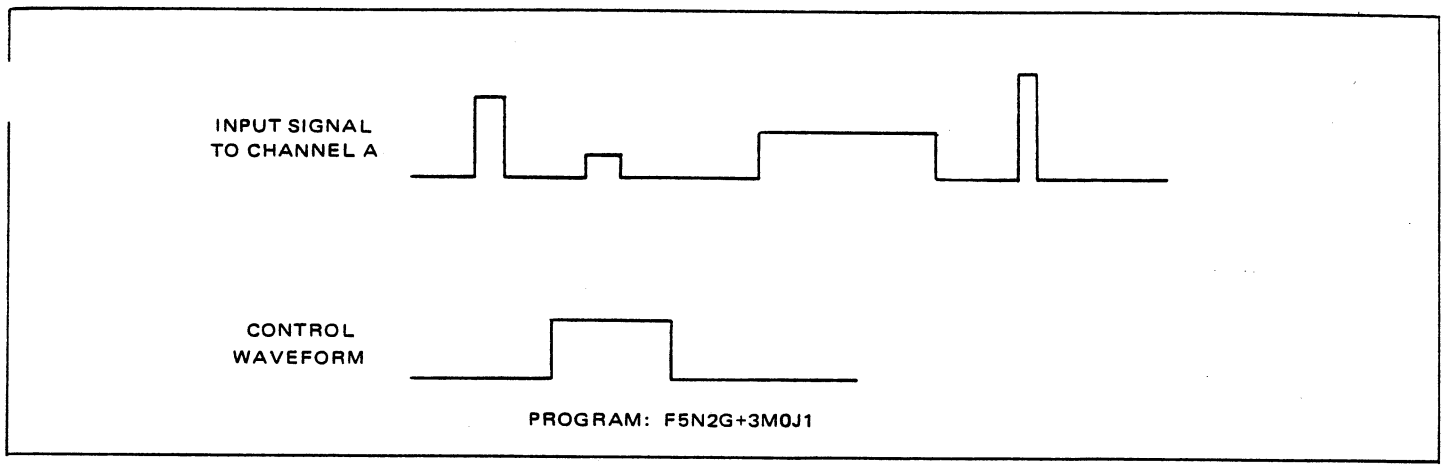
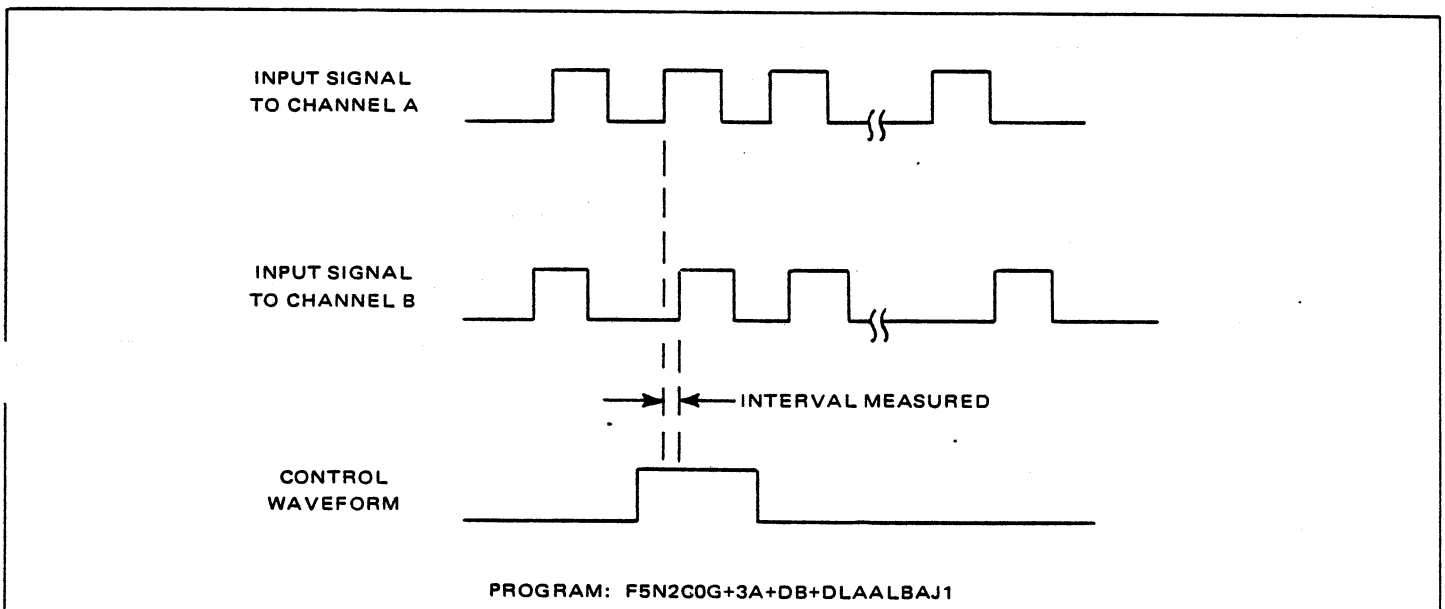


Figure 3.11 - Synchronous Window Example 1



NOTE: The control waveform must "bracket" both a rising and a falling edge for each input signal even though the desired measurement is between two rising edges.

Figure 3.12 - Synchronous Window Example 2

3.2.11.4.3.1 When programmed as shown above the counter will measure and calculate the average time between the pulses bracketed by the control waveform for 1000 measurements as shown in Figure 3.12.

3.2.11.5 GATE DELAY.

3.2.11.5.1 This mode of measurement is very similar to the selective gate mode except that the counter does not arm at the rising edge of the control waveform. The counter is kept from finishing a measurement whenever the control veform is at a high level.

3.2.11.5.2 A typical application of this mode is to measure the time between R.F. bursts (< 100 MHz) when a control signal is not available (i.e., the selective gate mode cannot be used).

3.2.11.5.3 In this case the setup shown in Figure 3.13 will make the measurement.

3.2.11.5.4 Program the counter as follows:

Period	F2
Gate Delay	N4
Inputs Separate	C0
Channel A Positive Slope, DC Coupled	A + D
Trigger Level Channel A Automatic	LAA
Clear, Measure, SRQ, and Transmit when Talked	J1

3.2.11.5.5 In this case the test setup provides a control waveform a little longer than the R.F. burst thus preventing the counter from closing the measurement gate until the start of the next R.F. burst. The result is a measurement period starting at the beginning of the first R.F. burst and ending at the beginning of the next R.F. burst as shown in Figure 3.14.

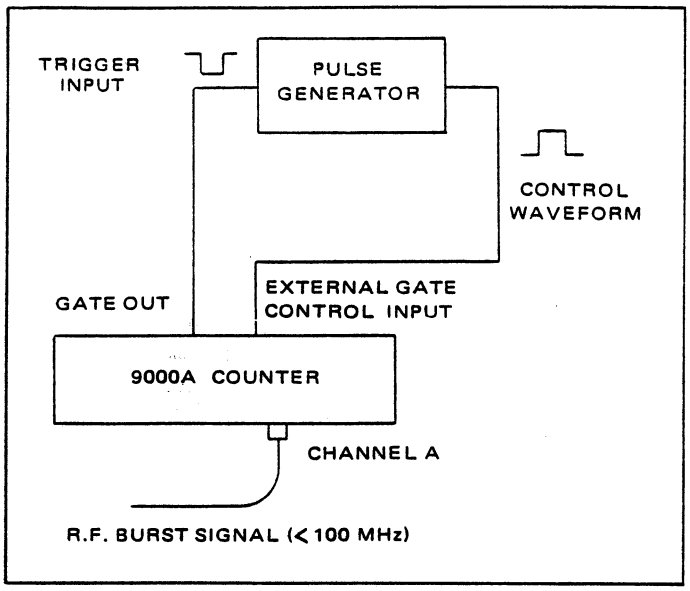


Figure 3.13 - Gate Delay Measurement Connections

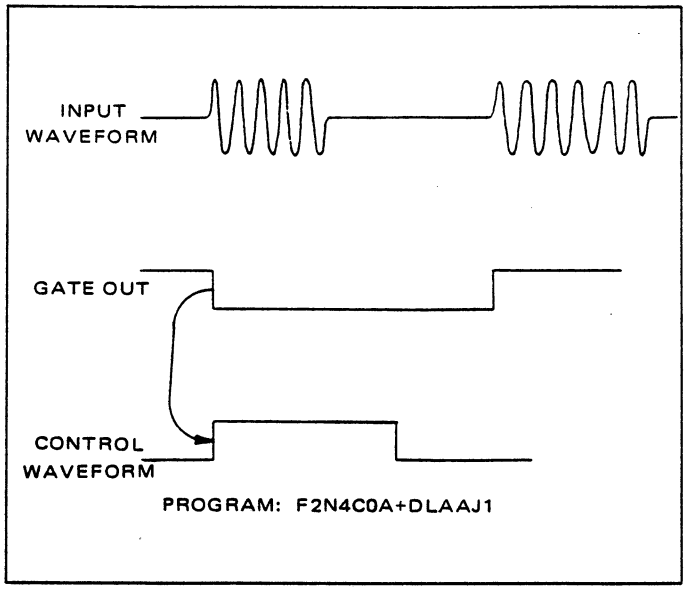


Figure 3.14 - Gate Delay Timing Example

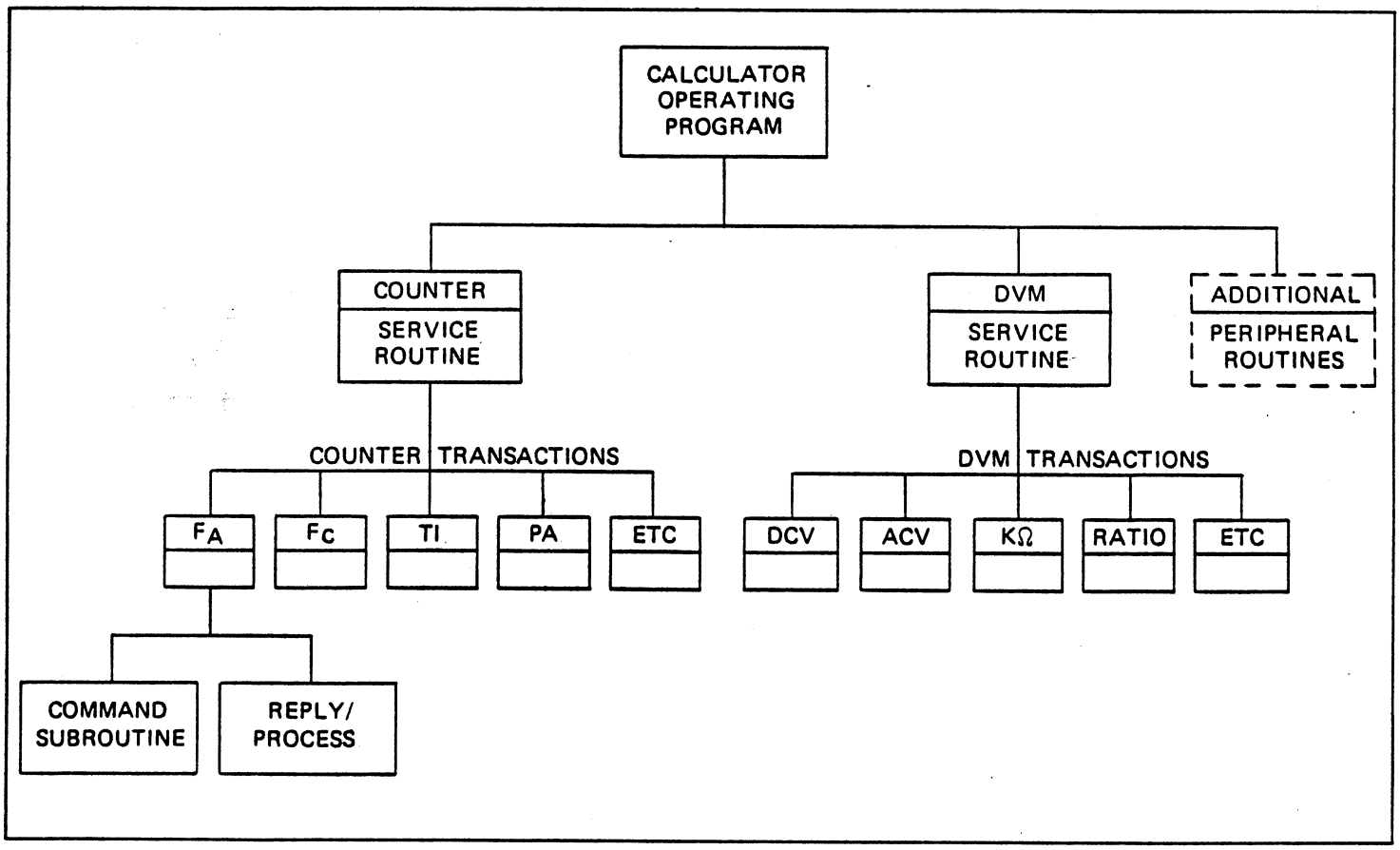


Figure 3.15 - Software Organization

Action or Message	Active Unit	Transaction	
IFC	C	Interface Message	COMMAND Subroutine
ATN	C		
UNLISTEN	C		
I TALK	C		
YOU LISTEN	C		
FØ	C	Device Dependent Message Command Characters	
G5	C		
A+D	C		
CØ			
ATN	C	Interface Message	REPLY Subroutine
UNLISTEN	C		
J TALK	C		
I LISTEN	C		
• 1 2 3 4 5 6 7 8 9 E + 0 7 CR LF	9000A ↓ 9000A	Peripheral Message Reply (Data, Status) Characters	

Figure 3.16 - Series 9000A Counter Transaction For Frequency Measurement, Channel A

3.3 SOFTWARE ORGANIZATION.

3.3.1 The following paragraphs are presented to acquaint the reader with the device messages used when operating 9000A Counter/Timer and to explain the relationship of these device dependent messages to the user's overall software package.

3.3.2 A calculator, computer or other controller device software package usually includes a collection of transactions, service routines and subroutines for controlling all of the elements of a system. The relationship of the various parts of a typical software operating system are illustrated in Figure 3.15. A complete operating system may include the main executive program, the keyboard monitor program, some form of statistical routine, an arithmetic or decision making routine and a set of peripheral servicing routines. Figure 4.1 illustrates a portion of a software package referred to as an operating system. The portion illustrated is a typical collection of peripheral service routines. These peripheral service routines are groups of subroutines known as transactions. Note that the illustration shows a service routine for a counter, a digital voltmeter and a number of additional peripheral equipments. A counter service routine for the 9000A might include a number of transactions depending on the application of the instrument in the system. Each transaction will include the bus commands and device messages necessary to accomplish the specific function for each transaction. Note that the transactions shown are for FA (Frequency A), FC (Frequency C), TI (Time Interval), PA (Period Average) and any number of other transactions necessary for the particular counter application. Note that under the FA transaction block a further breakdown is illustrated: that of the command subroutine and the reply or process subroutine. This is the point in the overall software structure that the 9000A device messages appear.

3.3.3 Counter Transactions.

3.3.3.1 Figure 3.16 illustrates a typical counter transaction designed to operate the 9000A. The left-hand column of the illustration titled "Bus Action or Message" contains a sequence of bus control line titles and device characters. The second column of the illustration indicates whether the controller or the counter is controlling the bus or transmitting the characters. This column is titled "Active Unit or Talker". The brackets to the right of the second column identify the portion of the transaction as the command subroutine or the reply subroutine. Note that the command portion of the transaction includes an interface message which establishes the talker/listener relationship and the

device dependent message which instructs the counter to perform a specific operation. Once the peripheral, in this case the 9000A Counter/Timer, has been programmed to perform a function the controller transmits the second interface message to reestablish the listener/talker relationship and the counter makes the measurement and transmits a series of characters over the interface bus which represents the measurement data.

3.4 HIGH SPEED INTERFACE, OPTION 56.

3.4.1 Programming Considerations.

3.4.1.1 Use of the 9000A Counter as a peripheral in minicomputer applications requires consideration of the various operating modes, speeds and input/output formats available to the user. Information concerning operating modes, cycle times and speed is presented in the Theory of Operation, Section 4 of this manual. Information concerning the command and measurement data formats and programming sequences are presented in the following paragraphs. In addition this section contains the I/O connector pin/signal assignments usually found in the installation section. Because the signal assignments are so closely related to the data format and computer programming this information is presented here.

3.4.2 Programming Commands.

3.4.2.1 All computer instructions or commands are transmitted to the counter via the 16-bit data bus regardless of the measurement format selected. The purpose, function, and format of these command words are presented in Figures 3.17 through 3.21. An example of a command word sequence is illustrated in Figure 3.23. The length of the command sequence and number of words is variable depending upon the operation to be programmed.

3.4.3 Interface Electrical Connection.

3.4.3.1 The interface connector and pin assignments for the Parallel format are shown in Table 3.10. Note that this table shows only that J211, Pins 1 through 16 are used for the 16-bit data bus without definition of the individual command or status word formats.

3.4.3.2 The connector and pin assignments for the 16-bit data bus and the output word formats are shown in Figure 3.22. Note that at the top of the illustration the J211 and J212 pin assignments are shown for the measurement data when transmitted in the 16-bit MUX mode. The J211 and J212 connector pins are not connected internally; this parallel connection must be made externally when it is desired to configure the counter for 16-bit MUX format operation. Refer to the functional block diagram (Figure 4.35) and note that the input to the Command Register and the output of the Measurement Data Register are shown to be connected to the 16-bit data bus. This connection must be made externally if bidirectional data flow is desired.

3.4.4 Control Signal Description.

3.4.4.1 Communication between the counter and computer is controlled by signal lines which carry control and status signals. A description of these signals and their functions is presented in table 3.11.

3.4.4.2 The sequence of control and status signals exchanged between the computer and the counter during Program Cycle is illustrated in figure 3.24.

3.4.4.2.1 *Trigger Status Cycle.* One of the command words transmitted to the counter is the Trigger word. The Trigger word defines the triggering parameters to be used by the counter in performing a measurement. There are instances when the computer will have occasion to interrogate the counter for information regarding the triggering parameters presently in use by the counter. For example, the computer might program the counter to operate in "Auto Trigger" mode. The computer can request transmission of the trigger status word by the counter and then use the information transmitted to generate the new counter program instructions. This transfer of operating parameters is a Write operation in that the data flow is toward the computer but it is related to the Read operation in that it includes information concerning operating parameters of the counter. The transfer operation that transmits such information is illustrated in figures 3.25 and 3.26. The format and content of the Trigger Word is the same regardless of whether it is transmitted by the counter as a status word or transmitted by the computer as a command word.

3.4.4.2.2 *Measurement Cycle Timing.* The counter is capable of operating in two modes: microprocessor speed and high speed. It is also capable of operating in two I/O data formats: Parallel and 16-Bit MUX format. Selection of one of these is controlled by a DTDP switch on the interface board (S1). For this reason there are four separate sequences of measurement control and status signals. These timing sequences are illustrated in figures 3.25 and 3.26. Measurement transfer times (not including measurement time) are 25 msec for μprocessor speed, and 50 msec for μprocessor speed with display. In the high speed mode, the first measurement after programming will take 1 ms to be transmitted. Subsequent measurements will take 35 μsec to be transmitted.

									CHANNEL B		CHANNEL A			WORD ID	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNCTION CODE			SIGN →	TIME BASE/ MULTIPLIER VALUE				INPUT COM./SEP.	▽/△	DC/AC	▽/△	DC/AC	1/X / X	0	0

Function code	Bits 15 14 13
FA	= 0 0 0
FC	= 0 0 1
P	= 0 1 0
PA	= 0 1 1
TI	= 1 0 0
TIA	= 1 0 1
TOT	= 1 1 0
A/B	= 1 1 1

SIGN (bit 12): 1 = – ; 0 = +

TIME BASE/MULTIPLIER VALUE (bits 11–8): BCD Format

INPUT (bit 7): 1 = C ; 0 = S

Notes: a. The first word to be programmed after power-on must be a function word.

b. Any arithmetic manipulation of data implies µProcessor speed.

Figure 3.17 - Function Word Format

CHAN	SIGN	TRIGGER LEVEL (See Note 1)										RANGE OR AUTO		WORD ID	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A/B	–/+	1st DIGIT MSB		2nd DIGIT				3rd DIGIT			LSB	RANGE OR AUTO		0	1

CHAN (bit 15): A = 1 ; B = 0

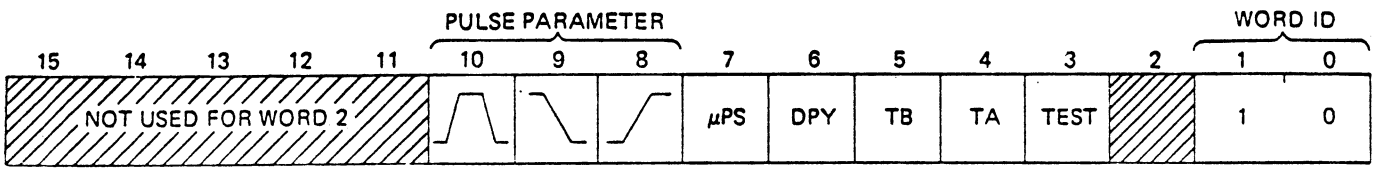
SIGN (bit 14): – = 1 ; + = 0

Range	Bits 3 2
X1	= 0 0
X10	= 0 1
X100	= 1 0
AUTO	= 1 1

Note 1: The first digit of the trigger level portion of the word is only a 2 bit byte and thus can contain only the values 0 thru 3. The 2nd and 3rd digit bytes are 4 bit BCD bytes. The trigger level value is limited to values between –320 and +319.

Note: This format is used for the trigger status word transmitted to the controller and for the trigger command word transmitted to the counter.

Figure 3.18 - Trigger Word Format



Bits 0 and 1 are word ID bits and are always set for word two: bit 0 = 0, 1 = 1.

Bit 2 Not used in word two

Bit 3 when set to 1 causes the counter to go into test mode, e.g., 10 MHz reference signal is measured.

Bits 4 and 5 when set to 1 instruct the counter to output the trigger levels, upon IOX command, when R/W returns high. After trigger status messages are transmitted, the counter will transmit measurement data, in all subsequent measurement cycles.

Note: 6 and 7 are related in that:

bit 6 infers bit 7, e.g., when bit 6 is set to 1 the counter operates at microprocessor speed. Bit 7, however does not infer bit 6, e.g., the counter can be operated at microprocessor speed without display.

Bit 6 when set to 1 selects DISPLAY mode.

Bit 7 when set to 1 selects microprocessor speed.

Bits 8, 9, and 10 mutually exclusive and when set to 1:

a. bit 8 = rise time

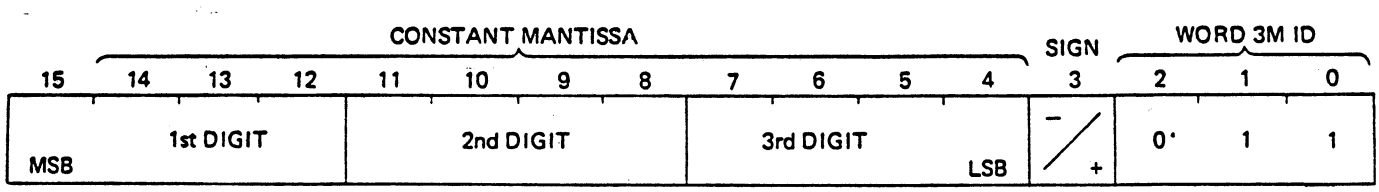
b. bit 9 = fall time

c. bit 10 = pulse width

Note: In order to program bits 8, 9, or 10, the counter must have been previously programmed for TI or TIA functions.

Bits 2 and 11 thru 15 not used in word Two.

Figure 3.19 - Definition Word Format



May be repeated three times with one constant E word to input a 9 digit number. The number entered will have the following format: $\pm$DDD.DDDDDD x $10^{\pm DD}$.

Figure 3.20 - Constant M Word Format

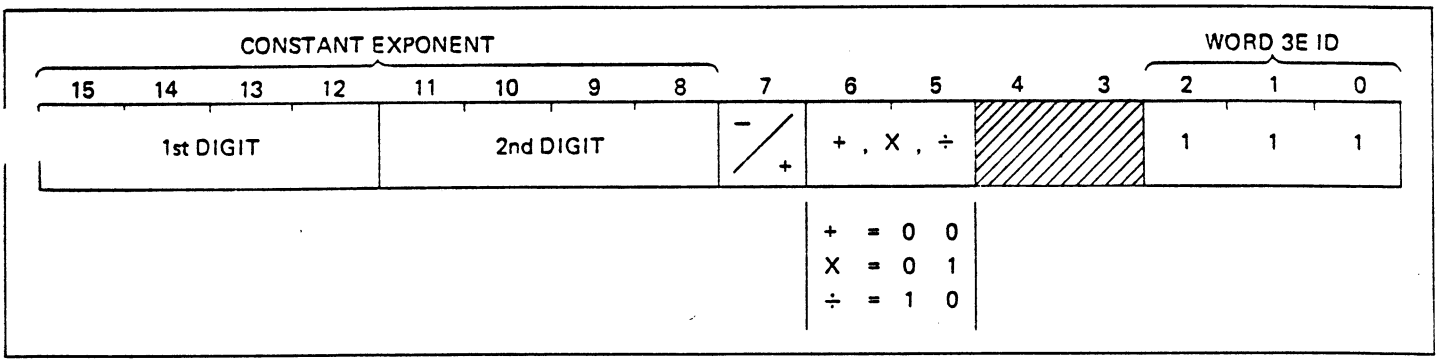


Figure 3.21 - Constant E Word Format

Table 3.10 - Option 56 Pin Description (Parallel Mode)

Jack & Pins	Signal Description
J211 1 – 16	Input lines, instruction lines from computer for programming counter functions
J211 17 – 20†	LSD of exponent
J211 21 – 24†	MSD of exponent
J211 25	Exponent sign
J211 26	Mantissa sign
J211 27	Overflow
J211 28 – 31†	Data 9th digit (least significant)
J211 32 – 35†	Data 8th digit
J211 36 J212 1 – 3 †	Data 7th digit
J212 4 – 7 †	Data 6th digit
J212 8 – 11†	Data 5th digit
J212 12 – 15 †	Data 4th digit
J212 16 – 19 †	Data 3rd digit
J212 20 – 23 †	Data 2nd digit
J212 24 – 27 †	Data 1st digit (most significant)
J212 28	IOX – Input/Output Execute
J212 29	R/W – Read/Write
J212 30	DONE – Operation Complete
J212 31	PRINT – Signal for Low Speed Calculators Only
J212 32	$\overline{\text{TRDY}}$ – Transfer Ready
J212 33	$\overline{\text{HLD}}$ – HOLD *
J212 34	$\overline{\text{REMOTE}}$ – Puts Interface and Counter Under Computer
J212 35	GROUND
J212 36	$\overline{\text{HSP}}$ – High Speed – Overrides any μProcessor speed commands previously given

*Used in High Speed operation only to cause the counter to reset and keep the counter from making a new measurement.

†Denotes most-significant-bit within BCD digit.

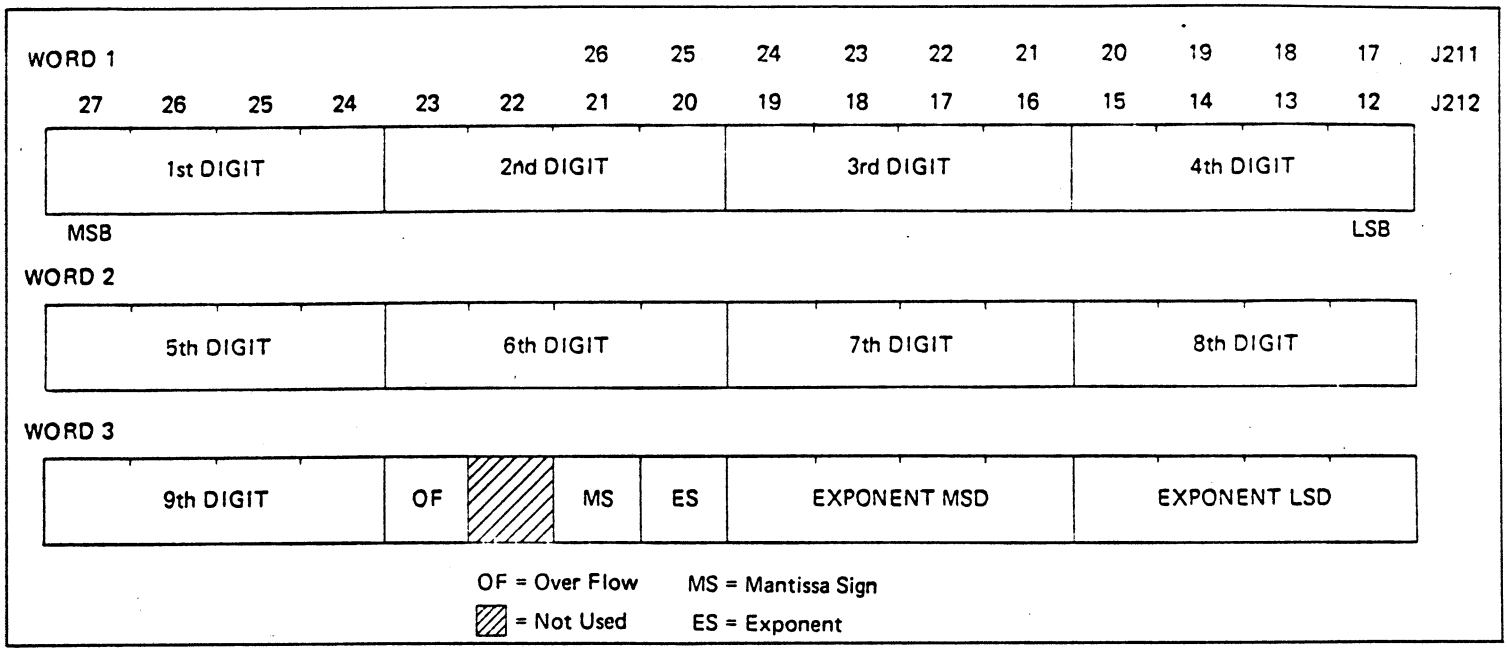


Figure 3.22 - Option 56 Pin Description (16-Bit MUX Mode)

INPUT SIGNAL: TTL CLOCK, 2 MHz FREQUENCY

PROGRAM: FA, 100 MSEC TIME BASE, DC COUPLING, POS. SLOPE
AUTO TRIGGER
TRIGGER LEVEL OUTPUT (CHANN A)
DISPLAY MEASUREMENT

FUNCTION WORD

15	14	13	12	11	10	9	8	7	CHANNEL B 6	5	CHANNEL A 4	3	2	WORD ID 1	0
FUNCTION CODE			SIGN →	TIME BASE/ MULTIPLIER VALUE				INPUT COM. SEP.	⏚/⊓	DC/AC	⏚/⊓	DC/AC	1/X/X	0	0
0	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0

TRIGGER WORD

CHAN 15	SIGN 14	13	12	11	10	9	8	7	6	5	4	3	2	WORD ID 1	0
A/B	−/+	1st DIGIT MSB		2nd DIGIT				3rd DIGIT LSB				RANGE OR AUTO		0	1
1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

DEFINITION WORD

15	14	13	12	11	PULSE PARAMETER 10	9	8	7	6	5	4	3	2	WORD ID 1	0
NOT USED FOR WORD 2					⊓	⊔	⊓	µPS	DPY	TB	TA	TEST		1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

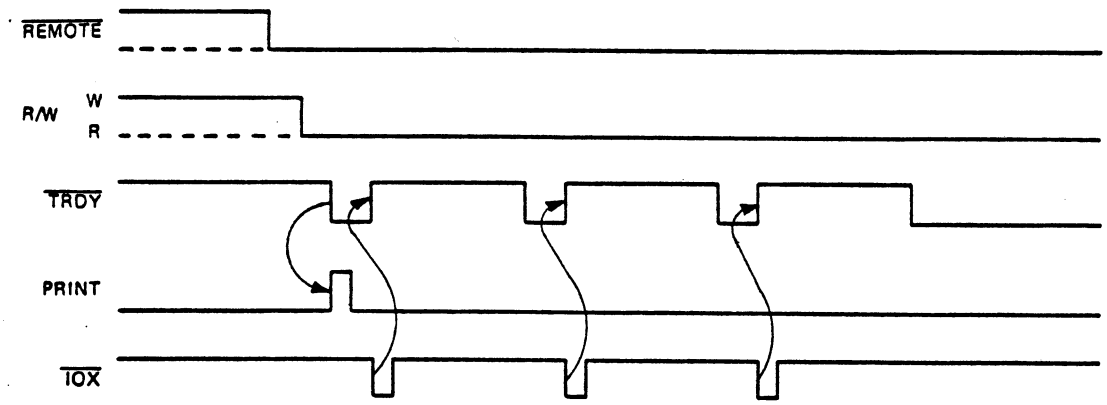
Figure 3.23 - Command Word Sequence Example

Table 3.11 - Control Signal Functions

Mnemonic	Description and Function
$\overline{\text{REMOTE}}$	REMOTE. This signal is set low when the computer is to control the operation of the counter.
R/W	READ/WRITE. Instructs the counter to prepare to make measurements (when set high) or to prepare to receive programming command words (when set low) upon receipt of the INPUT/OUTPUT EXECUTE (IOX) control signal.
IOX	INPUT/OUTPUT EXECUTE R/W Low: negative going IOX signal indicates to the counter that the computer has placed a 16-bit programming command word on the bus and that the counter is to read-in the command. R/W High: instructs the counter to make a new measurement and make the measurement data available on the bus. In Parallel mode, the counter will make the measurement and place the measurement data on the 47-bit data bus. The counter then lowers the $\overline{\text{DONE}}$ status line. In 16-Bit MUX mode, the counter will make the measurement and place the first 16-bit byte of measurement data on the 16-bit data bus. After the computer accepts the first byte the counter places the next byte on the bus. This is repeated until all measurement data has been multiplexed in three bytes to the computer. The counter then lowers the DONE status line.
$\overline{\text{HSC}}$	HIGH SPEED CONTROL. A low level on this signal line will cause the counter to send unprocessed measurement data at the high speed transfer rate regardless of previous program command instructions, i.e., front panel display or arithmetic manipulation. To use this feature the R/W line must be set to the READ (low) condition before the $\overline{\text{HSC}}$ is changed. The R/W line is then returned to the WRITE (hi) condition and the counter will operate at the high speed. Instructions are not destroyed however, and the counter may be returned to the microprocessor speed (and function) by setting R/W low, returning the $\overline{\text{HSC}}$ to high and then setting the R/W back to high.
$\overline{\text{HLD}}$	HOLD. This signal resets the counter and initiates a new measurement. It must appear only after a TRANSFER READY (TRDY) or PRINT signal has been transmitted.

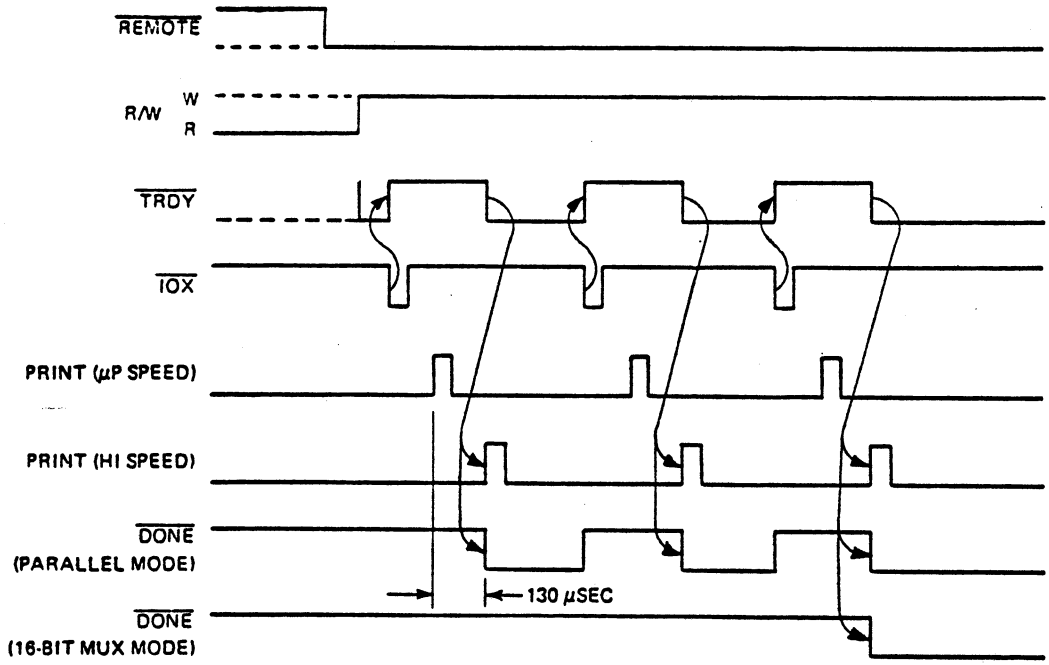
Table 3.10 - Status Signal Functions

Mnemonic	Description and Function
$\overline{\text{TRDY}}$	TRANSFER READY. Indicates to the computer that the counter is ready to transfer data to or from the computer. This signal has three discrete meanings depending upon the R/W mode and the interface format configuration: READ mode (R/W low, regardless of format) setting the $\overline{\text{TRDY}}$ line low indicates to the computer that the counter is ready to transfer a program instruction into the counter. WRITE mode (R/W high) in Parallel format operation the counter sets the TRDY line low to indicate that a measurement has been taken and the data is available at the 47-bit bus. WRITE mode (R/W high) in 16-bit MUX format operation the counter sets the TRDY line low to indicate that a 16-bit byte of information is available at the 16-bit I/O bus lines.
$\overline{\text{DONE}}$	DONE. A low level signal on this line indicates to the computer that a complete measurement data transfer has been completed. In the Parallel mode the DONE signal occurs simultaneously with the TRDY signal. In the 16-Bit MUX mode the DONE signal occurs after the last 16-bit byte of measurement data has been placed on the I/O lines.
PRINT	PRINT. This signal is a 5 μsec positive-going pulse provided for use with the slower machines such as calculators and printers. It has the same meaning as the TRDY signal but the timing within the high speed interface is such that the PRINT signal should not be used in high speed minicomputer applications. See figure 4.39 and note the difference in timing between TRDY and PRINT. This time difference exists only in the microprocessor speed mode.



$\overline{\text{Remote}}$	Line must be down at all times when the computer has control of the counter
R/W	Goes low to indicate to counter that the following operation is programming
$\overline{\text{TRDY}}$	Counter signals "Transfer Ready" to computer
Print	In the read mode print appears coincident with the first $\overline{\text{TRDY}}$ after R/W goes low
$\overline{\text{IOX}}$	Must only be given when $\overline{\text{TRDY}}$ is low. It indicates to counter that a programming word is present at the input lines.

Figure 3.24 - Read Mode Handshake Timing



$\overline{\text{REMOTE}}$	Must be low at all times when the computer has control of the counter
R/W	Low indicates that a measurement is being called for by the computer
$\overline{\text{IOX}}$	Commands the counter to update measurement data
$\overline{\text{TRDY}}$ or PRINT	Indicates data is available at the interface
$\overline{\text{DONE}}$	Indicates that a complete measurement has been made available at the interface.

Figure 3.25 - Write Mode Handshake Timing

1 ;ER LEVEL CHAN A

CHAN 15	SIGN 14	13	12	11	10	9	8	7	6	5	4	3	2	WORD ID 1	0
A / B	− / +	1st DIGIT MSB		2nd DIGIT				3rd DIGIT			LSB	RANGE OR AUTO		0	1
1	0	0	0	0	0	1	0	0	1	0	1	0	1	0	1

1st WORD OF MEASUREMENT DATA

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	
1st DIGIT				2nd DIGIT				3rd DIGIT				4th DIGIT				J211
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	J212

'nd WORD OF MEASUREMENT DATA

5th DIGIT				6th DIGIT				7th DIGIT				8th DIGIT			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

3rd WORD OF MEASUREMENT DATA

9th DIGIT				OF		MS	ES	EXPONENT MSD				EXPONENT LSD			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 3.26 - Output Word Sequence Example

SECTION 4 APPLICATIONS

4.1 INTRODUCTION.

4.1.1 This section contains system operating examples for the Series 9000A timer/counter. Each example contains a statement of purpose, a sample program string and the device dependent message required to program the instrument for the particular application. These examples were prepared using a Hewlett-Packard 9825 calculator connected to the Racal-Dana Series 9000A through the IEEE-STD-488-1978 Standard Interface. Each example contains a program listing as printed by the calculator along with an explanation for each line of the program. If the 9000A is to be used with a Hewlett-Packard Model 9825 calculator the programming presented in this section may be used directly and/or further modified to suit the users needs. Because the Series 9000A may be used with any controller which operates on the standard interface bus the user may wish to prepare equivalent software for another controller device. In such a case the user should review the remote operating instructions contained in Section 3 of this manual to select and assemble appropriate operating statements for his controller which cause the transmission of the required interface messages and device dependent messages.

4.1.2 For example, in the first program sample in this section, line zero of the program is `rem 7` and the accompanying explanation indicates that this statement on the Hewlett Packard 9825 calculator sends the remote message to all devices on the bus. This statement causes the calculator to lower the REN line thus arming the counter for remote operation.

4.1.3 Referring again to the first example note that line 1 of the program printout contains the statement `fli 6` and that the accompanying explanation indicates that this sets the floating decimal format. This may or may not be a feature or function of the controller in use and since it is not an interface or device dependent message use of an equivalent is at the discretion of the user. Line 2 of the program shows the statement `wrt 702`. The explanation indicates that this transmits the device listen address 02. The user should select the statement for his controller which causes it to transmit the listen address assigned to the counter. Instructions for the address assignment of the Series 9000A are presented in paragraph 3.3.5. Table 3.26 shows the address switch setting, the talk and listen address characters and data line binary code for each available decimal address of the instrument.

4.1.4 Line 2 of the example also contains the program string which is composed of the device dependent messages. The device dependent message is the primary subject to which this section of the manual addresses itself. The examples contained in this section are presented primarily to show the various combinations of device dependent messages used to accomplish the various remotely controlled measurement operations. Note that the program printout indicates the string of device dependent messages presented in the table directly above the program tape. This format is maintained throughout the section and thus the user may use this section conveniently by referring to the device dependent message string shown for each system operation example.

4.1.5 Line 3 of the program shown in the example is the reply subroutine of the program and instructs the counter to become a talker and transmit the measurement data. Line 3 also instructs the calculator to store the measurement data transmitted by the counter in a storage register known as "Variable A" and subsequentially to print the value in Variable A on the program tape. The final line on the program printout is the measurement value `2.713534e 07` the answer 27.13534 MHz.

Purpose: Remotely program the FA function to measure 27.135 MHz transmitter frequency

9000A Program String: F0G-1A2C0LAA

Device Dependent Messages

Device Code	Parameter
F0	Frequency A
G-1	Range 5 (10 Hz)
A+D	A DC Coupling, pos slope
C0	Separate inputs
LAA	Channel A Auto Trigger

```
0: rem 7;clr 700

1: flt 6

2: wrt 702;

                "F0G-
 1A+DC0LAA"

3: red 702;A;

4: prt A
*26744


2.713534e 07
```

Sends Remote message to all devices on the bus and send device clear to 9000A counter.

Sets floating decimal (scientific notation) format. Six places to the right of the decimal. i.e. X.XXXXXXeXX

Address device 02 (9000A) as a listener.

Writes a device dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (9000A).

Address device 02 (9000A) as a talker. Reads values into variable A from device 02 (9000A).

Prints the value stored in variable A.

Answer: 27.13534 MHz

Purpose Remotely program the FC function to measure a 147.09 MHz transmitter frequency.

9000A Program String F1G-1

Device Dependent Messages

Device Code	Parameter
F1 G-1	Frequency C 10 Hz Resolution

```
0: rem 7;clr 700
1: flt 9

2: wrt 702;
   "F1G-1"
3: red 702;A;

4: prt A
*1087


  1.470901500e 08
```

Send Remote message to all devices on the bus and send clear device 700 (9000A).

Sets floating decimal point (scientific notation) nine places to the right of the decimal. i.e. X.XXXXXXXXXeXX

Address device 02 (9000A) as a listener.

Writes a device.dependent message, 9000A program string, followed by a (CR) Carriage Return and (LF) Line Feed to device 02(9000A).

Address device 02 (9000A) as a talker. Reads values into specified variable (A) from device 02 (9000A).

Prints the value stored in variable A.

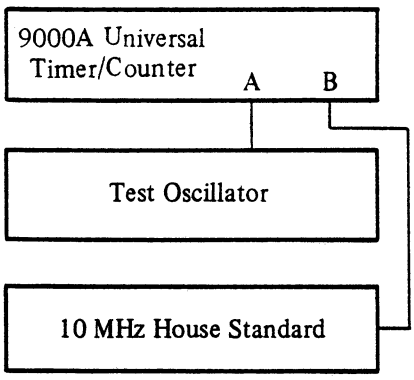
Answer: Transmitter frequency 147.0915 MHz.

Purpose: Remotely program the A/B Ratio function to check the calibration of a test oscillator against a 10 MHz house standard.

9000A Program String F7G+6A+AB+AC0LAALBAH1

Device Dependent Messages

Device Code	Parameter
F7	B/A Ratio Function
G+6	Range 6
A+A	AC Coupling channel A
B+A	AC Coupling channel B
C0	Separate inputs
LAA	Auto trigger A
LBA	Auto trigger B
HI	Transmit trigger levels




```
0: rem 7;clr 700

1: conv 13,32,
 10,44

2: wrt 702,

              "F7G+
 6A+AB+ALAALBAH1"

3: red 702,P,L,M

4: fxd 6;prt "A/
 B=",M

5: M*1e7→E;flt
 4;prt "F=",E

6: fxd 2;prt
 "LA=",P

7: prt "LB=",L
*27464


A/B=      0.050928

F=     5.0928e 05

LA=           0.00

LB=           0.00
```

Sends Remote message to all devices on the bus and send clear device 700 (9000A).

Cancels any previously sent conversion table and converts CR (Carriage Return) to a SP (Space) and LF (Line Feed) to a , (Comma).

Address device 02 (9000A) as a listener.

Writes a device dependent message (9000A program string) followed by a CR (Carriage Return) and LF (Line Feed) to device 02 (9000A).

Address device 02 (9000A) as a listener. Writes a device dependent message (9000A program string) followed by a CR (Carriage Return) and LF (Line Feed) to device 02 (9000A).

Sets fixed decimal format, 6 places after the decimal. Prints the characters A/B (RATIO) and the value stored in variable B.

Multiplies the value stored in variable B (ratio of channel A and B) by 1e7 (10 MHz house standard) to obtain frequency of test oscillator and stores that value in variable E.

Sets floating decimal point (scientific notation) format, 4 places to the right of the decimal. i.e. X.XXXXeXX

Prints the characters F= and the value stored in variable E.

Ratio of the oscillators = 0.050928

Frequency of the test oscillator = 509.28 KHz.

Trigger level of channel A.

Trigger level of channel B.

Purpose: Remotely program the Time Interval function to measure the pulse width of a T^2L 1 Hz clock at the two volt level.

9000A Program: F4G-8A+DB–DLA+2.00
LB+2.00

Device Dependent Messages

Device Code	Parameter
F4	Time interval
G-8	10ns res
A+D	Channel A + Slope
B1	Channel A DC Coupling
B–D	Channel B – Slope
B2	Channel B DC coupling
C1	common input
LA+2.00	Trigger level A+2.00V
LB+2.00	Trigger level B+2.00V

```
0: rem 7;clr 700

1: flt 5


2: wrt 702,

              "F4G-
 8A+DB-DLA+2.00L
 B2.00"

3: red 702,A

4: prt "TI=",A
*16183



TI=     4.98662e-1
```

Sends Remote Enable message to all devices on the bus and send clear device 700 (9000A).

Sets floating decimal (scientific notation) format. Five places to the right of the decimal. i.e. X.XXXXXeXX

Address device 02 (9000A) as a listener.

Writes a device dependent message (9000A program string) followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (9000A).

Address device 02 (9000A) as a talker. Reads values into specified variables (A) from device 02 (9000A).

Prints the characters TI= and the value stored in variable A.

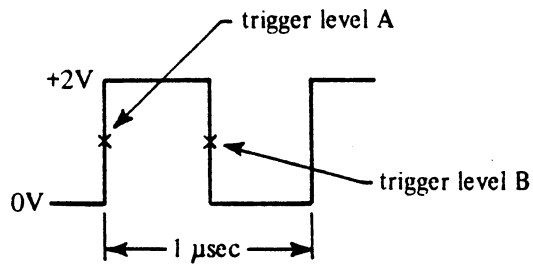
Answer: Time interval = .498662 sec.

Purpose: Measure the Pulse Width of a 2V 1 MHz clock @ the 50% point using time interval average for greater resolution.

9000A Program String: F5G+5M2

Device Dependent Messages

Device Codes	Parameter
F5	Time Interval Average
G+5	10e5 Samples
M2	Pulse Width Command




```
0: rem 7;clr 700
1: flt 6
2: wrt 702,
              "F5G+
 5M2"
3: red 702,A;
4: prt A
*14240

     4.733907e 00
```

Sends Remote message to all devices on the bus and send clear device 700 (9000A).

Sets floating decimal (scientific notation) format. Six places to the right of the decimal. i.e. X.XXXXXXeXX

Address device 02 (9000A) as a listener.

Writes a device dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (9000A).

Address device 02 (9000A) as a talker. Reads values into variable A from device 02 (9000A).

Prints the value stored in variable A.

Answer: .4733907 µsec

Purpose: Measure number of noise spikes occuring on a 5 volt power supply line over a 3 second interval

9000A Program String F6A+DCOLA+05.5J2S
S

Device Dependent Messages

Device Codes	Parameter
F6	Totalize
A+D	Channel A + Slope Channel A DC coupling
CO	Separate Inputs
LA+05.5	Trigger level 5.5V in the 10V range
J2	Arm counter to initiate measurement
S	Start/Stop

```
0: rem 7;clr 700
1: fxd 0
2: wrt 702,
                "F6A+
 DC0LA+05.5J2S"


3: wait 3000
4: wrt 702,"S"



5: red 702,A
6: prt A
*15124


                 20
```

Send Remote message to all devices on the bus and send clear device 700 (9000A).

Sets fixed decimal format (no trailing decimals).

Address device 02 (9000A) as a listener.

Writes a device dependent message, followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (9000A).

NOTE: The first S opens the measurement gate.

Commands the controller to wait 3 sec before proceeding to the next step.

Address device 02 (9000A) as a listener and writes a device dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (9000A).

NOTE: The second S closes the measurement gate.

Address device 02 (9000A) as a talker. Reads values into variable A from device 02 (9000A).

Prints the value stored in variable A.

Answer: 20 noise spikes

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REPAIR REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline and include a copy with your instrument to be sent to your local Racal-Dana repair facility.

Model Number _____ Options _____ Date _____

Serial Number _____ P. O.# _____

Company Name _____

Address _____

City _____ State _____ Zip Code _____

Contact _____ Phone Number _____

1. Describe, in detail, the problem and symptoms you are having.

_____

_____

2. If you are using your unit on the bus, please list the program strings used and the controller type, if possible.

_____

_____

3. List all input levels, and frequencies this failure occurs.

_____

_____

4. Indicate any repair work previously performed.

_____

_____

5. Please give any additional information you feel would be beneficial in facilitating a faster repair time. (I. E., modifications, etc.)

_____

_____

PUBLICATION NO. 980537

MAINTENANCE MANUAL

9000A

MICROPROCESSING TIMER/COUNTERS

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PUBLICATION DATE: JULY 1986

WARRANTY

Within one year of purchase, Racal-Dana will repair or replace your instrument, at our option, if in any way it is defective in material or workmanship. The instrument must be returned to the country of purchase, unless prior arrangement has been made, and Racal-Dana Instruments will pay all parts and labor charges. Just call Racal-Dana Customer Service at (714) 859-8999 in U.S.A., Windsor (0753) 868101 in England, (1) 3-955-8888 in France, 06102-2861/2 in Germany or (02) 5062767, 5062686, or 503444 in Italy for assistance. We will advise you of the proper shipping address for your prepaid shipment. Your instrument will be returned to you freight prepaid.

PROPRIETARY NOTICE

FOR YOUR SAFETY

Before undertaking any maintenance procedure, whether it be a specific troubleshooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the **WARNING** and **CAUTION** notices contained therein.

The equipment described in this manual contains voltage hazardous to human life and safety and which is capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical hazards and thus prevent personal injury and damage to equipment.

If this instrument is to be powered from the AC line (mains) through an autotransformer (such as a Variac or equivalent) ensure that the common connector is connected to the neutral (earthed pole) of the power supply.

Before operating the unit ensure that the protective conductor (green wire) is connected to the ground (earth) protective conductor of the power outlet. Do not defeat the protective feature of the third protective conductor in the power cord by using a two conductor extension cord or a three-prong/two-prong adaptor.

Maintenance and calibration procedures contained in this manual sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures carefully and heed Warnings to avoid "live" circuit points to ensure your personal safety.

Before operating this instrument:

1. Ensure that the instrument is configured to operate on the voltage available at the power source. See Installation Section.

2. Ensure that the proper fuse is in place in the instrument for the power source on which the instrument is to be operated.

3. Ensure that all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If at any time the instrument:

- Fails to operate satisfactorily
- Shows visible damage
- Has been stored under unfavorable conditions
- Has sustained stress

It should not be used until its performance has been checked by qualified personnel.

ERRATA SHEET

July 1986

The following Racal-Dana Model 9000A part numbers have new FSC numbers and/or new manufacturers part numbers:

Racal-Dana Part Number	FSC	Manu P/N
100017	56289	1C25Z5U103M100E
100024	56289	1C25Z5U104M050E
110125	05397	T355C225M035AS
110126	05397	T355F685M035AS
110141	05397	T355F226M016AS
110143	05397	T355A105M035AS
110151	05397	T354G106M035AS
130103	72982	GR42-6X7R103M05Y
210074	50434	HPQDSP-411S
210079	50434	HLMP-3401
600805	79727	G-127-L-3/G-20-59
110174 (9100 MFD SUBSTITUTE)	00853*	066/HS/912/0015B
	*00853	SANGAMO ELECTRIC CO. PICKENS, SC

ADDENDUM

December 12, 1984

THIS ADDENDUM REPLACES THE EXISTING REFERENCE MULTIPLIER CIRCUIT

TO THE 9000A TIMER/COUNTER

4.4.5 Reference Multiplier Circuit

4.4.5.1 The reference multiplier circuit converts the internal reference oscillator (10 MHz) or an external reference (1.5, 1, 5, or 10 MHz) to a 100 MHz reference signal, used as the timing standard for all measurement functions except A/B and TOTALIZE.

4.4.5.2 The circuitry, shown in block form in Figure 4.15, consists of signal shaping circuit, 10 MHz filter, signal detector, phase detector comparator, loop filter, voltage-controlled oscillator, divide by 10 prescaler and ECL to TLL Converter.

4.4.5.3 The signal shaping circuit and the 10 MHz filter are in operation only when an external reference is used. With an external reference of 1 volt RMS (–0, +50%) at 1 MHz, 5 MHz, or 10 MHz applied, the signal shaping circuit converts the input into a squarewave of the same frequency. The shaping circuit consists of an inverter, biased to operate in the class A mode, driving two inverters, connected as a Schmitt trigger. This drives a standard TTL logic level inverter, the output of which is fed to the 10 MHz filter.

4.4.5.4 The 10 MHz filter is an active ringing circuit, consisting of transistors Q1, Q2, and 10 MHz crystal Y1. The square wave output of the shaping circuit is differentiated and the negative spikes from the differentiated signal applied to the base of Q1. The emitter of Q1 drives one side of Y1 (operating in the series mode) causing the crystal to ring at 10 MHz. The collector of Q1 in conjunction with capacitor C8 effectively neutralizes case capacitance of the crystal. The output end of the crystal drives Q2 wired as a common emitter, tuned collector amplifier. The 10 MHz output of the filter is applied to the signal detector/gate. The signal detector/gate circuit is controlled by, and when energized routes through the gate, the output of the 10 MHz filter. In its passive state (no external reference input applied) the gate routes the internal reference oscillator output (10 MHz) through the gate.

4.4.5.5 The gate, shown simplified in Figure 4.16, consists of two differentially coupled transistors (Q3 and Q4) and three segments of a quad dual input Nand gate (U2). Because of the additional diode drop (CR3) between ground and the base of Q4, Q4, is biased off and Q3 is biased on when no signal is received from the filter. The logic low output of Q3 is inverted by U2-6, producing a REF LITE logic high (signifying no external reference signal) and biasing U2-13 on, permitting the 10 MHz from the internal reference oscillator to pass through U2-11. The logic high output of Q4 biases U2-1 high, allowing the 10 MHz output of U2-11 to pass through U2-3 to the PLL multiplier. The same signal is inverted by U2-8 and routed to other circuitry and to the rear panel REFERENCE OUT.

4.4.5.6 When a 10 MHz signal is received from the 10 MHz filter circuit, the signal is clipped by CR2 and CR3 and drives the base of Q4. The collector of Q4, is an inverted square wave of the input signal and is applied to one of Nand gate U2-1. The input signal is also coupled through the emitter of Q4-Q3 to the collector of Q3. The signal is inverted by U2-6 to produce a logic low on the REF LITE line (the EXT REF lamp on the front panel lights) through Nand gate U2-11. The output of U2-11 is logic high enabling the 10 MHz signal from the collector of Q3 to pass through U2-3. As in the case of the switch in the passive mode, the 10 MHz from the output of U2-3 is fed to the PLL Frequency Multiplier and is routed to other circuits in the instrument.

4.4.5.7 The PLL frequency multiplier consists of the phase comparator U3; active loop filter configured with U3 Darlington section, Q5, VR1-2, C26, C29 and Z1 resistor array; 100 MHz VCO (voltage controlled oscillator) U5, in association with CR6, C34 and C30; divide by 10 prescaler U4 and ECL to TTL converter Q6 and Q7. The 10 MHz Reference signal generated on the motherboard is applied to the phase detector at U3-1, where it is compared with the 10 MHz feedback signal from the VCO, which is applied to U3 at pin 3. The resulting correction voltage (error voltage) appears at U3-5, the pull-up or U3-10 the pull-down charge amplifiers and it is then routed to the high impedance Darlington pair in the emitter circuit of Q5 the active filter. The filtered DC voltage from the filter network of C26, C29 and 1 K resistors in Z1 is applied to varactor CR6 in the VCO oscillator tank circuit. The oscillator chip U5, with ECL logic format, and LC circuit components generate the 100 MHz Reference for all functions of the counter except A/B and TOTALIZE modes. The 100 MHz ECL Reference continues in the loop to the ECL divider U4 which divides the 100 MHz by 10, then the ECL-TTL converter Q5 and Q7, and the 10 MHz TTL signal is then applied to the phase comparator.

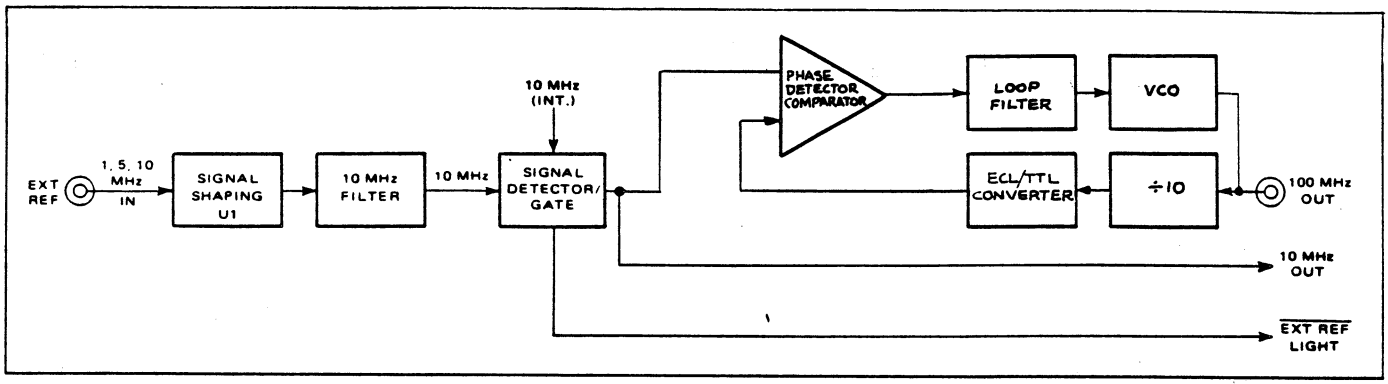


Figure 4.15 - Reference Multiplier Circuit

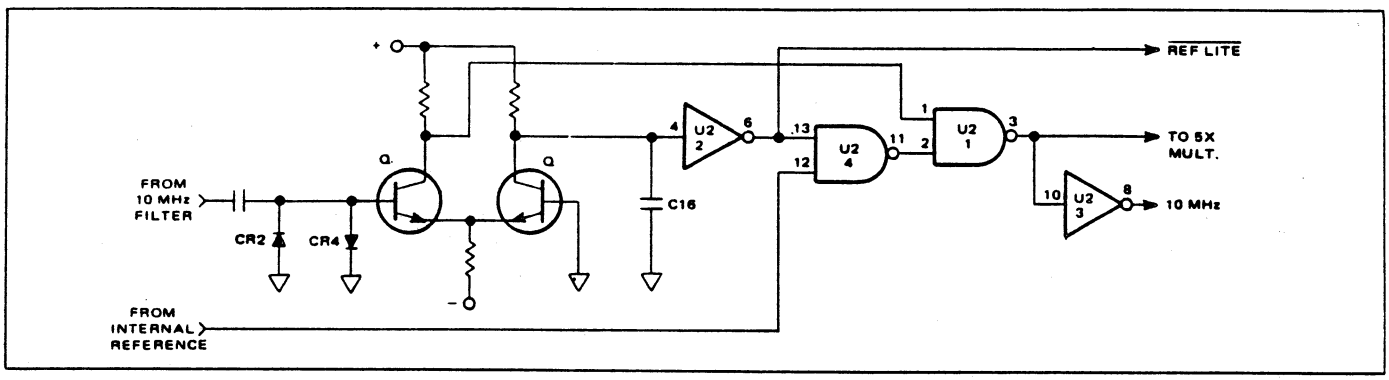


Figure 4.16 - Switch/Gate

5.8.4 Reference Board (Assembly No. 406179)

a. Set counter to FA, TEST, and with an oscilloscope referenced to TP2 (GND), monitor TP1. Adjust C34 until the counter locks up at 100 MHz and provides a reading of 10.000000 MHz. Remember this adjustment position of C34. Refer to alternate figures 5.1 and 5.6 below, and on the next page, as required.

b. Continue to adjust C34 until the counter goes out of lock.

c. Then center C34 between the two points at which the counter locked up. (Assembly and Schematic Drawings for Assy. No. 406179 in this Addendum should be consulted whenever necessary.)

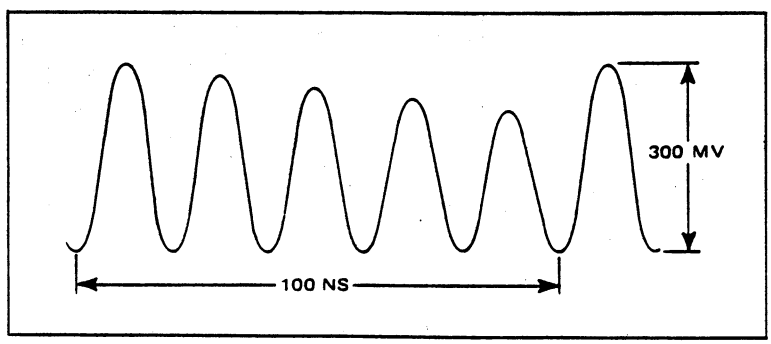


Figure 5.1 - 5th Harmonic Output

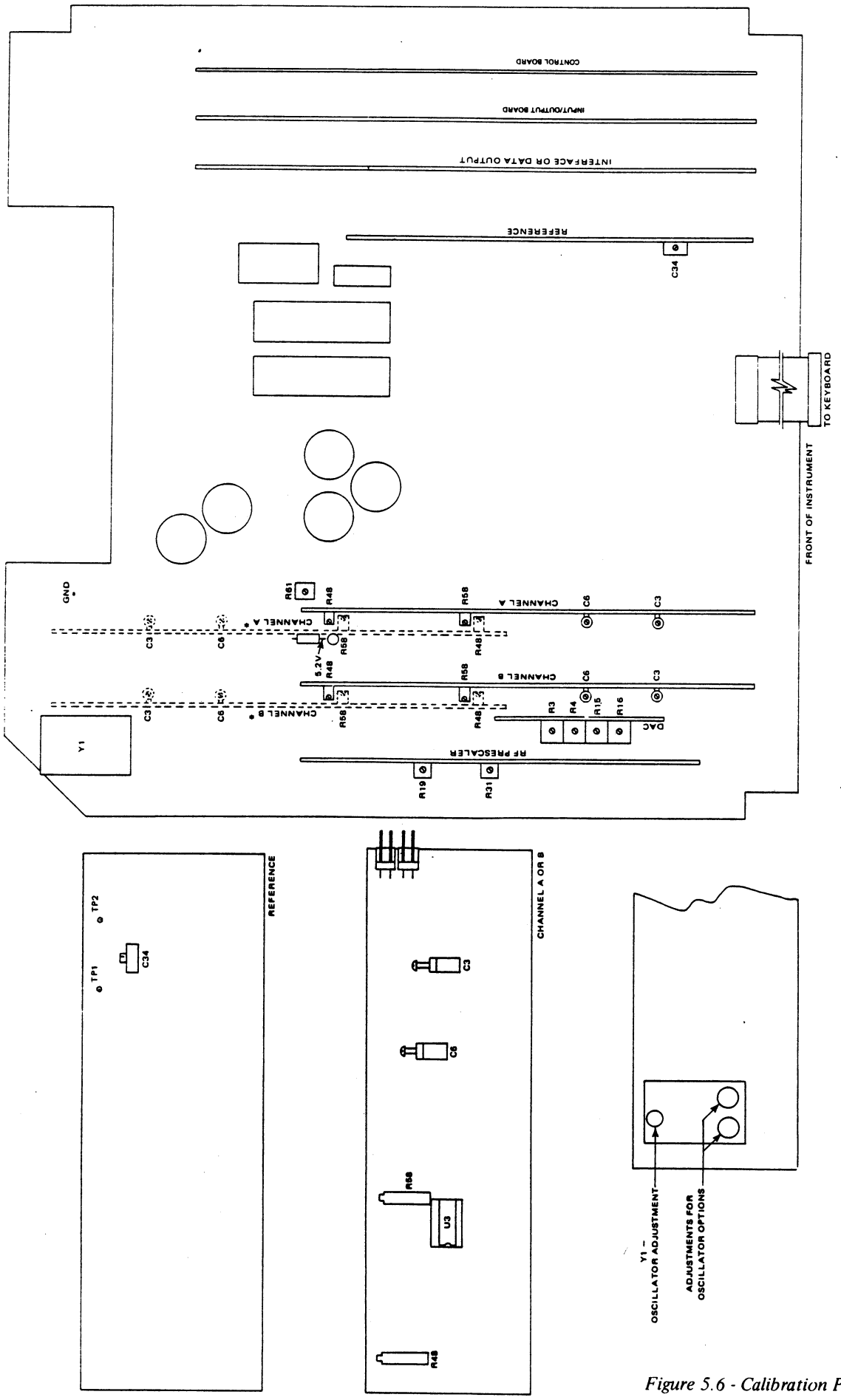
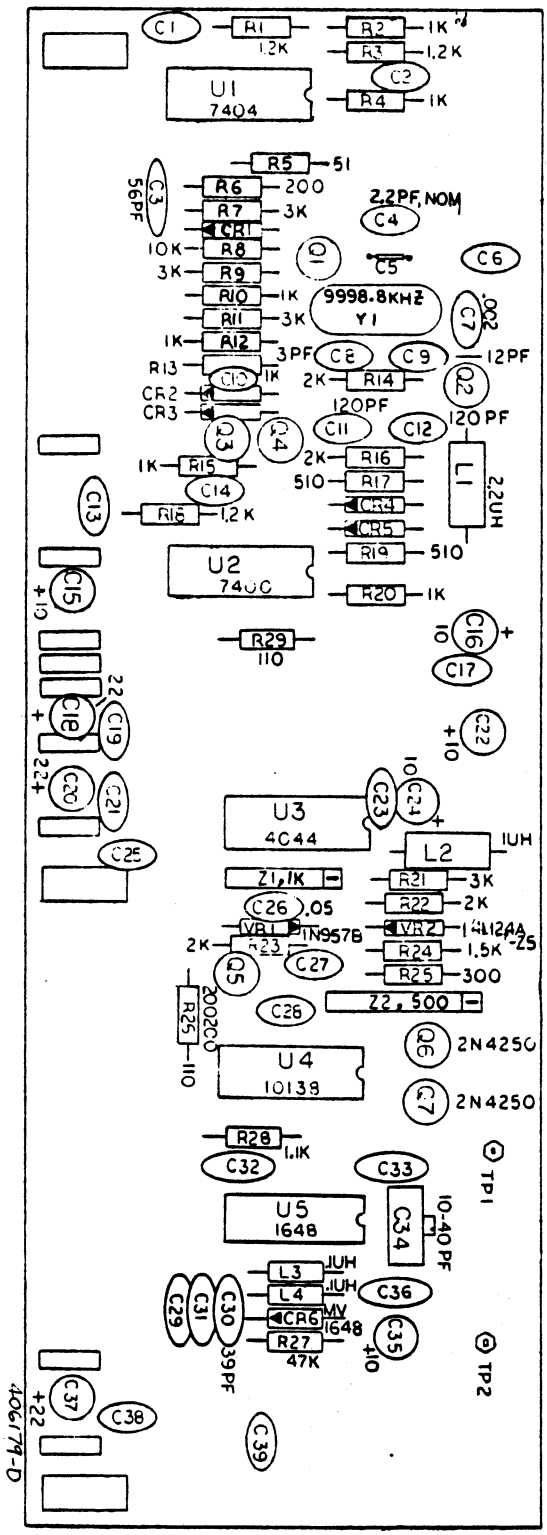
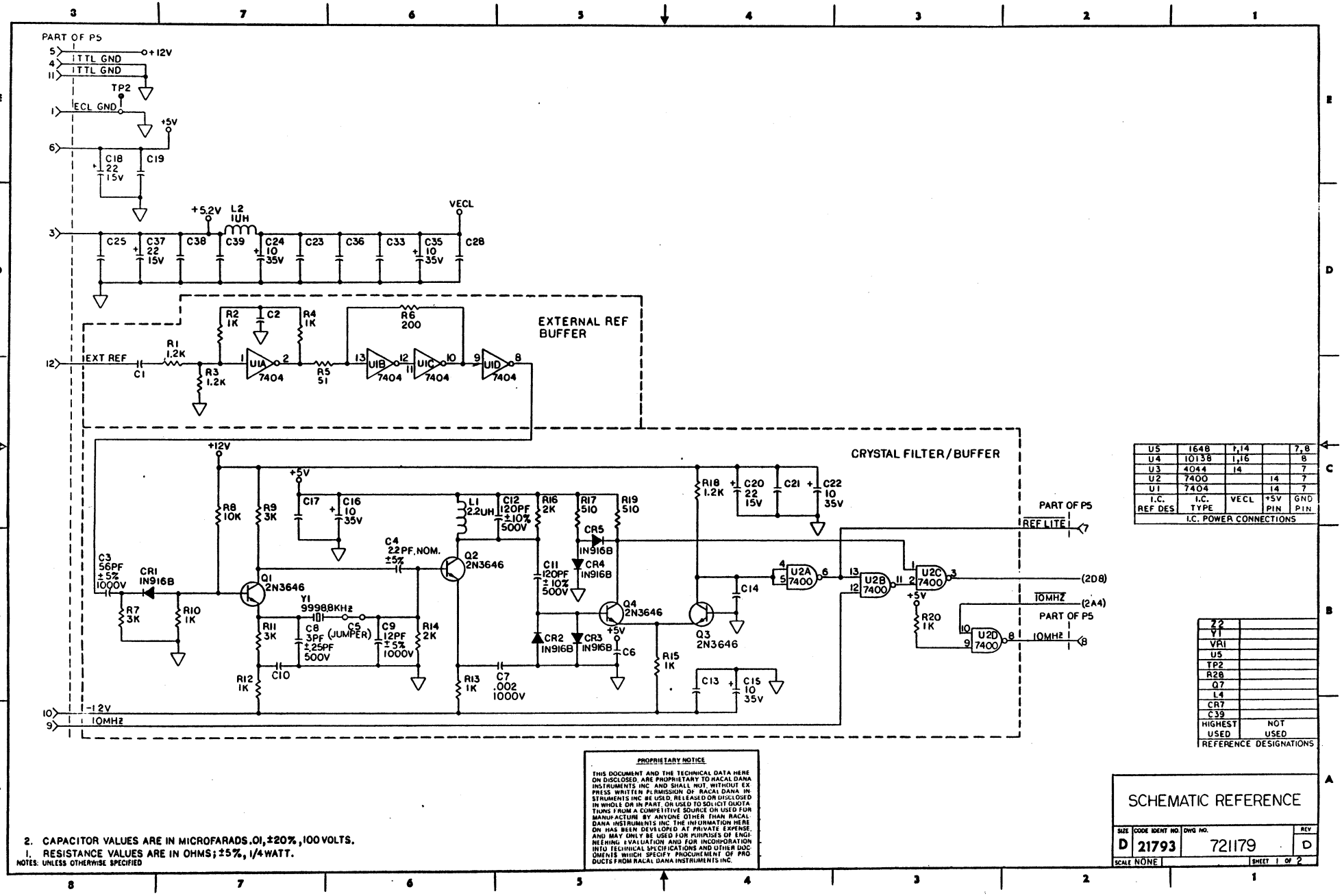


Figure 5.6 - Calibration Points



Replaces Layout, Reference - page 6-20

Schematic on following page
replaces the schematic on page 6-21



U5	1648	7,14		7,8
U4	10138	1,16		8
U3	4044	14		7
U2	7400		14	7
U1	7404		14	7
I.C. REF DES	I.C. TYPE	VECL	+5V PIN	GND PIN

I.C. POWER CONNECTIONS

Z2	
Y1	
VR1	
U5	
TP2	
R28	
Q7	
L4	
CR7	
C39	
HIGHEST USED	NOT USED

REFERENCE DESIGNATIONS

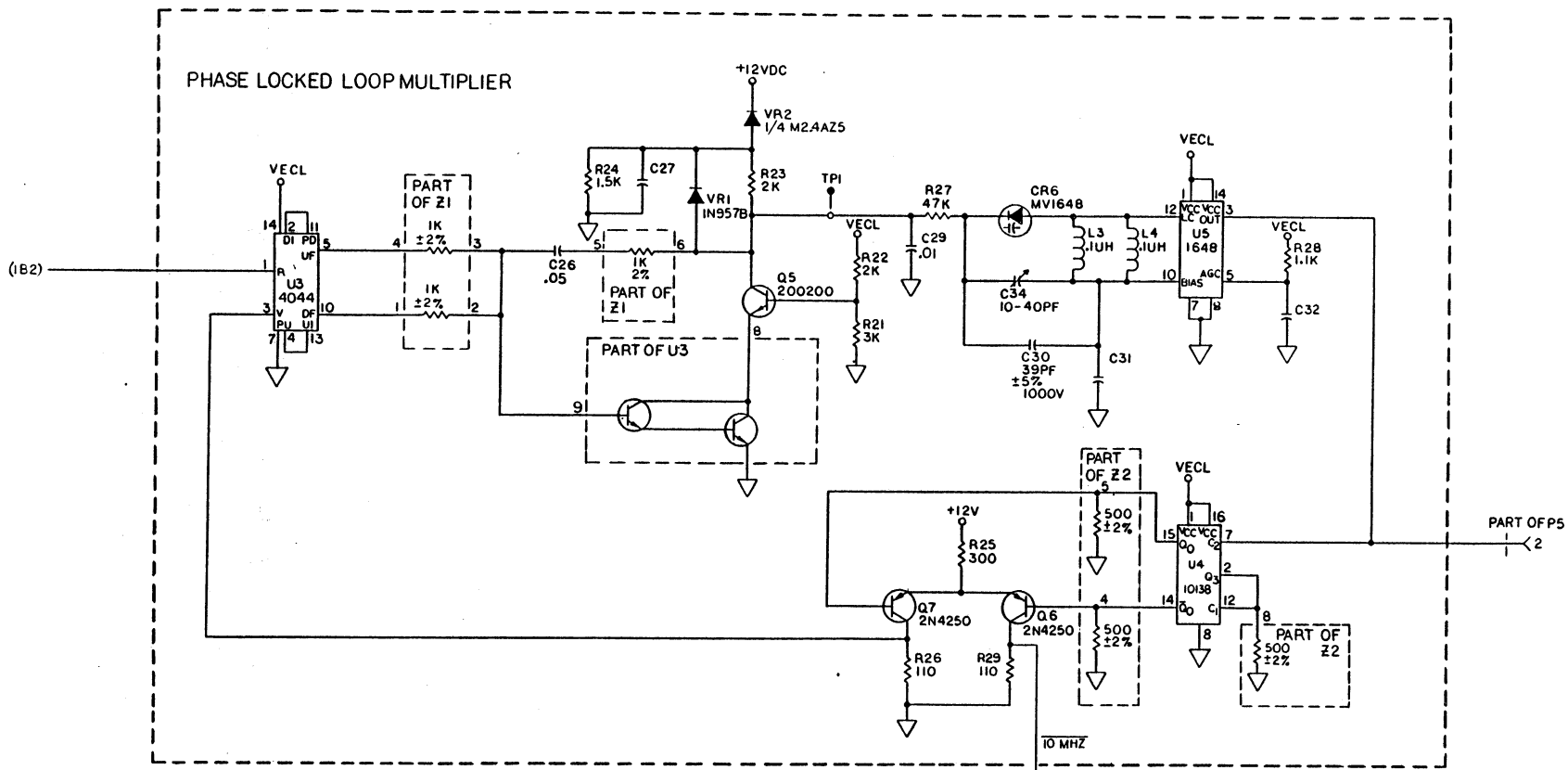
2. CAPACITOR VALUES ARE IN MICROFARADS. 01, ±20%, 100 VOLTS.
1. RESISTANCE VALUES ARE IN OHMS; ±5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC REFERENCE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721179	D

SCALE NONE | SHEET 1 OF 2



NOTES: UNLESS OTHERWISE SPECIFIED

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721179	D
SCALE NONE		SHEET 2 OF 2	

406179 - Assy., PCB, REFERENCE

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	100017	CAP CERAM .0 1 MFD 100V 20%	56289	C023B101F103M
C2	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C3	100053	CAP CERAM 56PFD 100V 5%	56289	C030A102J560J
C4	100050	CAP CERAM 2.2PFD 1000V 5%	56289	C030B102S2R2D
C6	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C7	100019	CAP CERAM .002MFD 1000V 10%	56289	C023B102F202M
C8	100051	CAP CERAM 3PFD 500V	71471	TCD-B1-0
C9	100097	CAP CERAM 12PFD 1000V 5%	56289	C030B102E120J
C10	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C11	100018	CAP CERAM 120PFD 500V 10%	71471	ETCD (N5600)
C12	100018	CAP CERAM 120PFD 500V 10%	71471	ETCD (N5600)
C13	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C14	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C15	110151	CAP TANTA 10MFD 35V 20%	05397	T362C106M035A
C16	110151	CAP TANTA 10MFD 35V 20%	05397	T362C106M035A
C17	100017	CAP TANTA 1MFD 35V 10%	05397	T301A105K035AS
C18	110141	CAP TANTA 22MFD 15V 20%	05397	T368B266M015AS
C19	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C20	110141	CAP ELECT 250MFD 6V	87730	250-6
C21	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C22	110151	CAP ELECT 2000MFD 25V 20%	90201	FP060.2
C23	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C24	110151	CAP ELECT 2000MFD 25V 20%	90201	FP060.2
C25	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C26	100080	CAP CERAM .05MFD 100V 20%	56289	C023A101L503M
C27	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C28	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C29	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C30	100061	CAP CERAM 39PFD 1000V 5%	56289	C030B102G390J
C31	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C32	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C33	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C34	130127	CAP TRIMMER 10-40PFD	52763	300324-52D
C35	110151	CAP ELECT 2000MFD 25V 20%	90201	FP060.3
C36	100017	CAP CERAM .01MFD 100V 20%	05397	C023B10F103M
C37	110141	CAP TANTA 22MFD 15V 20%	05397	T368B226M015AS
C38	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
C39	100017	CAP CERAM .01MFD 100V 20%	56289	C023B101F103M
CR1	211083	DIODE SILICO 1N916B	81349	1N916B
CR2	211083	DIODE SILICO 1N916B	81349	1N916B
CR3	211083	DIODE SILICO 1N916B	81349	1N916B
CR4	211083	DIODE SILICO 1N916B	81349	1N916B
CR5	211083	DIODE SILICO 1N916B	81349	1N916B

406179 - Assy., PCB REFERENCE - Continued

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
CR6	210091	VARACTOR-TUNING DIODE	04713	MV1648
L1	310072	CHOKE RF 2.2μH 10%	99800	1537-20
L2	310068	CHOKE RF 1μH 10%	99800	1537-12
L3	310092	CHOKE RF .1μH 10%	76493	9230-94
L4	310092	CHOKE RF .1μH 10%	76493	9230-94
Q1	200037	TRANS SILICO NPN	80131	2N3646
Q2	200037	TRANS SILICO NPN	80131	2N3646
Q3	200037	TRANS SILICO NPN	80131	2N3646
Q4	200037	TRANS SILICO NPN	80131	2N3646
Q5	200200	TRANS NPN	21793	200200
Q6	200068	TRANS PNP	80131	2N4250
Q7	200068	TRANS PNP	80131	2N4250
R1	000122	RES CARBON 1.2K 5% 1/4W	81349	RC07GF122J
R2	000102	RES CARBON 1K 5% 1/4W	81349	RC07GF102J
R3	000122	RES CARBON 1.2K 5% 1/4W	81349	RC07GF122J
R4	000102	RES CARBON 1K 5% 1/4W	81349	RC07GF102J
R5	000510	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF510J
R6	000201	RES CARBON 200 OHM 5% 1/4W	81349	RC07GF201J
R7	000302	RES CARBON 3K 5% 1/4W	81349	RC07GF302J
R8	000103	RES CARBON 10K 5% 1/4W	81349	RC07GF103J
R9	000302	RES CARBON 3K 5% 1/4W	81349	RC07GF302J
R10	000102	RES CARBON 1K 5% 1/4W	81349	RC07GF102J
R11	000302	RES CARBON 3K 5% 1/4W	81349	RC07GF302J
R12	000102	RES CARBON 1K 5% 1/4W	81349	RC07GF102J
R13	000102	RES CARBON 1K 5% 1/4W	81349	RC07GF102J
R14	000202	RES CARBON 2K 5% 1/4W	81349	RC07GF202J
R15	000102	RES CARBON 1K 5% 1/4W	81349	RC07GF102J
R16	000202	RES CARBON 2K 5% 1/4W	81349	RC07GF202J
R17	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R18	000122	RES CARBON 1.2K 5% 1/4W	81349	RC07GF122J
R19	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R20	000102	RES CARBON 1K 5% 1/4W	81349	RC07GF102J
R21	000302	RES CARBON 3K 5% 1/4W	81349	RC07GF302J
R22	000202	RES CARBON 2K 5% 1/4W	81349	RC07GF202J
R23	000202	RES CARBON 2K 5% 1/4W	81349	RC07GF202J
R24	000152	RES CARBON 1.5K 5% 1/4W	81349	RC07GF152J
R25	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R26	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R27	000473	RES CARBON 47K 5% 1/4W	81349	RC07GF473J
R28	000112	RES CARBON 1.1K 5% 1/4W	81349	RC07GF112J
R29	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J

406179 - Assy., PCB, REFERENCE - Continued

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
U1	230064	IC CERAM	07263/ 01295	7404
U2	230028	IC CERAM	07263/ 01295	7400
U3	230439	IC CERAM MC4044	04713	MC4044
U4	230436	IC QUINARY COUNTER	04713	MC10138
U5	230438	IC MC1648	04713	MC1648
VR1	220049	DIODE ZENER 5%	81349	1N957B
VR2	221177	DIODE SILICO ZENER 1/5W	04713	1/4M2.4A75
Y1	920583	CRYSTAL H33 HOLDER 9.9988 MHz	21793	920583
Z1	080037	RES NETWORK 1K OHMs 1P/6P,3R 2%	11236	750-63-R1KΩ
Z2	080002	RES CERMET 500 OHM NETWORK 8P,7R 2%	11236	750-81-R500Ω

ADDENDUM

November 1, 1984

THIS ADDENDUM ADDS RACAL OVEN OSCILLATORS,

OPTION 22A or 24A, TO THE 9000A TIMER/COUNTER

1. GENERAL

1.1 The Racal Oven Oscillator generates a precise sine wave frequence of 5 MHz as the fundamental reference for multiplier applications. The oven oscillator's controlled environment of 60 degrees centigrade generates a stability of 3×10^{-9} for Option 22A and 3×10^{-10} for option 24A per degree centigrade. The 5 MHz sine wave is modified to a square pulse, then doubled to 10 MHz and routed to the 100 MHz Reference Multiplier section.

2. THEORY OF OPERATION

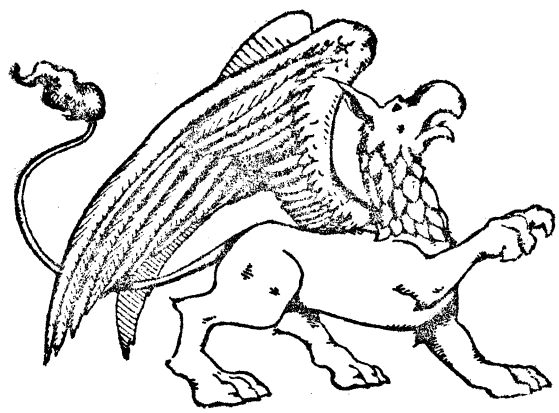
2.1 The oven oscillator, labelled Y1 on the oscillator reference multiplier drawing shown in Figure 1, applies the 5MHz sine wave through C3-R2 to the squaring amplifier. The squaring amplifier, UC2, operates in class A current mode, and buffers the oven oscillator output signal to reduce oscillator loading. The diodes CR1 and CR2 with U2C convert the sine wave to symmetrical squares with a TTL format at 5 MHz pulse. The 5 MHz signal is conditioned by inductor L1 for high frequencies, then buffered through U2A and routed to the dual one-shot multivibrator (OSM) U1A-U1B.

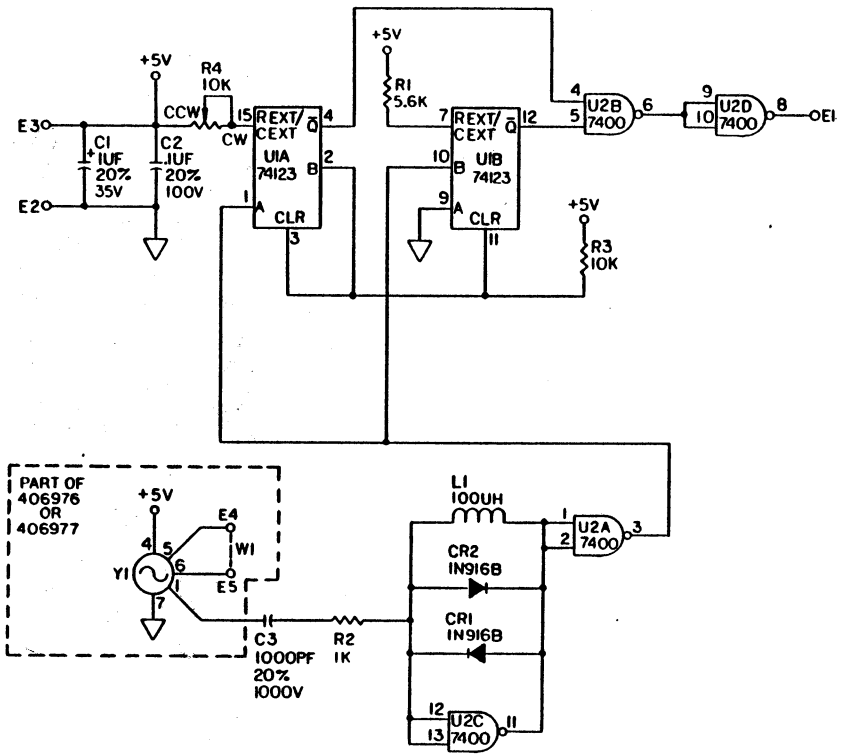
2.2 The dual OSM is configured to generate a 10 MHz pulse with 50% duty cycle. The duration of the pulse or pulse width is determined by R1 and R4. By design, U1A will trigger on falling pulse edge and U1B will trigger on rising pulse edge. When the 5 MHz signal is routed to the OSM, the signal is applied to pin one of U1A and to pin ten of U1B. On the falling pulse edge of the 5 MHz signal, U1A triggers generating a pulse train that appears at $\overline{Q}$-pin 4 which is applied to the NAND gate U2B pin four. The falling edge of the same pulse triggers U1B, this generates a pulse train at $\overline{Q}$-pin 12 which is applied to NAND gate U2B pin four. The falling edge of the same pulse triggers U1B, this generates a pulse train at Q-pin 12 which is applied to NAND gate U2B pin five. The two pulse trains with 50% duty cycle are NANDed by U2B to generate the 10 MHz signal, buffered and inverted by U2D, then propagated to the 100 MHz Reference Multiplier section. The timing and pulse generation from the 5 MHz sine wave to the 10 MHz TTL signals are presented in Figure 1.

2.3 The oven oscillator derives its DC power from a unique AC to DC power supply that serves only the oven oscillator. The circuitry is conventional in that the output from the AC step-down transformer T1 is connected across a bridge rectifier consisting of CR1, CR2, CR3, and CR4. The DC from the bridge rectifier is filtered by C3-4700 MF and regulated by U1-LM309K before connecting to the oven oscillator and the oscillator reference multiplier PCB assembly. The schematic diagram and PCB for the oscillator power supply are shown in Figure 2. The oscillator power supply is wired independently from the front panel AC power switch, and remains active whenever unit is plugged in. The primary voltage can be selected from 115 to 230 volts with primary switch S1.

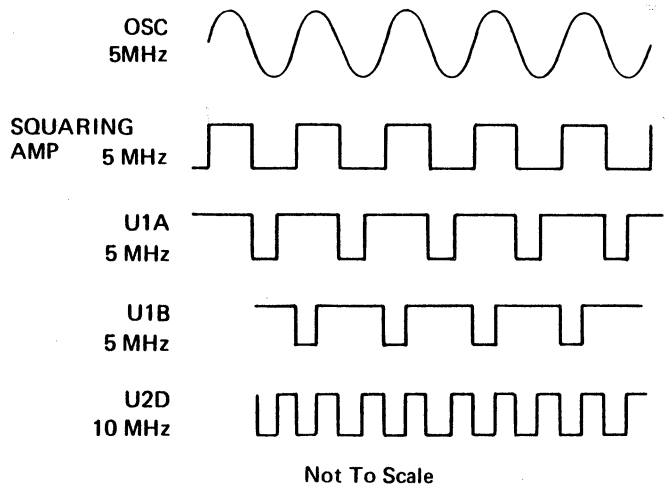
3. PARTS AND COMPONENT PLACEMENT

3.1 The oscillator assembly and reference multiplier are positioned above the main PCB assembly at the rear-left corner of the unit. The drawings on pages B5 thru B8 give the position of the optional installation. The oscillator power supply is located on the mid-right panel of the chassis. The additional parts required to assemble option 22A or option 24A are listed in the Parts Lists that follow.

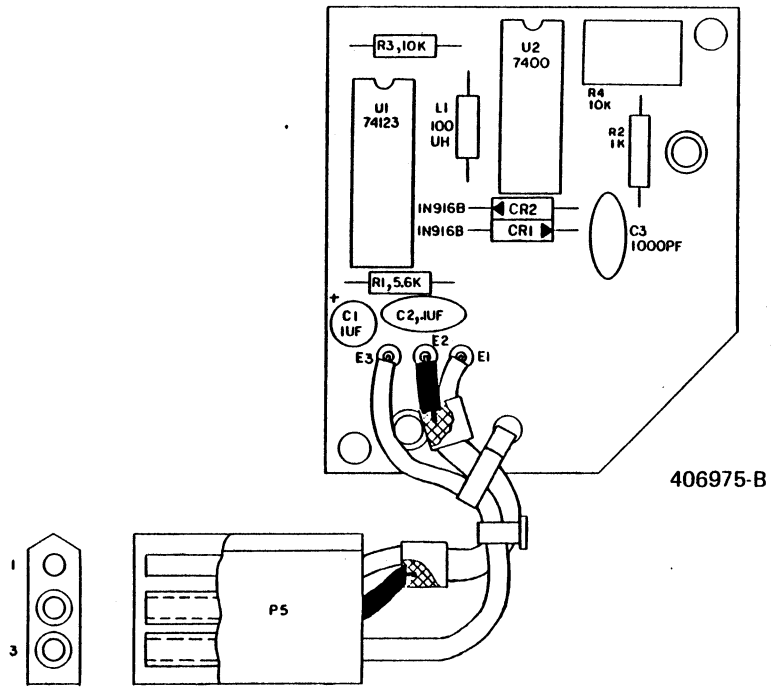




721975-C



Not To Scale



406975-B

Figure 1A - Oscillator Reference Multiplier Schematic and PCB Assy. (For earlier units)

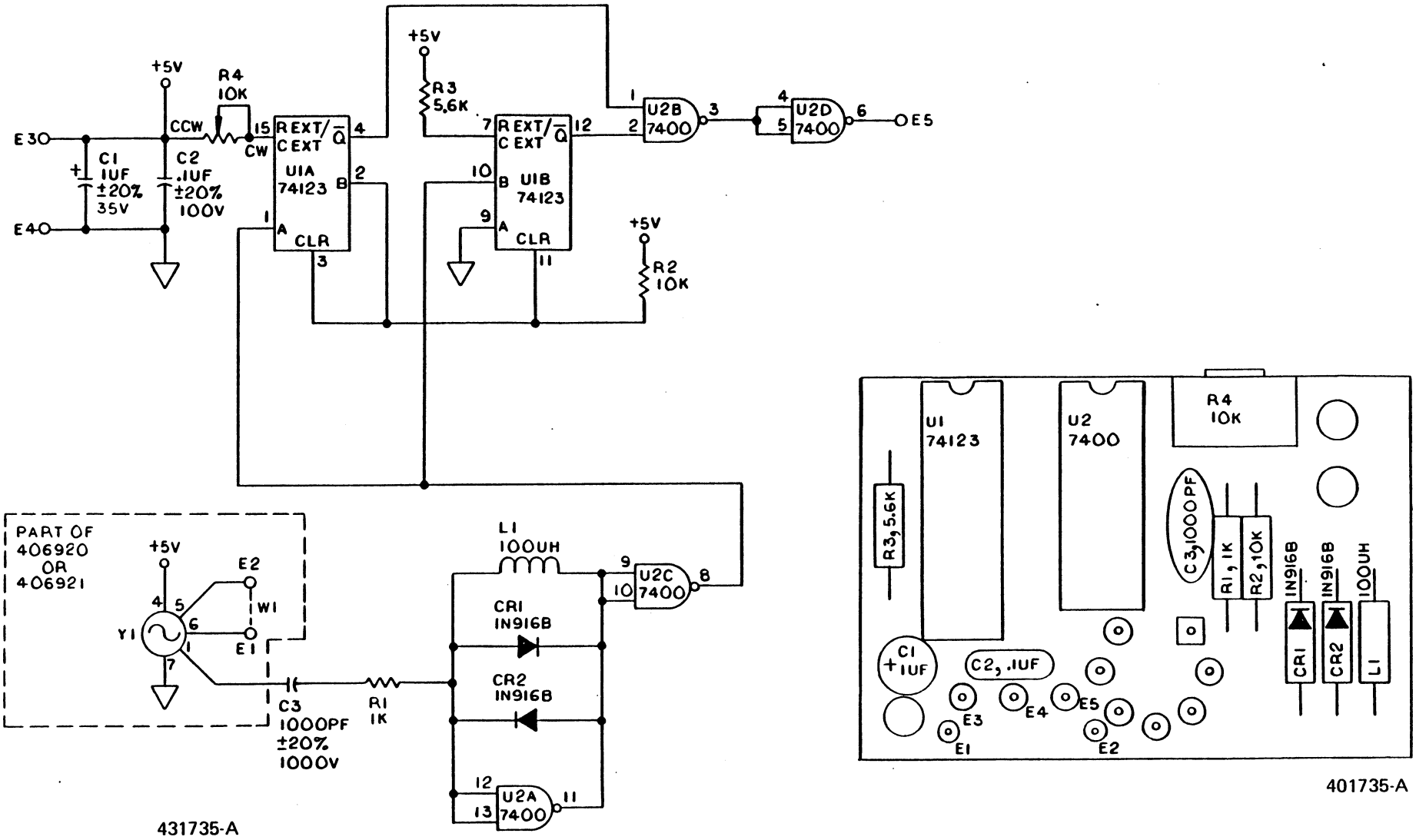
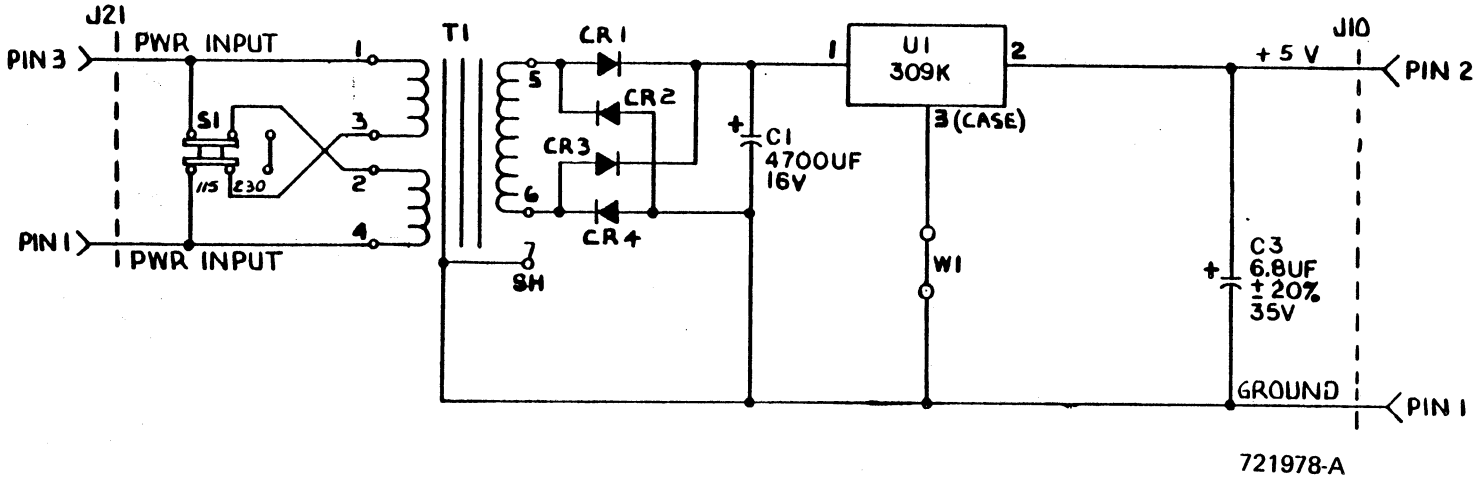


Figure 1B - Oscillator Reference Multiplier Schematic and PCB Assy. (For later units)



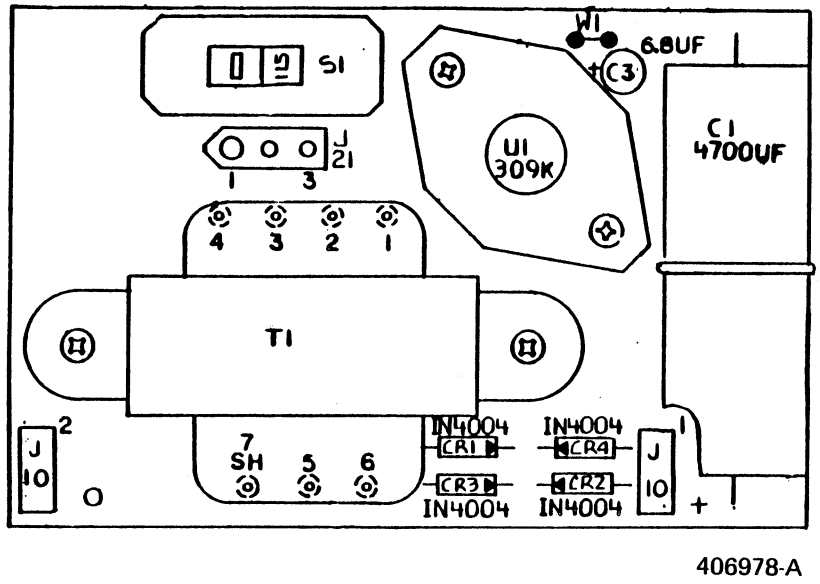
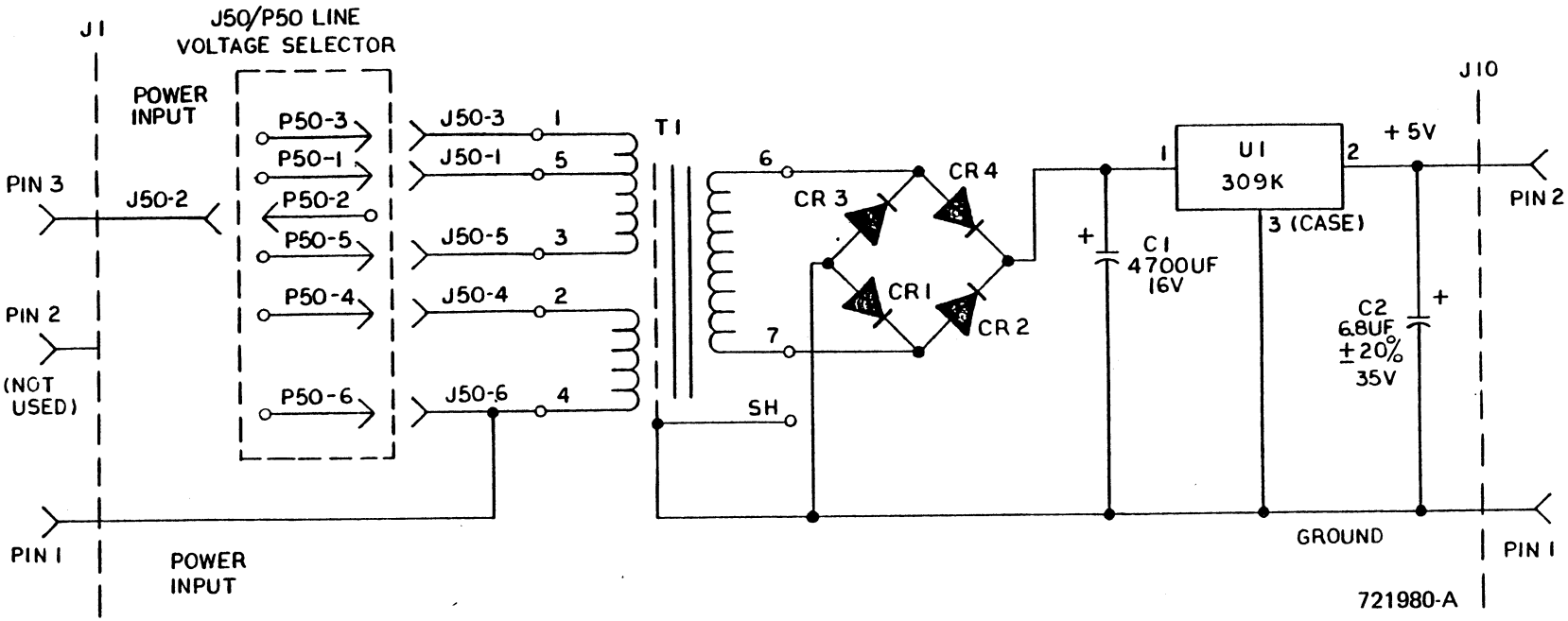


Figure 2A – Oscillator Power Supply Schematic and PCB Assy.
(For earlier units)



P50	100V	120V	220V	240V
1				
2				
3				
4				
5				
6				

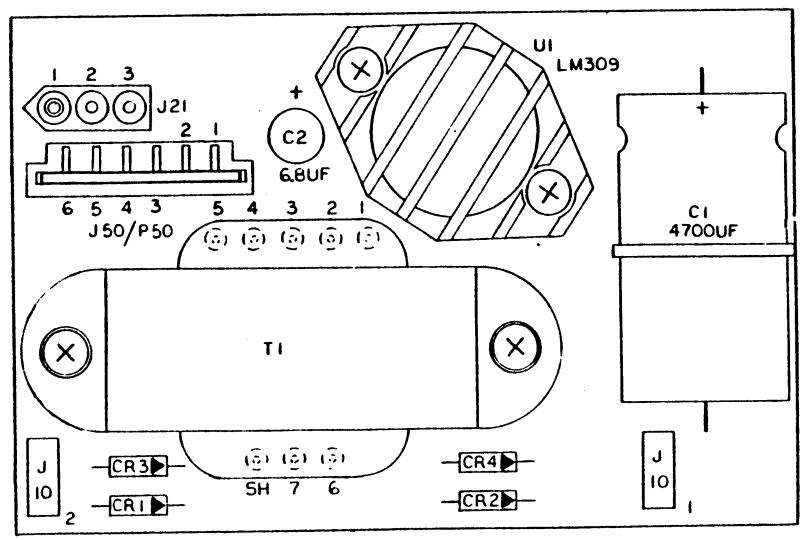
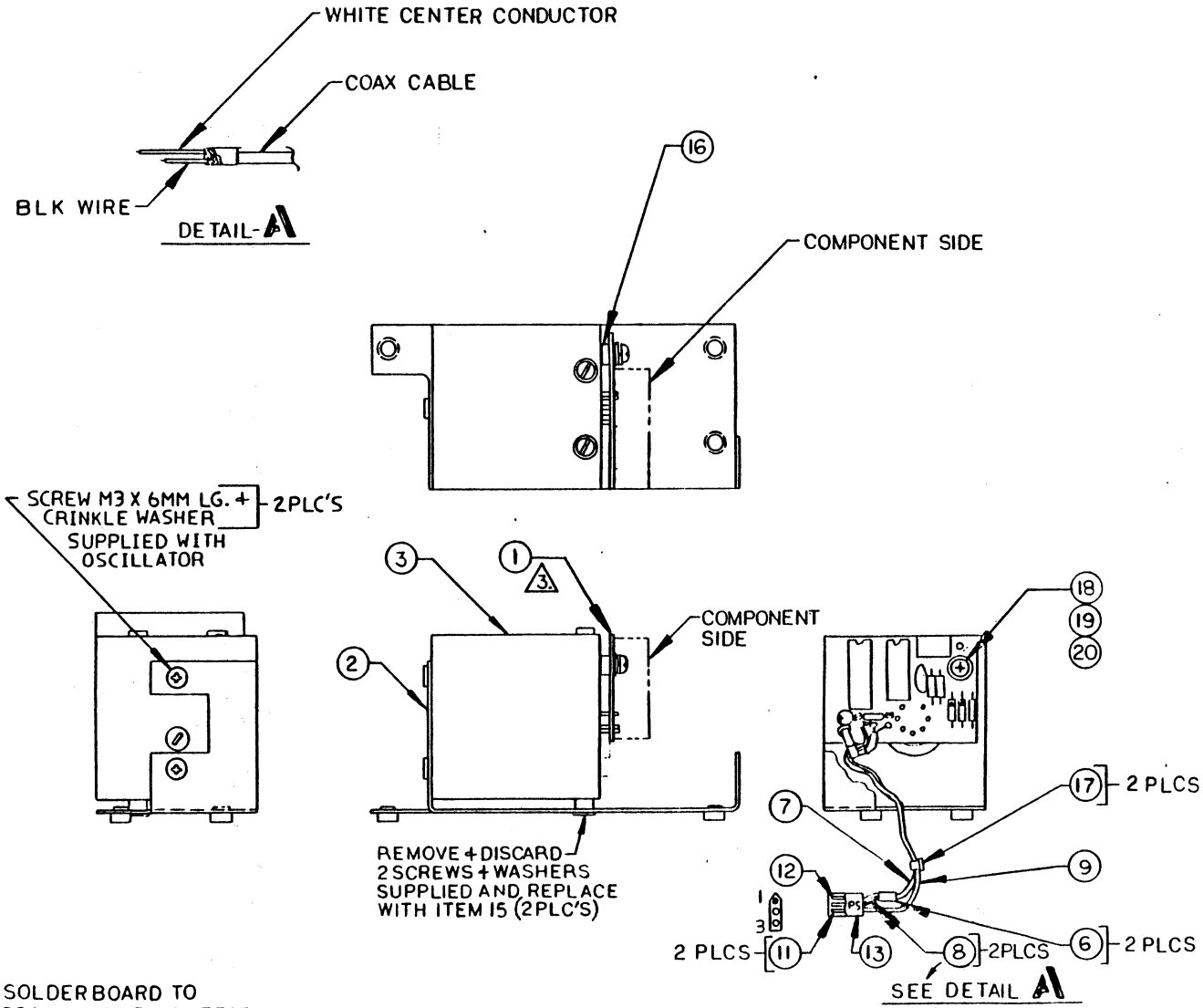


Figure 2B – Oscillator Power Supply Schematic and PCB Assy.
(For later units)



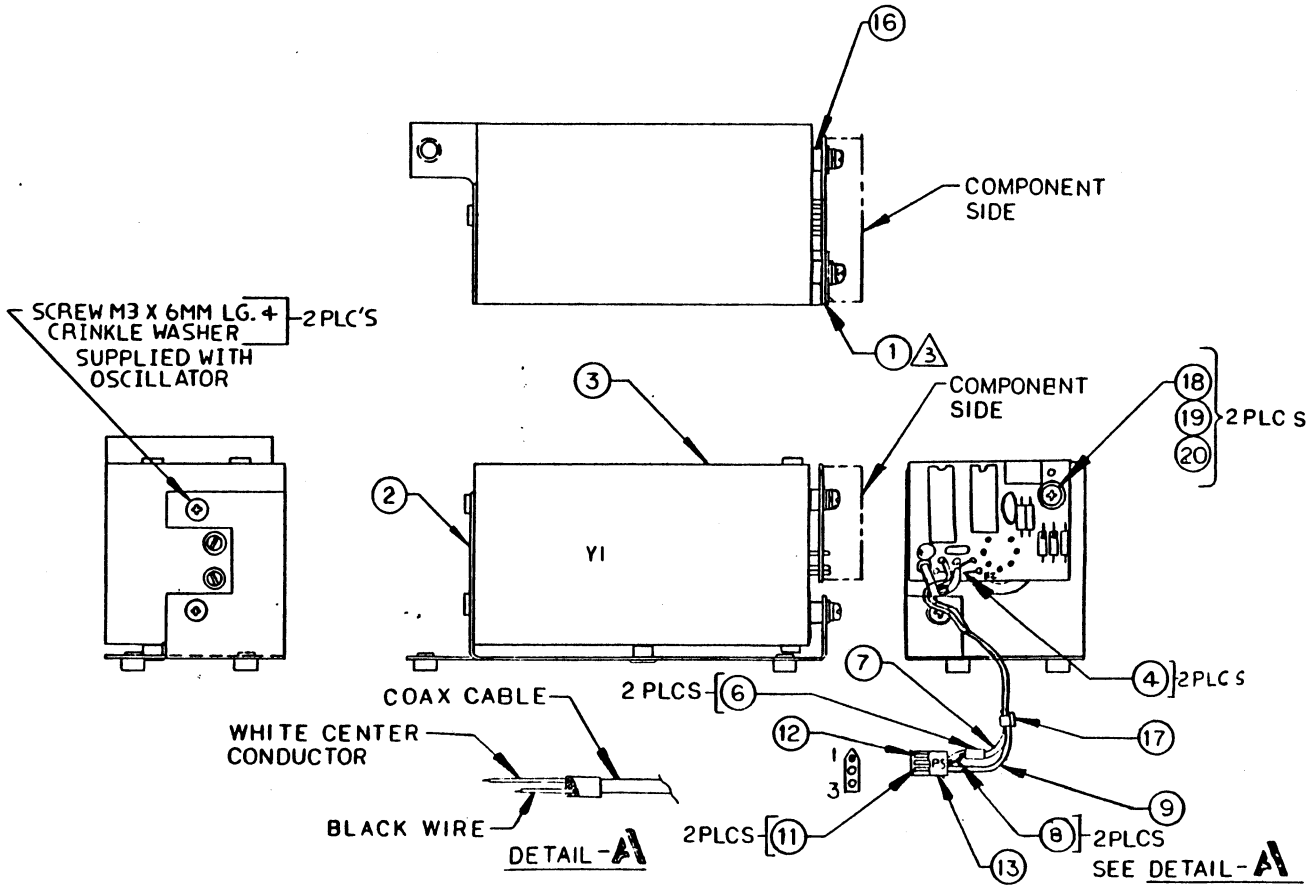
3. SOLDER BOARD TO OSCILLATOR PINS AFTER MECHANICAL ASSEMBLY.
2. TAG + IDENTIFY WITH RACAL-DANA P/N + CURRENT REV LTR.
1. ASSEMBLY PROCESSES + PROCEDURES TO CONFORM TO RACAL-DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

OSC ASSY,
5MHZ ±3X10^{-9}

SIZE	CODE IDENT NO	DWG NO.	REV
C	21793	406977	B

SCALE 1/1 SHEET OF 3



3. SOLDER BOARD TO OSCILLATOR PINS AFTER MECHANICAL ASSEMBLY.
2. TAG + IDENTIFY WITH RACAL DANA P/N + CURRENT REV. LTR
1. ASSEMBLY PROCESSES + PROCEDURES TO CONFORM TO RACAL-DANA WORKMANSHIP STANDARDS.

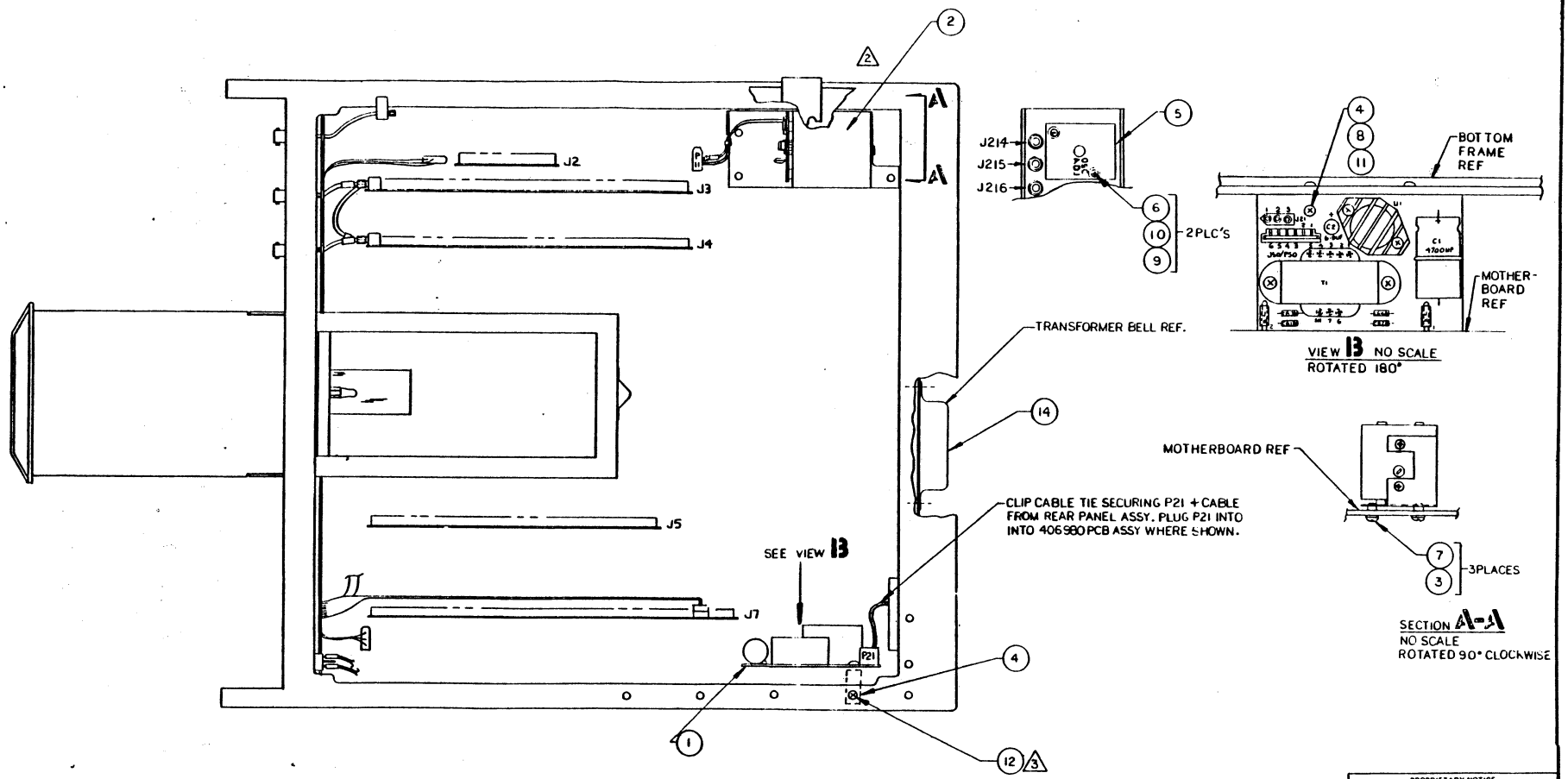
NOTES: UNLESS OTHERWISE SPECIFIED

OSC. ASSY, 5MHZ ±5X10⁻¹⁰

SIZE	CODE IDENT NO	DWG NO.	REV
C	21793	406976	B

SCALE 1/1 SHEET 1 OF 1

B7



3 ATTACH 454715 BRACKET (ITEM 13) TO THE BOTTOM FRAME AS SHOWN USING #6 THREAD FORMING SCREW (ITEM 12). DO NOT TIGHTEN. PLUG 406980 ASSY (ITEM 1) INTO MOTHERBOARD AND SECURE TO MOUNTING BRACKET (ITEM 13) USING #6 HARDWARE (ITEM 4 & 11). REPLACE 730706 RETAINER + FINALLY TIGHTEN #6 THREAD FORMING SCREW (ITEM 12).

2 REMOVE STANDARD OSCILLATOR 730655 IF INSTALLED + REPLACE WITH 406977.

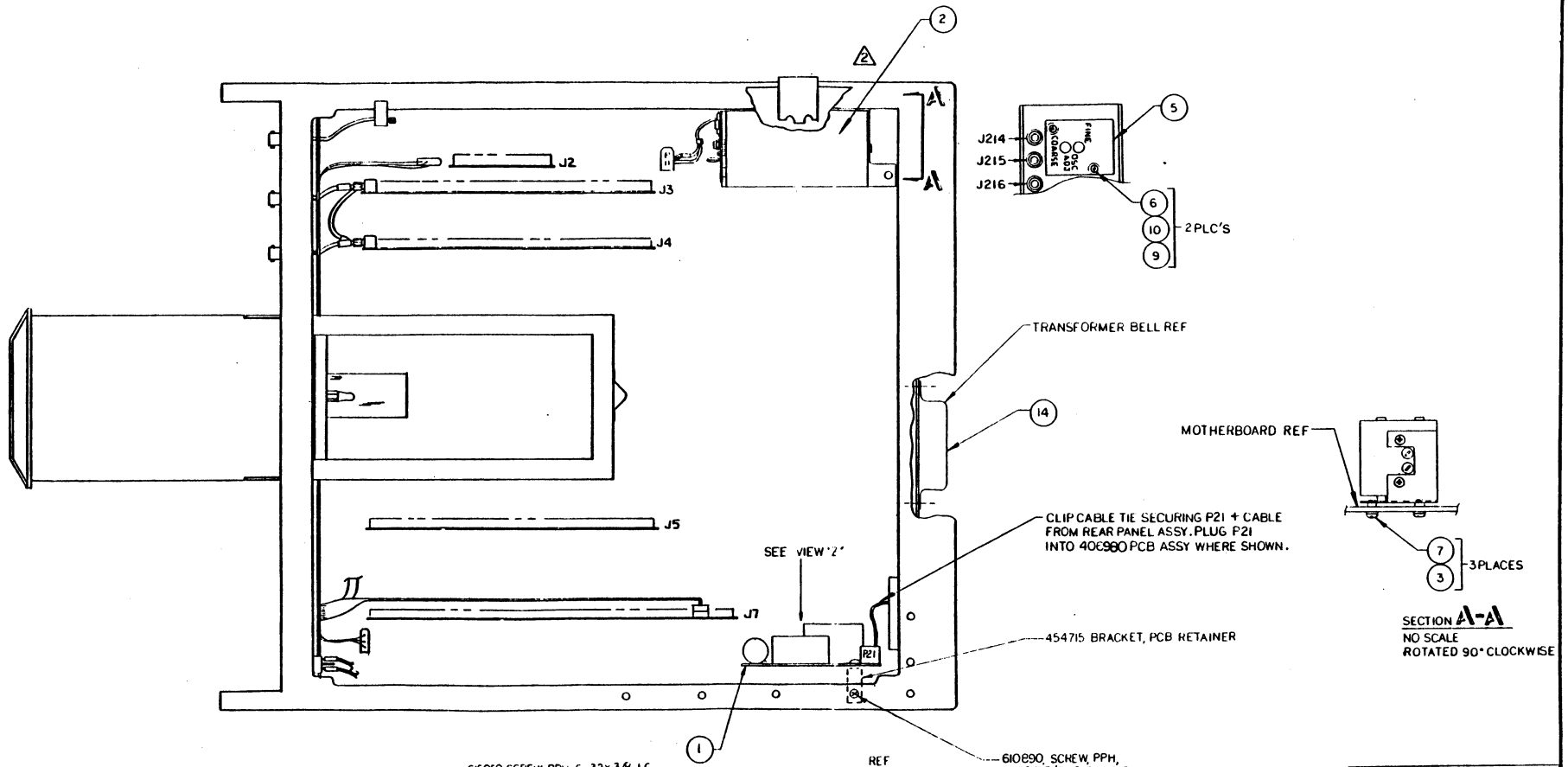
1. ASSY PROCESSES + PROCEDURES TO CONFORM TO RACAL-DANA WORKMANSHIP STANDARDS.

NOTES UNLESS OTHERWISE SPECIFIED

OSC ASSY, OVEN, OPT 22A

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	406180	C

SCALE NONE | SHEET 1 OF 2



3 ATTACH 454715 BRACKET TO THE BOTTOM FRAME AS SHOWN USING #6 THREAD FORMING SCREW. DO NOT TIGHTEN. PLUG 406980 ASSY INTO MOTHERBOARD AND SECURE TO MOUNTING BRACKET USING #6 HARDWARE. REPLACE 730706 RETAINER AND FINALLY TIGHTEN #6 THREAD FORMING SCREW.

2 REMOVE STANDARD OSCILLATOR 730655 IF INSTALLED & REPLACE WITH 406976.

1. ASSY PROCESSES & PROCEDURES TO CONFORM TO RACAL-DANA WORKMANSHIP STANDARDS.

NOTES UNLESS OTHERWISE SPECIFIED

OSC ASSY, OVEN, OPT 24 A

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406181	D

SCALE NONE SHEET 1 OF 2

By

406977 - OSCILLATOR ASSEMBLY, 5 MHz

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	401735	PCB ASSY., REFERENCE	21793	401735
2	730771	BRACKET, OSCILLATOR	21793	730771
3	730746	OSCILLATOR, XTAL, OVEN, 5 MHz (Y1)	21793	730746
6	500002	TUBING, SHRINK, .153 ID	--	--
7	501446	CABLE, COAX, RG188A	--	--
8	524000	WIRE, TEFLON, STRANDED, 24 GA, BLK	--	--
9	524929	WIRE, TEFLON, STRANDED, 24 GA, WHT/RED	--	--
11	600650	TERMINAL PIN, FEMALE (2 REQ'D)	27264	1433
12	600651	TERMINAL PIN, MALE	27264	1434
13	600797	CONN, RECEPT., 3-PIN, (P5)	27264	03-09-1032
15	610931	SCREW, PFH, M3 X 10, (2 REQ'D)	21969	7987 (DIN)
16	610503	SPACER, NON-SWAGE,#6, METALLIC, .125L X .250D X .140 ID	--	--
17	610777	CABLE TIE (2 REQ'D)	--	T18R
18	610869	SCREW, PFH, M3 X 12 (2 REQ'D)	05573	43583
19	617103	WASHER, FLAT,#6, LIGHT SERIES (2 REQ'D)	--	--
20	617128	WASHER, LOCK,#6, LIGHT SERIES (2 REQ'D)	--	--

406976 - OSCILLATOR ASSEMBLY, 5 MHz

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	401735	PCB ASSY., REFERENCE	21793	401735
2	730771	BRACKET, OSCILLATOR	21793	730771
3	730745	OSCILLATOR, XTAL, OVEN, 5 MHz (Y1)	21793	730745
4	500023	WIRE, BARE, COPPER/TIN, 24 GA	--	--
6	500002	TUBING, SHRINK, .153 ID	--	--
7	501446	CABLE, COAX, RG188A	--	--
8	524000	WIRE, TEFLON, STRANDED, 24 GA, BLK	--	--
9	524929	WIRE, TEFLON, STRANDED, 24 GA, WHT/RED	--	--
11	600650	TERMINAL PIN, FEMALE (2 REQ'D)	27264	1433
12	600651	TERMINAL PIN, MALE	27264	1434
13	600797	CONN, RECEPT., 3-PIN, (P5)	27264	03-09-1032
15	610931	SCREW, PFH, M3 X 10, (2 REQ'D)	21969	7987 (DIN)
16	610503	SPACER, NON-SWAGE,#6, METALLIC, .125L X .250D X .140 ID	--	--
17	610777	CABLE TIE (2 REQ'D)	--	T18R
18	610869	SCREW, PFH, M3 X 12 (2 REQ'D)	05573	43583
19	617103	WASHER, FLAT,#6, LIGHT SERIES (2 REQ'D)	--	--
20	617128	WASHER, LOCK,#6, LIGHT SERIES (2 REQ'D)	--	--

406180 - OSCILLATOR ASSY., OVEN, OPT. 22A

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	406980	PCB ASSY., OSC PWR SUPPLY	21793	406980
2	406977	OSCILLATOR ASSY.	21793	406977
3	610568	WASHER, FLAT, NYLON, BLK, .12 X .28 X .06 (3 REQ'D)	95987	NW4-2816
4	615059	SCREW, PPH, 6-32 X .375	--	--
5	454525	COVER, OSCILLATOR	21793	454525
6	615042	SCREW, PPH, 4-40 X .250 (2 REQ'D)	--	--
7	615058	SCREW, PPH, 6-32 X .312 (3 REQ'D)	--	--
8	617103	WASHER, FLAT,#6, LIGHT SERIES	--	--
9	617102	WASHER, FLAT,#4, LIGHT SERIES (2 REQ'D)	--	--
10	617127	WASHER, LOCK,#4, LIGHT SERIES (2 REQ'D)	--	--
11	617128	WASHER, LOCK,#6, LIGHT SERIES	--	--
12	610890	SCREW, TAPTITE, THREAD FORMING, 6-32 X .375	78189	--
13	454715	BRACKET, PCB RETAINER	21793	454715
14	920893	LABEL, CAUTION	21793	920893

406181 - OSCILLATOR ASSY., OVEN, OPT. 24A

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	406980	PCB ASSY., OSC PWR SUPPLY	21793	406980
2	406976	OSCILLATOR ASSY.	21793	406976
3	610568	WASHER, FLAT, NYLON, BLK, .12 X .28 X .06 (3 REQ'D)	95987	NW4-2816
4	615059	SCREW, PPH, 6-32 X .375	--	--
5	454526	COVER, OSCILLATOR	21793	454526
6	615042	SCREW, PPH, 4-40 X .250 (2 REQ'D)	--	--
7	615058	SCREW, PPH, 6-32 X .312 (3 REQ'D)	--	--
8	617103	WASHER, FLAT,#6, LIGHT SERIES	--	--
9	617102	WASHER, FLAT,#4, LIGHT SERIES (2 REQ'D)	--	--
10	617127	WASHER, LOCK,#4, LIGHT SERIES (2 REQ'D)	--	--
11	617128	WASHER, LOCK,#6, LIGHT SERIES	--	--
12	610890	SCREW, TAPTITE, THREAD FORMING, 6-32 X .375	78189	--
13	454715	BRACKET, PCB RETAINER	21793	454715
14	920893	LABEL, CAUTION	21793	920893

406975 - Assy., PCB, OSC REF MUL

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	110143	CAP TANTA 1MFD 35V 20%	05397	T368A105M035AS
C2	100027	CAP CERAM .1MFD 100V 20%	72982	845-000-X5V0104Z
C3	100071	CAP CERAM .001MFD 100V 20%	56289	C023B102E102M
CR1	211083	DIODE SILICO 1N916B	81349	1N916B
CR2	211083	DIODE SILICO 1N916B	81349	1N916B
L1	310151	CHOKE 100μH	91637	IR-2, 100μH
P5	600797	CON RECPTLE 3P	27264	03-09-1032
R1	000562	RES CARBON 5.6K 5% 1/4W	81349	RC076F562J
R2	000102	RES CARBON 1K 5% 1/4W	81349	RC076F102J
R3	000103	RES CARBON 10K 5% 1/4W	81349	RC076F103J
R4	040179	POT CERMET 10K 20% 3/4W	11237	360 SERIES
U1	230189	IC	01295	SN75123N
U2	230028	IC CERAM	07263	7400

401735 - Assy., PCB, OSC REF MUL

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	110143	CAP TANTA 1MFD 35V 20%	05397	T368A105M035AS
C2	100027	CAP CERAM .1MFD 100V 20%	72982	845-000-X5V0104Z
C3	100071	CAP CERAM .001MFD 100V 20%	56289	C023B102E102M
CR1	211083	DIODE SILICO 1N916B	81349	1N916B
CR2	211083	DIODE SILICO 1N916B	81349	1N916B
L1	310151	CHOKE 100μH	91637	IR-2, 100μH
R1	000102	RES CARBON 1K 5% 1/4W	81349	RC076F102J
R2	000103	RES CARBON 10K 5% 1/4W	81349	RC076F103J
R3	000562	RES CARBON 5.6K 5% 1/4W	81349	RC076F562J
R4	040179	POT CERMET 10K 20% 3/4W	11237	360 SERIES
U1	230189	IC	01295	SN75123N
U2	230028	IC CERAM	07263	7400

406978 - Assy., PCB, OSC POWER SUPPLY (FOR EARLIER UNITS)

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	110185	CAP ELECT 4700 MFD 16V	05397	T362D337K006AS
C3	110126	CAP TANTA 6.8MFD 35V 20%	05397	T368B685M035AS
CR1	210004	DIODE SILICO	81349	1N4004
CR2	210004	DIODE SILICO	81349	1N4004
CR3	210004	DIODE SILICO	81349	1N4004
CR4	210004	DIODE SILICO	81349	1N4004
J21	600798	CONN PLUG	27264	09-18-5031
S1	600521	SWITCH DPDT	82389	46256LFE
T1	300095	TRANS POWER SUPPLY	17474	4-10520
U1	230144	IC	27014	LM309KC

406980 - Assy., PCB, OSC POWER SUPPLY (FOR LATER UNITS)

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	110185	CAP ELECT 4700 MFD 16V	05397	T362D337K006AS
C2	110126	CAP TANTA 6.8MFD 35V 20%	05397	T368B685M035AS
CR1	210004	DIODE SILICO	81349	1N4004
CR2	210004	DIODE SILICO	81349	1N4004
CR3	210004	DIODE SILICO	81349	1N4004
CR4	210004	DIODE SILICO	81349	1N4004
J21	600798	CONN PLUG	27264	09-18-5031
J50	600821	CONN 6P	27264	09-03-1062
P50	410727	PCB LINE VOLTAGE	21793	410727
T1	300102	TRANSFORMER, POWER	23095	149000
U1	230144	IC	27014	LM309KC

TABLE OF CONTENTS

Section	Title	Page
1	GENERAL DESCRIPTION	
2	INSTALLATION & OPERATION	
3	SYSTEMS INTERFACE	

These sections are included in the Model 9000A Operators Manual. Publication No. 980535

4	**THEORY OF OPERATION**	4-1
4.1	General	4-1
4.2	Basic Operation	4-1
4.3	Measurement Modes	4-2
4.3.2	Test	4-2
4.3.3	Period	4-2
4.3.4	Period Average	4-3
4.3.5	Frequency A	4-3
4.3.6	Frequency C (Model 9035A only)	4-4
4.3.7	Totalize	4-4
4.3.8	Time Interval	4-4
4.3.9	Time Interval Average	4-4
4.3.10	A/B (Ratio)	4-5
4.4	Circuit Description	4-6
4.4.2	Signal Conditioning Modules	4-6
4.4.3	Prescaler, F_C (Model 9035A only)	4-7
4.4.4	DAC Board	4-8
4.4.5	Reference Multiplier Circuit	4-9
4.4.6	Display Board	4-12
4.4.7	Control-I/O System	4-12
4.4.8	Keyboard	4-14
4.4.9	Mainframe	4-15
4.5	Reference Option Supply	4-26
4.6	High Speed Interface Functional Operation (Option 56)	4-26
4.7	Control and Status Signals	4-26
4.8	Control Signal Description	4-27
4.9	Computer Programming Considerations	4-27
5	**MAINTENANCE**	5-1
5.1	Introduction	5-1
5.2	Function and Timebase Checks	5-1
5.3	Calibration Adjustment	5-4
5.3.1	Introduction and Description	5-4
5.4	Required Equipment	5-4
5.5	Disassembly, Calibration	5-4
5.6	Preliminary Operation	5-4
5.7	Calibration Points	5-5
5.8	Procedure	5-5
5.8.2	Power Supply (Main Logic Board)	5-5
5.8.3	DAC	5-5
5.8.4	Reference Board (Assembly No. 406768)	5-5
5.8.5	Signal Conditioning Circuit, Channel A and B	5-5
5.8.6	Prescaler (Model 9035A only)	5-9
5.8.7	Internal Reference	5-9
5.8.8	External Reference Circuit Check	5-10
5.9	Maintenance Disassembly	5-10
5.9.2	Replacing Front Panel LEDs	5-10

TABLE OF CONTENTS continued

Section	Title	Page
5.10	Unit Performance Tests	5-13
5.11	Subassembly Performance Tests	5-93
5.12	Main Logic Sig/Ref Circuits	5-112
5.13	Display Subassembly Performance Test	5-115
5.14	Board Revision	5-158
6	**DRAWINGS**	**6-1**
7	**PARTS LIST**	**7-1**

LIST OF ILLUSTRATIONS

Figure	Title	Page
4.1	9000A Block Diagram	4-1
4.2	Test	4-2
4.3	Period	4-2
4.4	Period Average	4-3
4.5	Frequency A	4-3
4.6	Frequency C	4-4
4.7	Totalize	4-4
4.8	Time Interval	4-5
4.9	Time Interval Average	4-5
4.10	A/B Ratio	4-5
4.11	Inter-Board Signal Flow	4-6
4.12	Signal Conditioning Block Diagram	4-7
4.13	Prescaling Amplifier, F_C (Model 9035A only)	4-8
4.14	DAC Board	4-9
4.15	Reference Multiplier Circuit	4-9
4.16	Switch/Gate	4-10
4.17	Display Board Block Diagram	4-10
4.19	Control and I/O System Distribution	4-12
4.20	Keyboard	4-15
4.21	Gate Control	4-16
4.22	Synchronizer	4-17
4.23	Time Interval Signal Routing	4-20
4.24	Time Interval Average Signal Routing	4-21
4.25	Period Signal Routing	4-21
4.26	Period Average Signal Routing	4-22
4.27	Frequency A Signal Routing	4-22
4.28	A/B Ratio Signal Routing	4-23
4.29	Totalize Signal Routing	4-23
4.30	Marker	4-24
4.31	Start/Stop Circuit	4-24
4.32	Initialize Circuit	4-25
4.33	Signal Detect	4-25
4.34	Clear Circuitry	4-26
4.35	Interface Functional Block Diagram	4-28
4.36	Read Mode Handshake Timing	4-29
4.37	Write Mode Handshake Timing	4-30

LIST OF ILLUSTRATIONS (continued)

Figure	Title	Page
5.1	5th Harmonic Output	5-5
5.2	100 MHz Signal	5-5
5.3	Marker Hookup	5-8
5.4	Square Wave Signal	5-8
5.5	Oscillator Drift	5-10
5.6	Calibration Point	5-11
5.7	Main Logic Preliminary Unit Performance Test Points	5-18
5.8	Reference PCB Preliminary Unit Performance Test Points	5-19
5.9	DAC PCB Preliminary Unit Performance Test Points	5-19
5.10	Frequency A (Frequency B) Functional Block Diagram	5-25
5.11	Frequency A (FA Sig Cond) Unit Performance Test Points	5-27
5.12	Frequency A (Main Logic) Unit Performance Test Points	5-28
5.13	Frequency A (FA) Single Thread Diagram	5-33
5.14	Frequency C (Prescaler) Functional Block Diagram	5-37
5.15	Frequency C (Prescaler) Unit Performance Test Points	5-38
5.16	Frequency C (Main Logic) Unit Performance Test Points	5-40
5.17	Frequency C (FC) Single Thread Diagram	5-43
5.18	Period (Main Logic) Unit Performance Test Points	5-47
5.19	Period (P) Single Thread Diagram	5-51
5.20	Time Interval (Main Logic) Unit Performance Test Points	5-55
5.21	Time Interval (TI) Single Thread Diagram	5-59
5.22	Period Average (Main Logic) Unit Performance Test Points	5-63
5.23	Period Average (PA) Single Thread Diagram	5-67
5.24	Time Interval Average (Main Logic) Unit Performance Test Points	5-71
5.25	Time Interval Average (TIA) Single Thread Diagram	5-75
5.26	Ratio (Main Logic) Unit Performance Test Points	5-79
5.27	Ratio (A/B) Single Thread Diagram	5-83
5.28	Totalize (Main Logic) Unit Performance Test Points	5-87
5.29	Totalize (TO) Single Thread Diagram	5-91
5.30	Power Supply (Rear Panel & Main Logic) Subassembly Performance Test	5-94
5.31	Main Logic Subassembly Test Points	5-111
5.32	Display (Circuit Side) Component Location Drawing	5-115
5.33	Display Input/Output Signals	5-115
5.34	Signal Conditioner (Ch A/Ch B) Subassembly Test Points	5-124
5.35	Prescaler (FC) Subassembly Test Points	5-128
5.36	DAC Subassembly Test Points	5-133
5.37	Reference Subassembly Test Points	5-139
5.38	Option (22/24) Power Supply (Regulator) Test Points	5-141
5.39	Control PCB Assembly	5-145
5.40	I/O PC Board Assembly	5-155

LIST OF TABLES

Table	Title	Page
4.1	Operational Cycle	4-2
4.2	Display Coding	4-11
4.3	Synchronizer Timing Diagram (TIA)	4-17
4.4	Synchronizer Operation TIA	4-18
4.5	Control Register Codes	4-19
4.6	Control Signal Functions	4-31
4.7	Status Signal Functions	4-32
5.1	Function and Time Base Cal Check	5-2
5.2	Required Equipment	5-4
5.3	Trigger Level Cal Check	5-6
5.4	Sensitivity Cal Check	5-7
5.5	Internal Reference Oscillators	5-9
5.6	Preliminary Unit Performance Test	5-13
5.7	Keyboard Entry/Display Response Preliminary Unit Performance Test	5-14
5.8	Preliminary Main Logic, Reference and DAC Unit Performance Tests	5-16
5.9	Frequency A (FA) Unit Performance Test	5-22
5.10	Frequency C (FC) Unit Performance Test	5-35
5.11	Period (P) Unit Performance Test	5-45
5.12	Time Interval (TI) Unit Performance Test	5-53
5.13	Period Average (PA) Unit Performance Test	5-61
5.14	Time Interval Average (TIA) Unit Performance Test	5-69
5.15	Ratio (A/B) Unit Performance Test	5-77
5.16	Totalize (TO) Unit Performance Test	5-85
5.18	(Main Logic) Clear Subassembly Performance Test	5-97
5.19	(Main Logic) Start/Stop Subassembly Performance Test	5-101
5.20	(Main Logic) Signal Detector Subassembly Performance Test	5-103
5.21	(Main Logic) Synchronizer Subassembly Performance Test	5-106
5.22	(Main Logic) Gate Control Subassembly Performance Test	5-108
5.23	Accumulator Steering Logic Signal Paths	5-112
5.24	Gate Steering Logic	5-112
5.25	Timebase In Steering Logic	5-112
5.26	Timebase Counter	5-113
5.27	$\div 10^{0 \text{ to } 7}$ Counter Decode For T/B Multiplier	5-113
5.28	Signal Conditioner (Ch. A/Ch. B) Subassembly Performance Test	5-117
5.29	Prescaler (FC) Subassembly Performance Test	5-125
5.30	DAC Subassembly Performance Test	5-129
5.31	DAC Shift Register Logic Output Codes	5-132
5.32	Reference Subassembly Performance Test	5-134
5.33	Option (22/24) Oscillator Power Supply (Regulator) Subassembly Performance Test	5-140
5.34	Control Performance Test	5-142
5.35	I/O Performance Test	5-146
5.36	IC and Transistor Usage For (Main Logic) Function/Circuit Distribution	5-156
7.1	Table 7.1	7-1
7.2	List of Suppliers	7-1

SECTION 4 THEORY OF OPERATION

4.1 GENERAL.

4.1.1 This section covers the Theory of Operation of the Series 9000A Microprocessing Timer/Counter. The operation is first analyzed in terms of a basic block diagram (figure 4.1); second, the various operating modes are examined; and third, individual circuits are described.

4.1.2 The drawings included in this section are for aiding in the descriptions and are provided as a supplement to the complete schematics located in Section 6.

4.2 BASIC OPERATION.

4.2.1 The Series 9000A is shown in block diagram form in figure 4.1. Referring to this drawing, input signals are processed through the signal conditioner or RF prescaler and fed to the steering synchronizing circuitry. Depending on the function selected, the steering circuitry routes the input signal to the main gate, control logic or the timebase. The synchronizing circuitry is used in the TIA function. The steering logic also routes the output of the timebase to the control logic or the main gate and the 100 MHz output of the reference multiplier to the timebase counters, control logic, or main gate.

4.2.2 Operating instructions are entered through the keyboard. The microprocessor (μP) scans the keyboard and relays the programming information to the program control, which determines the routing through the steering circuitry, controls the control gate logic and sets the timebase frequency division.

4.2.3 The output of the main gate is fed to the accumulator counters, where the number of input pulses are accumulated, and the BCD equivalent of the number of pulses accumulated is transferred to the latch.

4.2.4 The μP strobes the latch and the data in the latch is transferred in serial form to the μP. The latch data, along with the status of the trigger levels, the timebase setting, the scale of the display, and function selected, is sent in multiplexed form to the display.

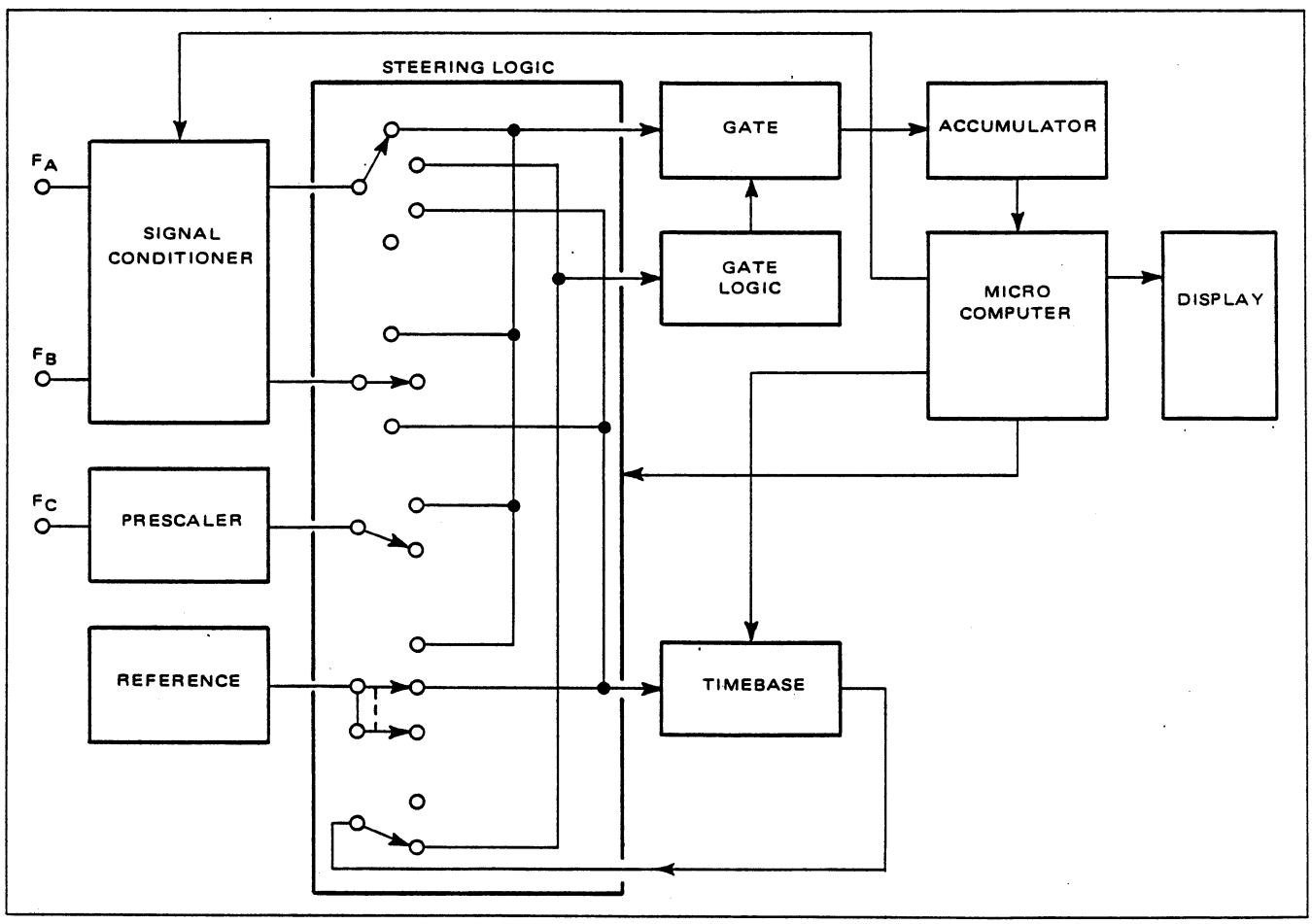


Figure 4.1 - 9000A Block Diagram

4.2.5 If arithmetic operations are performed on the measurement, the data is entered through the keyboard and the process takes place entirely within the μP. The resultant is then routed to the display.

4.2.6 The interface option permits control of the instrument by electrical means and provides the data displayed on the front panel in digital form.

4.2.7 The precise sequence by which the 9000A performs a specific measurement or operation varies from one instance to another. However, the overall operation follows a specific operational cycle. This is illustrated in table 4.1.

Table 4.1 - Operational Cycle

Control Signal	Operation	Note
1. $\overline{\text{CLEAR}}$ goes high:	A measurement cycle is performed	Gate Start Gate Stop
2. $\overline{\text{DATA READY}}$ goes low:	Signals μP measurement is complete	—
3. $\overline{\text{UPDATE}}$ goes low, μP generates ACC Clock:	Shift register feeds data to μP	—
4. $\overline{\text{CLEAR}}$ goes low:	Counters and flip-flops are reset	—

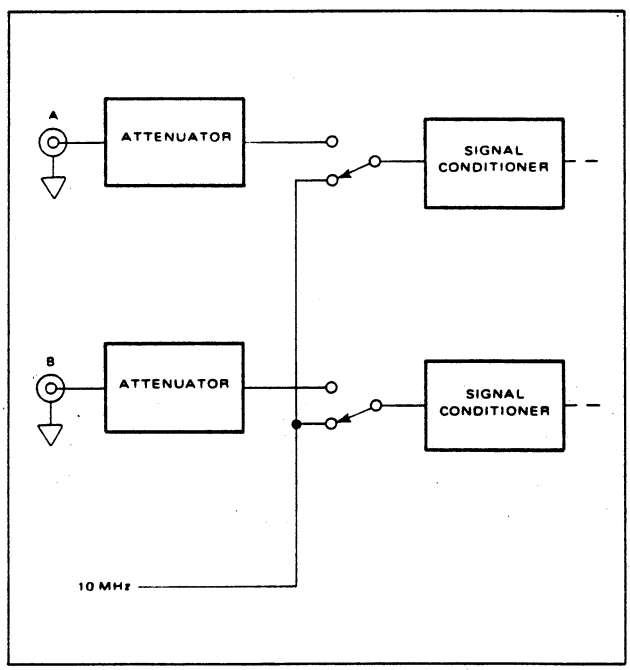


Figure 4.2 - Test

4.3 MEASUREMENT MODES.

4.3.1 The function selected modifies the routing of both the input signal or signals and the reference signal. These differences in instrument operation are described in the following paragraphs. For simplicity in the accompanying figures, the accumulator counters are shown driving the display.

4.3.2 Test.

4.3.2.1 The TEST mode of operation (figure 4.2) enables the operator to check for proper operation of the counter in all operating modes.

4.3.2.2 In this mode the reference signal is used as an input to both channel A and channel B signal conditioning networks.

4.3.3 Period.

4.3.3.1 Period is the inverse of frequency. Therefore, channel A signal is applied to the control logic and the reference signal is connected to the timebase counters (figure 4.3).

4.3.3.2 Clock pulses are derived by dividing down the 100 MHz reference multiplier output. The specific decade division is determined by the setting of the Timebase switches. The output of the Timebase counters is presented

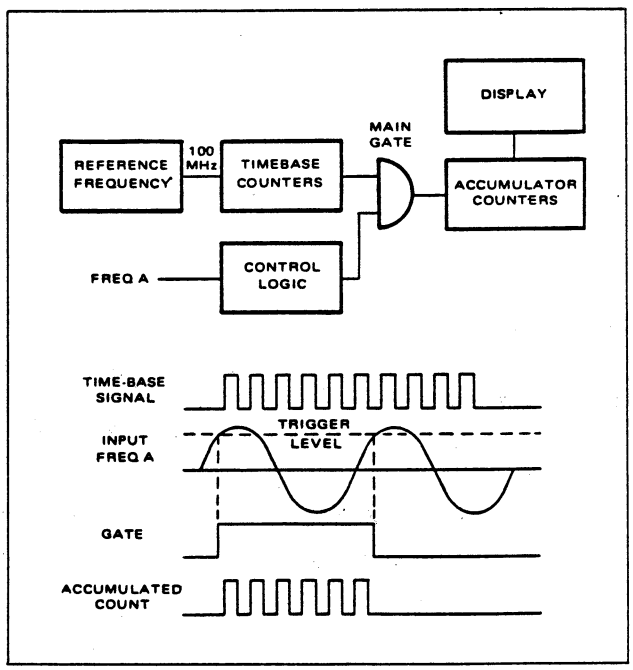


Figure 4.3 - Period

to the input of the accumulator counters. Trigger pulses resulting from two consecutive signals from input A are applied to the control logic. The first trigger pulse opens the main gate; the next pulse closes it. During "gate open" time, the counter counts the applied clock pulses. The count is displayed on the readout directly in microseconds, milliseconds, or seconds, according to the Timebase switch setting.

NOTE

Low frequencies may be determined more accurately by measuring period rather than frequency directly. This is because the longer period of a low frequency allows more counts to accumulate in a period measurement. Therefore, resolution and accuracy are both improved. The 1/X key can then be selected to display the reading directly in frequency.

4.3.4 Period Average.

4.3.4.1 Period Average mode is used to obtain increased resolution and accuracy over period measurements. The more periods over which a signal is averaged, the greater the accuracy of the measurement.

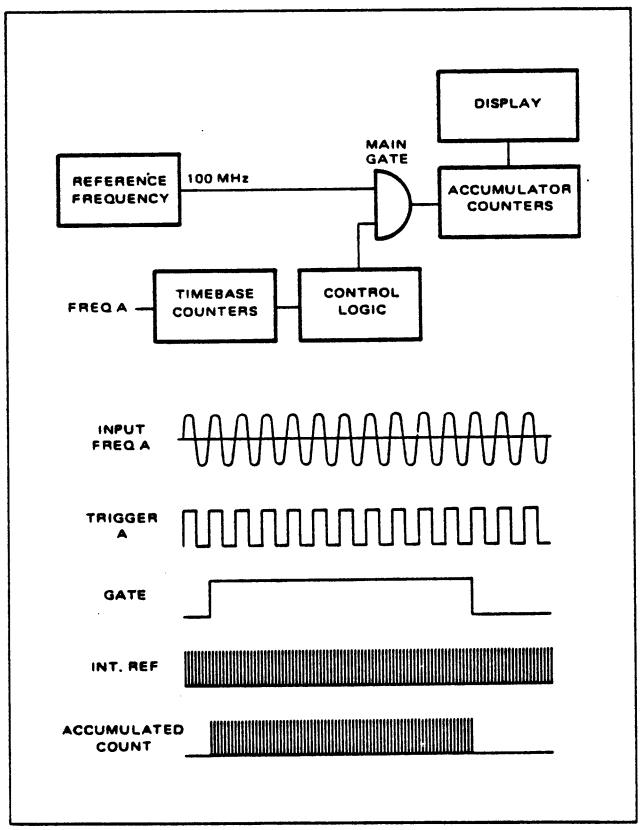


Figure 4.4 - Period Average

4.3.4.2 In this mode of operation (figure 4.4), the reference signal is routed directly to the main gate and the unknown signal is routed through the timebase to the control logic which, in turn, controls the main gate. The pulses occurring during main "gate open" are counted, stored, and an accurate readout measurement is displayed. The "gate open" period is determined by the timebase selected.

4.3.5 Frequency A.

4.3.5.1 During direct frequency measurements, the counter compares the unknown frequency against the known reference frequency (figure 4.5).

4.3.5.2 Channel A input signal is routed to the gate of the counter. The internal reference supplies a 100 MHz signal through the timebase and through the control logic to control the main gate.

4.3.5.3 The number of input pulses accumulated during the "gate open" interval is a measurement of the input frequency. The count obtained is displayed on the readout. This display may be retained until such time as a new sample is ready to be displayed.

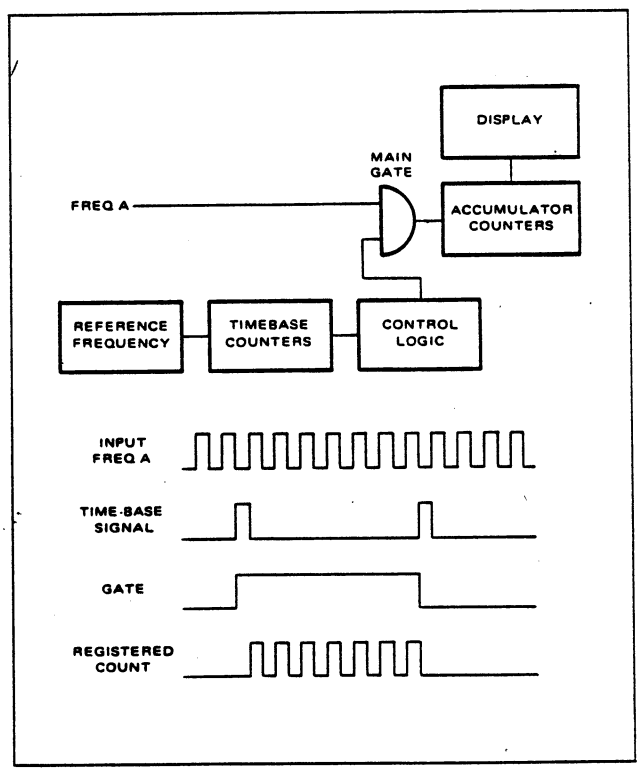


Figure 4.5 - Frequency A

4.3.6 Frequency C (Model 9035A only).

4.3.6.1 In the Frequency C mode, the signal of unknown frequency is applied to the main gate through the prescaler (406793). The prescaler includes an amplifier, automatic gain control circuit, and a divide-by-ten circuit (Figure 4.6).

4.3.6.2 The AGC circuit maintains the required amplifier gain which alleviates the need for manual trigger and range control. The divide-by-ten circuit is necessary to reduce the unknown frequency to a frequency which the main counter circuitry can count.

4.3.7 Totalize.

4.3.7.1 In Totalize mode, the main gate is controlled by the manual START/STOP switch on the keyboard or external START/STOP commands (figure 4.7).

4.3.7.2 With the first Start/Stop command, the control logic opens the main gate allowing the input pulses to be totalized by the counter. Assuming no arithmetic computations, the display is updated every 40 milliseconds. The counter readout then represents the input pulses received during the interval between "start" and "stop".

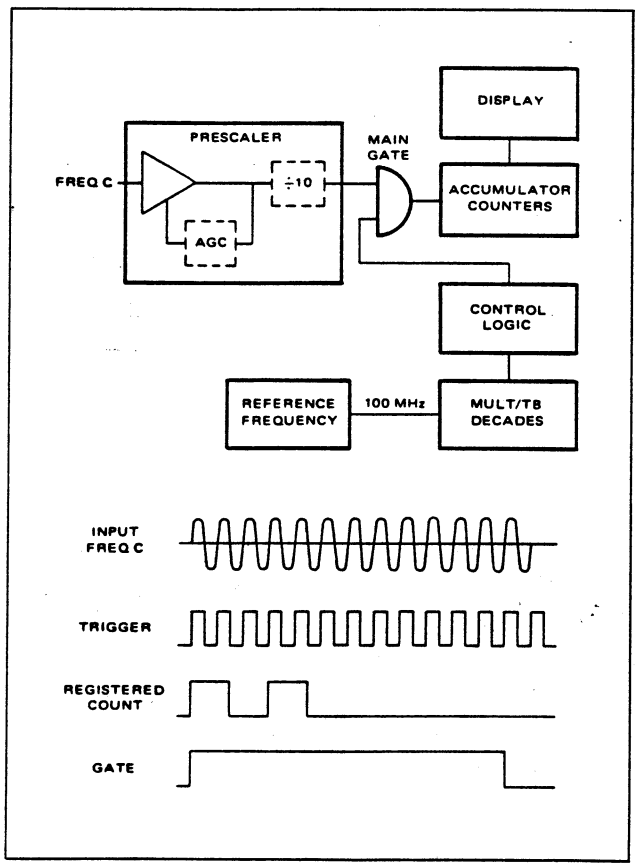


Figure 4.6 - Frequency C

External start/stop commands may be applied via the EXT GATE connector.

4.3.7.3 In this mode, the instrument delivers a scaled output frequency to a connector on the rear panel, SCALED OUT. The output is the input signal frequency scaled by 10^N where N is the multiplier setting.

4.3.8 Time Interval.

4.3.8.1 The Time Interval mode of operation allows measurement of the time between two electrical events to a maximum resolution of 10 nanoseconds (figure 4.8). The first event (start) is connected to channel A and opens the gate. The second event (stop) is connected to channel B and closes the gate. These signals control the main gate through the control logic. Slope and trigger level programming allow variable trigger levels on the + or – slope of the input waveforms. Pulses from the 100 MHz reference circuit are routed to the timebase and to the gate. The pulses occurring during the gate are counted and displayed.

4.3.9 Time Interval Average.

4.3.9.1 Similar to the Time Interval mode of operation, the Time Interval Average mode measures the count

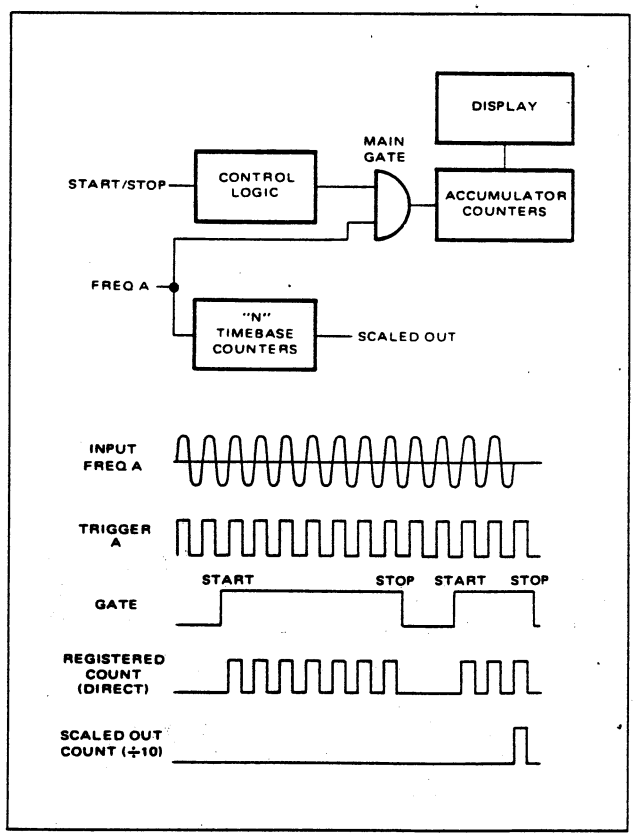


Figure 4.7 - Totalize

accumulated during a multiple of intervals (figure 4.9). It then averages the count by shifting the decimal point and displaying the result. This mode of operation makes it possible to achieve greater resolution and accuracy when measuring time intervals. The A trigger point can follow the B trigger point as close as 50 nanoseconds.

> **NOTE**
>
> In T.I. Average mode, the input signals must be repetitive and asynchronous with the counter's time-base.

4.3.10 A/B (Ratio).

4.3.10.1 This mode is identical in function to the frequency measurement modes, but substitutes an external signal for the reference signal (figure 4.10).

4.3.10.2 The higher of the two frequencies which are to be measured is connected to input A; the lower frequency to input B. Input B is applied to the timebase counters. The higher the timebase selected, the greater the resolution and the longer the measurement time. Two successive positive going edges derived from the timebase counters resulting from input B, open and close the main gate. During the "gate open" interval, the counter counts the trigger pulses derived from input A and the ratio F_a/F_b is then displayed on the readout.

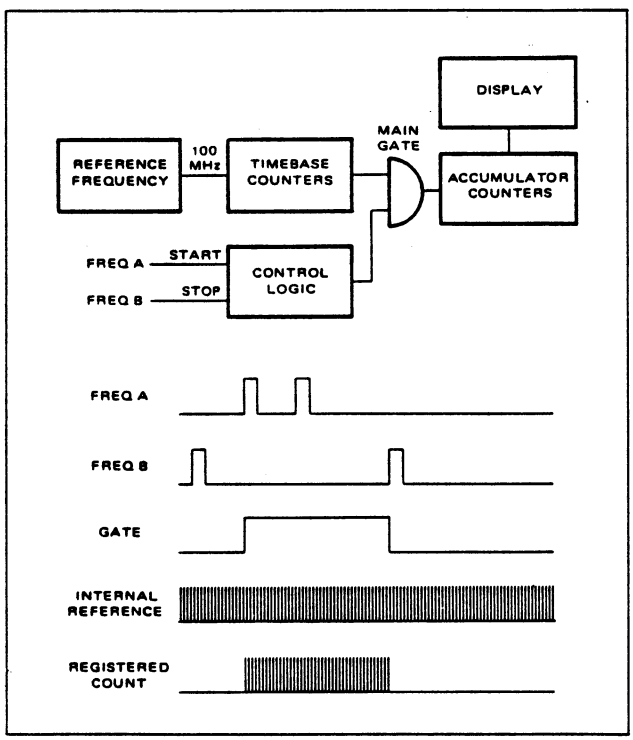


Figure 4.8 - Time Interval

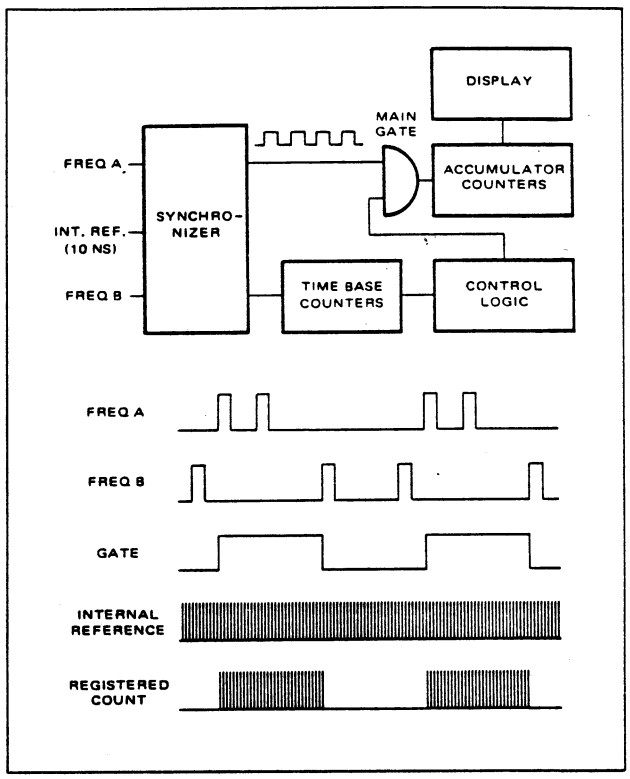


Figure 4.9 - Time Interval Average

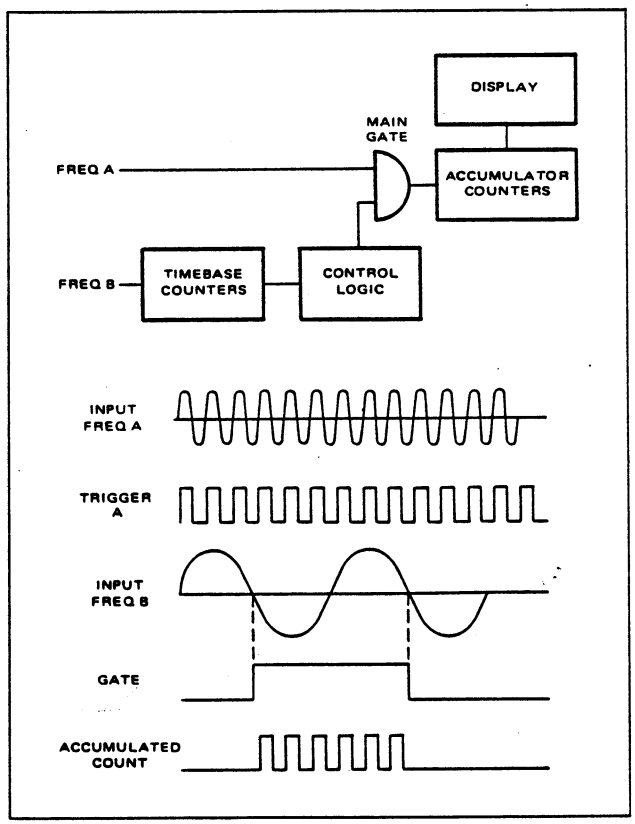


Figure 4.10 - A/B Ratio

4.4 CIRCUIT DESCRIPTION.

4.4.1 The following paragraphs contain descriptions of the circuitry, organized according to the board on which the circuitry is located. The boards with basic signal flow shown between the boards is illustrated in figure 4.11.

4.4.2 Signal Conditioning Modules.

4.4.2.1 The channel A input and channel B input each have identical signal conditioning circuits. The purpose of the circuits is to attenuate, shape, and convert the incoming signal into a squared waveform suitable for the measurement circuitry.

4.4.2.2 For operating convenience, the input to conditioner B can be routed internally from channel A input or channel B input depending on whether COM (common) is selected or not.

4.4.2.3 The conditioner circuitry, shown simplified in figure 4.12, consists of a DC bypass, an attenuator, an amplifier, a Schmitt trigger, a hysteresis compensation circuit, and a slope selection circuit.

4.4.2.4 Referring to the figure, the input signal passes through C1 (or through the relay contact when DC is selected). The signal is then attenuated by a factor of 1, 10, or 100 according to the range selected by relays K2, K3, K4, and K5 as shown in the table.

4.4.2.5 The output of the attenuator is routed to one half of the input of a dual input follower circuit (Q1, Q2, and Q3). The other half of the amplifier input is a trigger reference level and is fed by the output of the digital-to-analog converter (DAC). The dual output of the follower drives the Schmitt trigger.

4.4.2.6 The Schmitt trigger is a limited swing, bi-stable circuit that triggers on the rise and fall portions of the input signal and thereby converts the input into a squared waveform. The level at which the circuit triggers is dependent on the reference input supplied by the DAC and is not equal for both the positive and negative going portion of the input waveform; that is, the circuit displays a fixed amount of hysteresis.

4.4.2.7 For measurements of frequency and period, hysteresis is an advantage in that it reduces false triggering at low amplitude levels; for measurement of time interval and time interval average, however, a means of compensating for the hysteresis is needed.

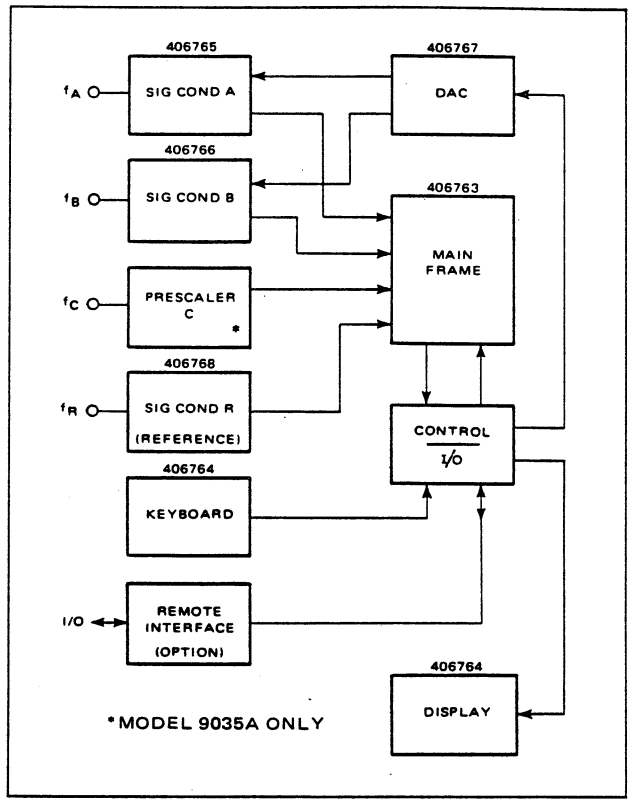


Figure 4.11 - Inter-Board Signal Flow

4.4.2.8 The hysteresis compensation circuit consists of a differential output current source (U1), activated when TI or TIA is selected. The circuit draws a fixed amount of calibrated current from the inverting or non-inverting input circuitry of the Schmitt trigger according to whether + slope is selected or not. The result is to cause the trigger circuit to trigger at the same voltage level on the positive and negative slope of the input signal.

4.4.2.9 The Schmitt trigger produces two squared waveform outputs, one in phase with the input signal and the other 180° out of phase. The slope circuit selects which of the two outputs is routed to the signal conditioning output. The gating consists of diodes CR12 and CR13, biased so that the anodes of the diodes must be positive in respect to the cathodes for the signal to pass through.

4.4.2.10 With + slope at logic True, open collector inverter U1 pulls resistor R51 to common and back biases CR12; the signal flows through CR13 and emitter follower

U2 to the trigger out connector. With + slope at logic false, inverter U1 is not conducting, CR12 is forward biased and open collector inverter U2 pulls R54 down, back biasing CR13. The signal flows through CR12 and emitter follower U2 to the trigger out connector.

4.4.3 Prescaler, F_C (Model 9035A only).

4.4.3.1 This circuitry (figure 4.13) automatically adjusts the amplitude of the channel C input signal to provide a suitable level for the remaining circuitry, divides the input signal frequency by ten, and generates a high, F_C logic signal when an input of the correct frequency range and of sufficient amplitude is applied to the channel C input connector. The circuitry, shown in figure 4.13, consists of an attenuator, RF amplifier, divider, detector, AGC amplifier, trigger circuit, and output signal gate.

4.4.3.2 The attenuator consists of two diodes in series with the input signal flow and three diodes shunting the signal flow. A variable bias voltage, applied in appropriate proportions and supplied by the automatic gain control (AGC), controls the amplitude of the signal that reaches the input of the RF amplifier.

4.4.3.3 The RF amplifier consists of two integrated amplifiers (U5 and U4) operating in series and providing a voltage gain of approximately 100. The amplifier output drives the divider and the AGC circuitry.

4.4.3.4 The divider is a high frequency digital counter capable of operating at near the GHz range. The prescaler divides the frequency output of the amplifier by a factor of 10. The output is controlled by the output signal gate. Scaling is required to reduce the input frequency to a level compatible with the counter circuit.

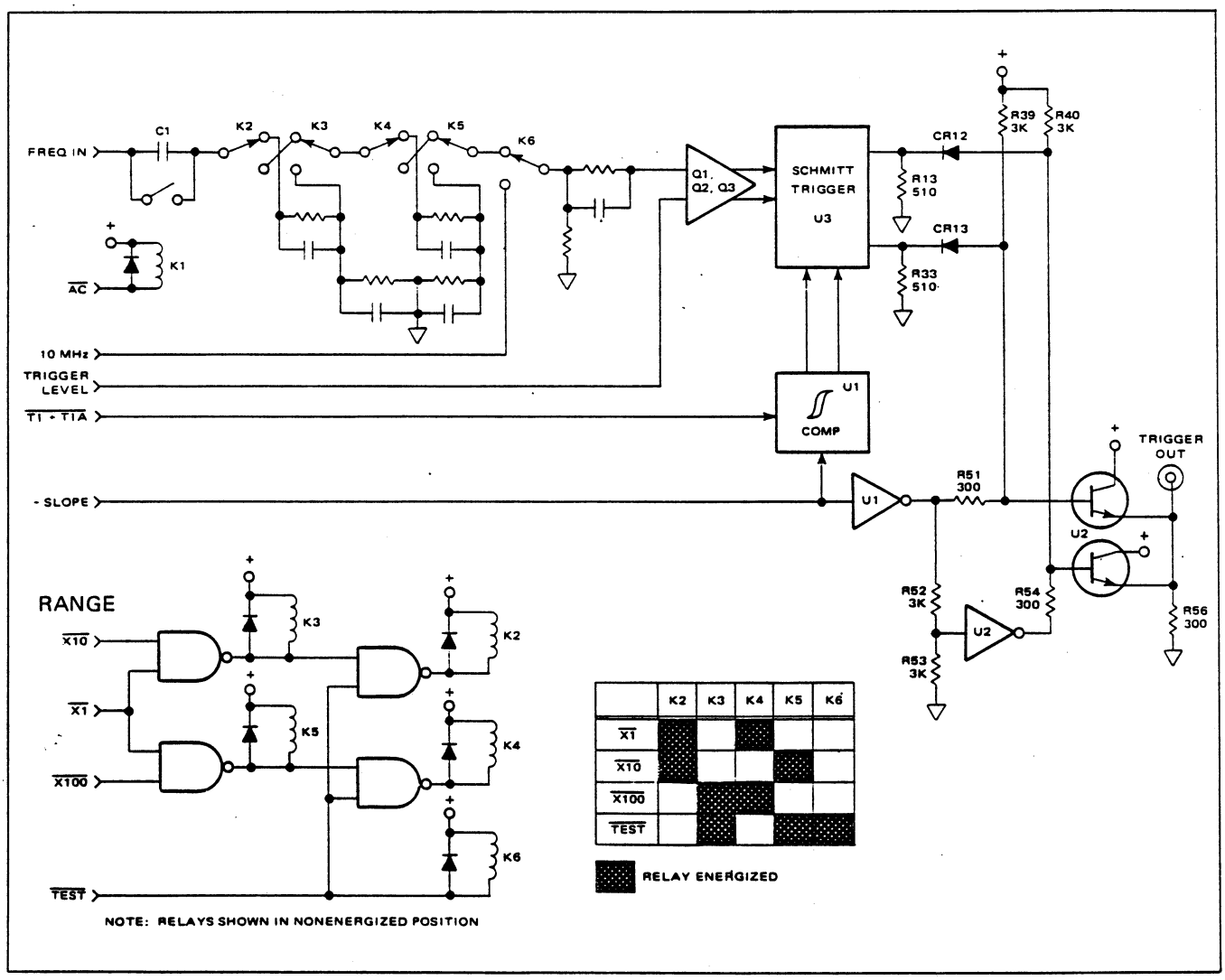


Figure 4.12 - Signal Conditioning Block Diagram

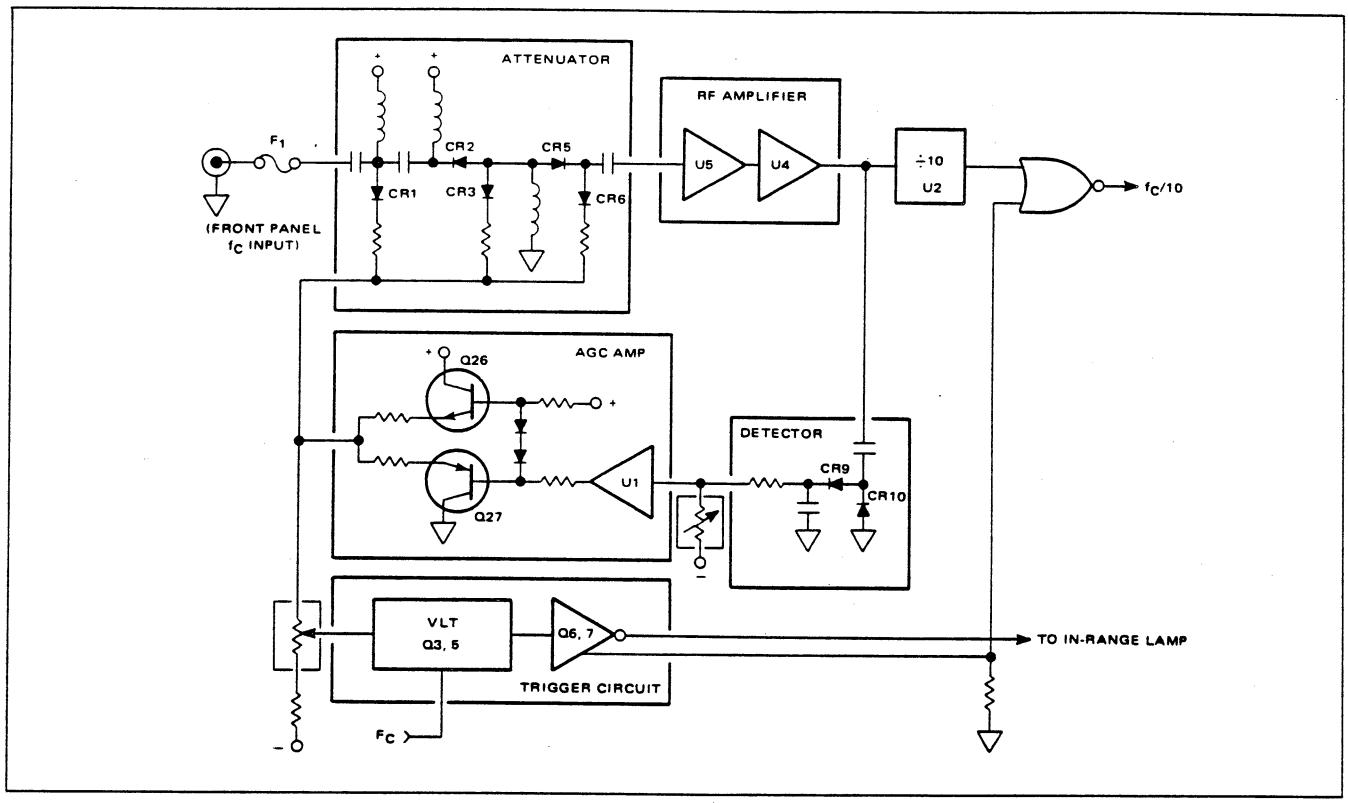


Figure 4.13 - Prescaling Amplifier, F_C (Model 9035A Only)

4.4.3.5 The detector and AGC amplifier generates the operating bias for the input attenuator and provides the input for the trigger circuit. As shown in the figure the AGC feedback path consists of a rectifier CR9, CR10 and an operational amplifier U1, Q26, Q27. The output of the RF amplifier is rectified and filtered to produce a proportional dc level. This dc level is amplified by the AGC amplifier circuitry to provide a control signal having a maximum excursion of from 0 to +10 volts.

4.4.3.6 The trigger circuit monitors the AGC output level and at a predetermined point, produces a logic true output. The circuit is adjusted to produce a true output, when the input signal amplitude is sufficient to operate the counter circuitry. The circuitry is a voltage level trigger and inverter consisting of transistors Q3, Q5, Q6, and Q7. The output lights the front panel IN-RANGE light.

4.4.4 DAC Board.

4.4.4.1 The DAC board generates analog trigger levels for the channel A and B signal conditioning boards. The circuitry on the board is shown in block diagram form in figure 4.14 and consists of two 9-bit shift registers, two 9-bit DACs (digital-to-analog converters), two summing amplifiers, a + reference, and a temperature compensation circuit.

4.4.4.2 The input to the channel A shift register is from the microprocessor. When a trigger level is selected, the selected value (in digital form) is serially fed to the shift register. At the completion of the transfer of data, the selected value is applied in parallel to the DAC. The DAC converts the digital information into its analog current equivalent. This is converted to a voltage equivalent by the summing amplifier and routed to the Schmitt trigger of the channel A conditioner. The circuitry for the channel B trigger level generating circuitry operates in the same manner.

4.4.4.3 Each 9-bit shift register consists of an 8-bit shift register and a D type flip-flop wired in series. Each DAC consists of an 8-bit DAC, generating a current output of from 0 to 1.992 mA. A 9th bit, corresponding to the most significant bit provides a current of 2 mA when selected. The summing amplifier totals the input currents and converts the current to a comparable voltage level.

4.4.4.4 The + reference is derived from a portion of a transistor array, using two transistors as forward biased diodes in series with a transistor used as a back biased diode. The array provides a voltage drop of approximately 8 volts. This level is buffered by an operational amplifier (U7) wired in a gain of one configuration. The + reference

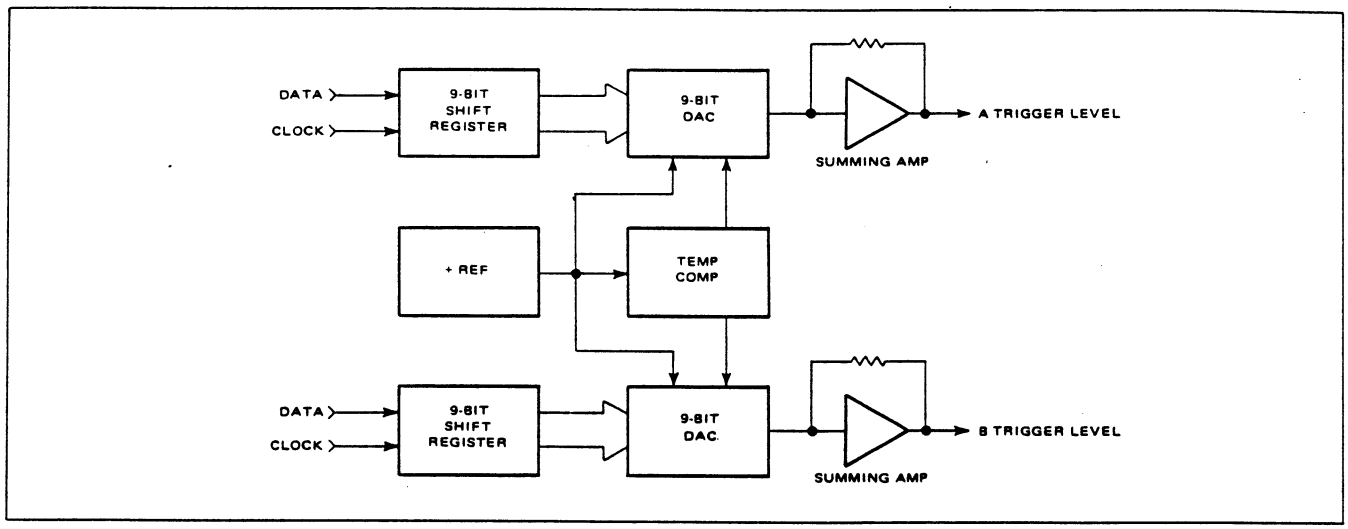


Figure 4.14 - DAC Board

is used by the 8-bit DACs, the MSB current generators and the temperature compensation circuitry.

4.4.4.5 The temperature compensation circuit consists of a voltage divider with two PNP transistors (Q2 and Q3) wired as diodes in series with the divider string. The divider output is used to set the voltage level for the bases of the MSB current generators. The temperature coefficient of the divider tracks with the current generators, making the MSB relatively temperature insensitive across the operating temperature scale.

4.4.5 Reference Multiplier Circuit.

4.4.5.1 The reference multiplier circuit converts the internal reference oscillator (10 MHz) or an external reference (1, 5, or 10 MHz) to a 100 MHz reference signal, used as the timing standard for all measurement functions except A/B and TOTALIZE.

4.4.5.2 The circuitry, shown in block form in figure 4.15, consists of a signal shaping circuit, 10 MHz filter, signal detect/gate circuit, a 5 times frequency multiplier, a frequency doubler, a buffer and a drive circuit.

4.4.5.3 The signal shaping circuit and the 10 MHz filter are in operation only when an external reference is used. With an external reference of 1 volt RMS (–0, +50%) at 1 MHz, 5 MHz, or 10 MHz applied, the signal shaping circuit converts the input into a squarewave of the same frequency. The shaping circuit consists of an inverter, biased to operate in the class A mode, driving two inverters, connected as a Schmitt trigger. This drives a standard T^2L logic level inverter, the output of which is fed to the 10 MHz filter.

4.4.5.4 The 10 MHz filter is an active ringing circuit, consisting of transistors Q1, Q2, and 10 MHz crystal Y1. The square wave output of the shaping circuit is differentiated and the negative spikes from the differentiated signal applied to the base of Q1. The emitter of Q1 drives one side of Y1 (operating in the series mode) causing the crystal to ring at 10 MHz. The collector of Q1 in conjunction with capacitor C6 effectively neutralizes case capacitance of the crystal. The output end of the crystal drives Q2 wired as a common emitter, tuned collector amplifier. The 10 MHz output of the filter is applied to the signal detector/gate. The signal detector/gate circuit is controlled by, and when energized routes through the gate, the output of the 10

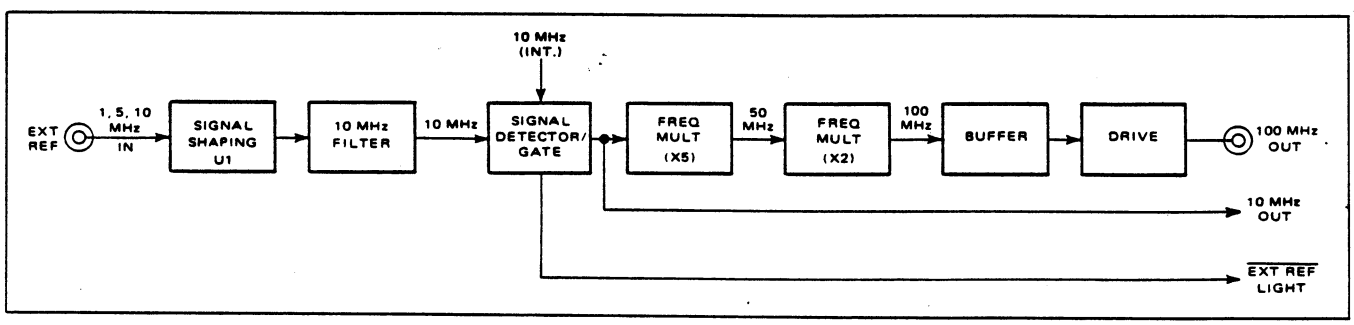


Figure 4.15 - Reference Multiplier Circuit

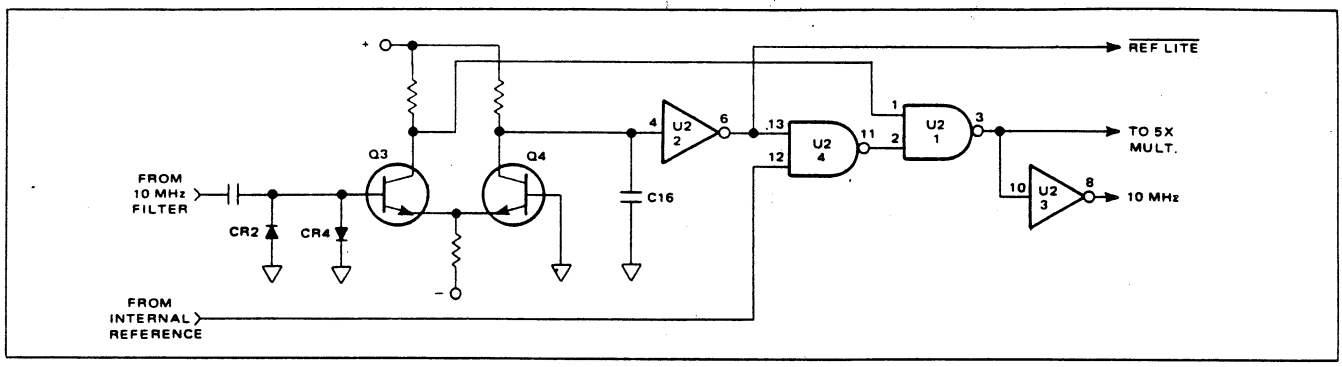


Figure 4.16 - Switch/Gate

MHz filter. In its passive state (no external reference input applied) the gate routes the internal reference oscillator output (10 MHz) through the gate.

4.4.5.5 The gate, shown simplified in figure 4.16, consists of two differentially coupled transistors (Q3 and Q4) and three segments of a quad dual input Nand gate (U2). Because of the additional diode drop (CR4) between ground and the base of Q3, Q3 is biased off and Q4 is biased on when no signal is received from the filter. The logic low output of Q4 is inverted by U2-6 producing a $\overline{\text{REF LITE}}$ logic high (signifying no external reference signal) and biasing U2-13 on, permitting the 10 MHz from the internal reference oscillator to pass through U2-11. The logic high output of Q3 biases U2-1 high, allowing the 10 MHz output of U2-11 to pass through U2-3 to the 5X multiplier. The same signal is inverted by U2-8 and routed to other circuitry and to the rear panel REFERENCE OUT.

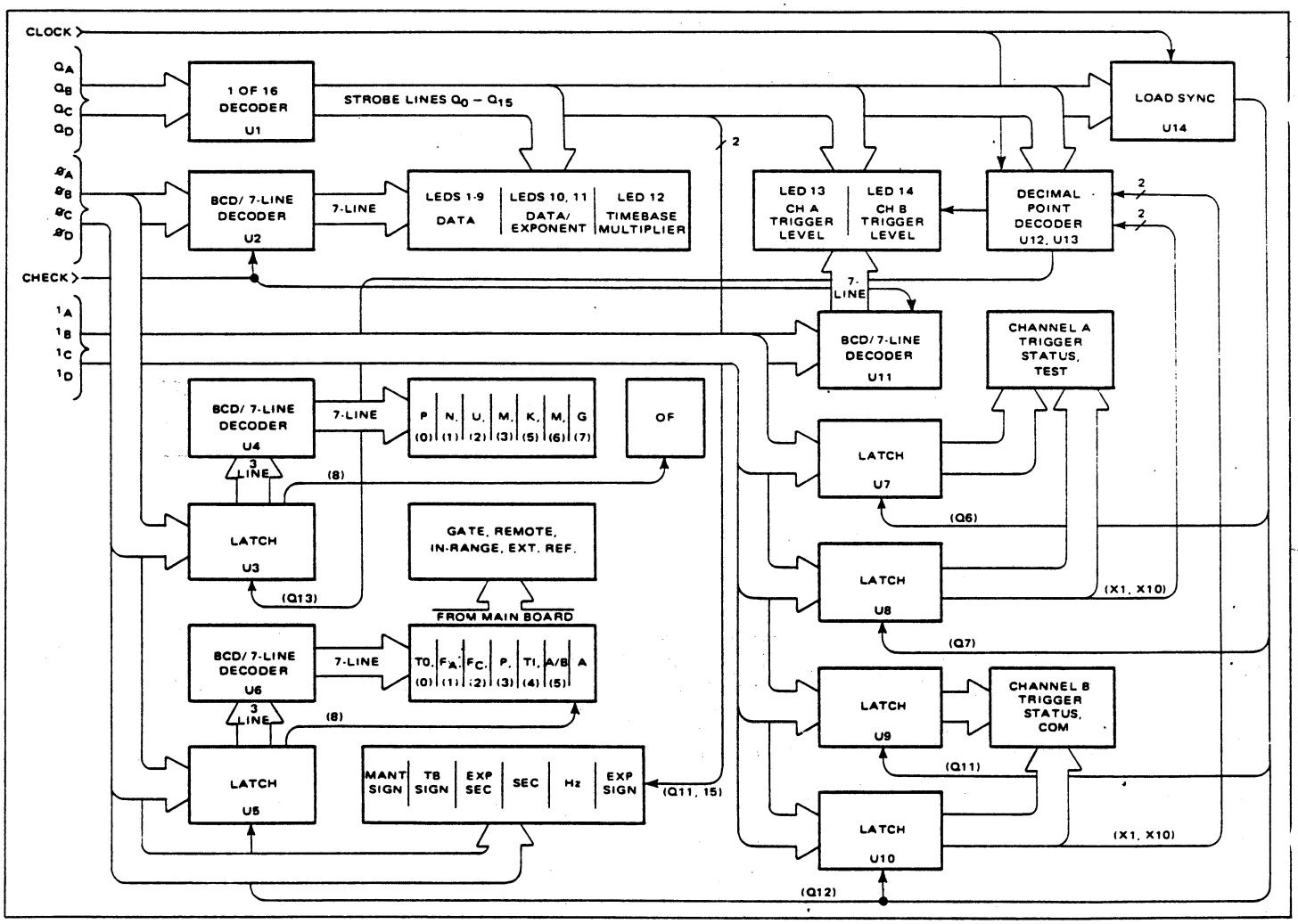


Figure 4.17 - Display Board Block Diagram

Table 4.2 - Display Coding

RAM 1 OUTPUT

Q	1_D	1_C	1_B	1_A	
15	LSD				Trigger Level BCD Coded; Channel B
14					
13	MSD				
12		100	10	1	
11	COM / SEP		− / +	DC / AC	1/0; Channel B
10	LSD				Trigger Level BCD Coded; Channel A
9					
8	MSD				
7		100	10	1	
6	TEST	↓ / ↑	− / +	DC / AC	1/0; Channel A
5					Not Used
4					
3					
2					
1					
0					

FUNCTION CODE

C	B	A	
0	0	0	TO
0	0	1	F_A
0	1	0	F_C
0	1	1	P
1	0	0	TI
1	0	1	A/B
1	1	0	Not
1	1	1	Used

RAM ϕ OUTPUT

Q	ϕ_D	ϕ_C	ϕ_B	ϕ_A	
15	$\overline{\text{Data Sign}}$	$\overline{\text{Timebase Sign}}$	$\overline{\text{SEC}}$ (TB)	EXP Sign	
14	D	C	B	A	Timebase Exponent BCD Coded
13	OF	C	B	A	Multiplier Code BCD Coded
12	$\overline{\text{AVG}}$	C	B	A	Function Code BCD Coded
11	1/X		$\overline{\text{SEC}}$	$\overline{\text{Hz}}$	
10					Data BCD Coded
9					
8					
7					
6					
5					
4					
3					
2					
1					
0					

MULTIPLIER CODE

C	B	A	
0	0	0	p
0	0	1	n
0	1	0	μ
0	1	1	m
1	0	0	
1	0	1	K
1	1	0	M
1	1	1	G

4.4.5.6 When a 10 MHz signal is received from the 10 MHz filter circuit, the signal is clipped by CR2 and CR4 and drives the base of Q3. The collector of Q3 is an inverted square wave of the input signal and is applied to one of Nand gate U2-1. The input signal is also coupled through the emitter of Q3, Q4 to the collector of Q4. The signal is integrated by capacitor C16 to produce a logic high which is inverted by U2-6 to produce a logic low on the $\overline{\text{REF LITE}}$ line (the EXT REF lamp on the front panel lights) and inhibits the internal 10 MHz signal from passing through Nand gate U2-11. The output of U2-11 is logic high enabling the 10 MHz signal from the collector of Q3 to pass through U2-3. As in the case of the switch in the passive mode, the 10 MHz from the output of U2-3 is fed to the 5X multiplier and is routed to other circuits in the instrument.

4.4.5.7 The 5X multiplier consists of transistor Q5 and a buffer Q6, Q7. The 10 MHz square wave input from the switch is differentiated through a C/R network and the positive spikes of the differentiated signal drives Q5 on. The collector circuit is tuned to 50 MHz and rings at this frequency. The 50 MHz output is buffered and squared by Q6, Q7 and routed to the frequency doubler. The output of Q7 drives a differential driver (Q9, Q11) driving a push, push doubler consisting of transistors Q8 and Q10. The output circuit is resonant at 100 MHz and the 100 MHz frequency signal from the output is buffered and squared by transistors Q12 and Q13. The output of Q13 is further buffered by emitter follower Q14.

4.4.6 Display Board.

4.4.6.1 The display board, shown in block form in figure 4.17, is mounted directly behind and is in parallel with the instrument front panel. On the board are all of the visual readouts along with the drivers, decoders, latches, and synchronizing circuitry required to control the readouts. Most of the input data for the display board is supplied in multiplex form across 12 lines from the microprocessor board.

4.4.6.2 The data on these lines is in two forms: multiplexed data and encoded strobe lines. The strobe lines are decoded by the 1 of 16 decoder (U1) and the strobe function is provided by the 16 U1 output lines designated Q0 through Q15. The multiplexed data is supplied to the display board over two separate 4-bit busses 0_A - 0_D and 1_A - 1_D.

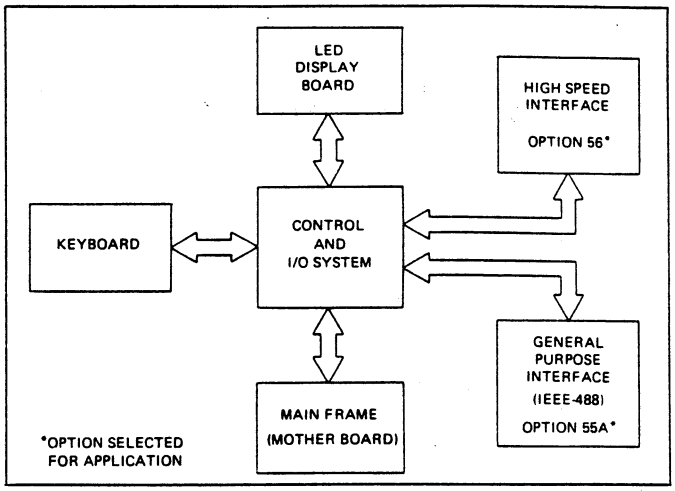


Figure 4.19 - Control and I/O System Distribution

4.4.7 Control-I/O System.

4.4.7.1 The block diagram Figure 4.19, presents the center-position occupied by the Control-I/O System. Physically the Control μP section is configured on PC board 406925 (schematic 721925) located at J8 terminal on the mainframe PCB with bus lines to I/O board 406926 (schematic 721926) located at J7 terminal on the mainframe (PCB 406763). Electrically, the Control and I/O modules operate in unison.

4.4.7.2 *CONTROL-I/O CLOCK.* The timing and synchronization signals required to coordinate the program sequence are generated by the master clock located on the mainframe PCB. The 10 MHz signal inputs at P7-74 is divided down to 5 MHz, then outputs at P7-73.

4.4.7.3 *KEYBOARD.* Every keyboard switch is labelled with the function or control required for complete operation of Model 9000A Counter. The keyboard functions input and output the I/O board through J14 bus to connector P7.

Input Lines	Designator		Function
P7-69	Keybutton Select	1A	Keyboard Matrix
P7-70	" "	2A	Inputs
P7-62	" "	4A	"
P7-65	" "	8A	"
P7-67	Slide Switch Select	1B	"
P7-61		4B	"
P7-66		8B	"
P7-71	Return to Manual or Remote Input	RM	"

Output Lines	Designator	Function
P7-30	$\overline{\text{Keyboard Clock}}$	Strobes the data level at $\overline{\text{KYBD DATA}}$ into the keyboard shift register.
P7-31	$\overline{\text{Keyboard Clock}}$	Serial data path which sequentially sets up the status of the keyboard matrix.
P7-29	$\overline{\text{Keyboard Enable}}$	Enables the keyboard shift register.

4.4.7.4 *DAC.* The input data for the generation of trigger level signals, originates at the keyboard. The output program from the I/O is identified as follows:

Output Lines	Designator	Function
P7-32	TRIG A DATA	The source for trigger level signals are two 9-bit DACs (one for Ch A, one for Ch B). Each DAC is programmed by a serial bit stream, with the level present on the latched data line transferred to the DAC by a momentary transition of the clock line.
P7-33	TRIG A CLOCK	
P7-24	TRIG B CLOCK	
P7-25	TRIG B CLOCK	

4.4.7.5 *MAINFRAME PROGRAMMING LINES.* The mainframe logic and interconnect houses the analog control circuitry where the timer-counter measurements are converted to digital logic. The program lines to the I/O module are labelled as follows:

Input Lines	Input Designator	Function
P7-68	M.F. ACC DATA	Serial Accumulator Data
P7-39	$\overline{\text{GATE A}}$	Gate A
P7-63	$\overline{\text{GATE B}}$	Gate B
P7-6	DATA READY	Accumulator Data Ready
P7-74	10 MHz CLOCK	System Clock Control

Output Lines	Designator	Function
P7-35	CONT REG DATA	Serial Data to Control Register.
P7-36	CONT REG CLOCK	Control Register Clock.
P7-28	REMOTE S/S	Remote Start/Stop.
P7-34	$\overline{\text{M.F. ENABLE}}$	Enable Readings by the Mainframe.
P7-37	$\overline{\text{PARALLEL ENABLE}}$	Enable Accumulator Latches.
P7-38	M.F. CLEAR	Clear Mainframe for New Readying.
P7-76	CONTROLLER	Remote Controller Enable.
P7-41	M.F. ACC CLK	Serial Accumulator Data Clock.
P7-73	5 MHz REF	

4.4.7.6 *HIGH SPEED COMPUTER INTERFACE.* For the automatic systems the control-I/O interfaces with option 56 for remote control of the counter. The I/O program lines are as follows:

Input Lines Connector	Designator	Function
P7-44	$\overline{\text{RMT}}$	Indicates Remote Computer Control is active (low).
P7-46	μP R/W	Defines programming cycle or measurement cycle.
P7-48	TRDY	Data transfer has occured an can be acted upon.
P7-75	$\overline{\text{RESET}}$	9000A is to abort in-process measurement or programming and await new remote instructions.
P7-45	$\overline{\text{HSP}}$	Indicates to 9000A Control that parallel rather than multiplexed data output mode is requested.
P7-47	μP WRD	Indicates end of transfer of data block (MUX mode).
P7-49	INO (μP INS)	Serial data path for remote instructions into the 9000A.
P7-20	μP DOT	Formatted low speed serial data from 9000A.
P7-16	μP IND	Intermediate status data transfer.
P7-14	μP TRO	Control for $\overline{\text{TRDY}}$.
P7-17	μP DRY	Used to mask $\overline{\text{TRDY}}$ done.
P7-15	μP PENB	Forces data transfer at μP speed.
P7-22	μP ESG	Exponent sign.
P7-21	μP MSG	Mantissa sign.
P7-12	μP PXIN	Formatted low speed serial exponent data from 9000A.
P7-19	μP PDCK	Strobe for low speed serial data.
P7-19	μP XCK	Commands and exponent register strobe.

4.4.7.7 *OPTION 06P.* The program lines through the control-I/O system that control the external gate and 50Ω option employ connector J24 as the input-output lines.

Output Lines	Designator	Function
J24-1	SGR	Remote selective gate.
J24-14	SWR	Remote synchronous window.
J24-2	GDR	Remote gate delay.
J24-12	50Ω	Remote 50Ω/1MΩ input impedance.
J24-13	−V	Minus supply voltage.

4.4.7.8 *OPTION 55A GENERAL PURPOSE INTERFACE BUS.* The remote programming from the GPIB interface to the counter are bused to the Control-I/O for execution at

J22 connector. The input-output program lines are labelled as follows:

Connector	Designator	Function
J22-6	BD0	μP buffered bi-directional data lines.
J22-13	BD1	"
J22-7	BD2	"
J22-12	BD3	"
J22-8	BD4	"
J22-11	BD5	"
J22-9	BD6	"
J22-10	BD7	"
J22-15	BA0	μP Address 0
J22-4	BA1	μP Address 1
J22-14	BA2	μP Address 2
J22-1	$\overline{EN4}$	SPE flip-flop control.
J22-5	$\overline{EN5}$	NRFD flip-flop control.
J22-3	$\overline{S0}$	GPIA chip enable.
J22-16	B R/$\overline{W}$	μP R/W
J22-2	B02	μP clock.
J22-17	$\overline{IRQ}$	Interrupt request.
J22-18	GROUND	

4.4.7.9 The seven segment LED display board drive signals generated in the Control-I/O system are bussed to the display PC board from J14. The display block diagram is shown in Figure 4.17 and the display coding in Table 4.2. The program lines are:

Connector	Designator	Function
J14-16	0C	Multiplexed
J14-15	0D	Numeric Data
J14-2	0B	Numeric Data
J14-1	0A	Numeric Data
J14-5	DISPLAY CLOCK	
J14-11	1C	Multiplexed Annunciator Data (BCD)
J14-7	1D	" "
J14-12	1B	" "
J14-6	1A	" "
J14-3	QD	Digit Strobe Count Lines
J14-14	QC	" "
J14-4	QB	" "
J14-13	QA	" "

4.4.7.10 The significant waveforms and signed voltage levels for this subsection are exhibited in Tables 5.34 and 5.35. The program line assignments are detailed on the I/O schematic 721926.

4.4.8 Keyboard.

4.4.8.1 The keyboard (figure 4.20) consists of 32 push-buttons, five (5) 2-position slide switches, one (1) 3-position slide switch, a type 4003 static shift register and some diode logic. The keyboard generates all the local control inputs for instrument operation.

4.4.8.2 The Check, Remote, S/S, Initialize, and the Norm/Hold switches are single line command type switches and control circuitry on the mainframe. The remainder of the switches, in conjunction with the shift register, produce multiplexed signals that are fed to the microprocessor.

4.4.8.3 The twenty eight multiplexed pushbutton switches have four output lines (A1, A2, A4, A8) and the five multiplexed switches have four output lines (B1, B2, B4, B8). These lines are checked on a "time share" basis with first the A lines monitored and then the B lines. The procedure is as follows:

Phase One.

a. $\overline{\text{Keyboard Enable}}$ is set high causing all output lines of U1 to be high.

b. If any of the multiplex keys are pressed, a logic high is produced on one of the A output lines.

c. A high level on an A line causes the μP to set $\overline{\text{Keyboard Enable}}$ low, set in a 1, and shift the 1 through the shift register. For example, if AUTO is selected (S28), line A8 goes high when U1 output Q6 goes high. The μP decodes the information and selects AUTO (this selection would require that a Trigger Level command have been previously selected).

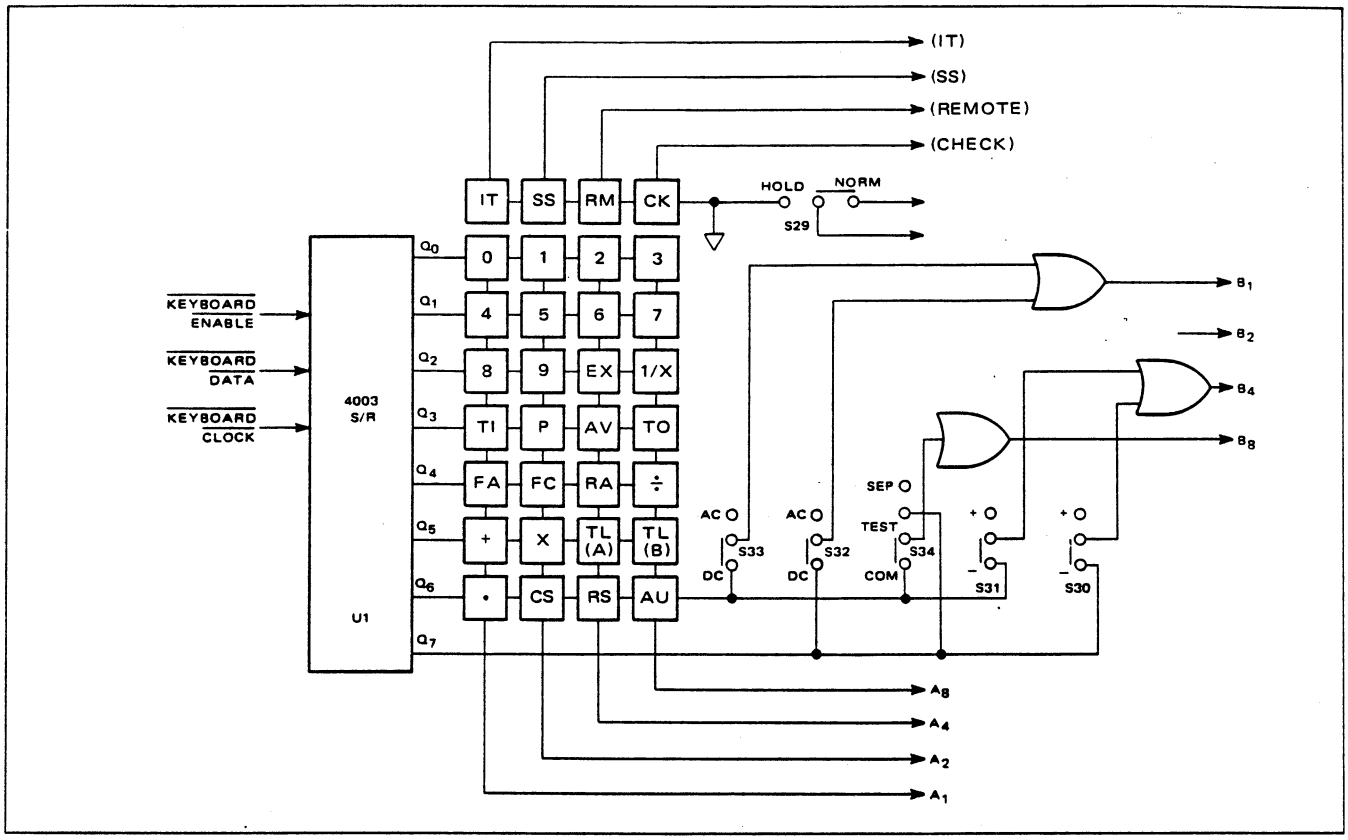


Figure 4.20 - Keyboard

Phase Two.

a. If no button were pushed (as in the previous example), after a given time period the μP strobes lines Q6 and Q7 and reads the positions of the multiplexed slide switches.

4.4.9 Mainframe.

4.4.9.1 The mainframe is the logic and interconnection board of the instrument. On the board is located the accumulator counters, shift register, timebase counters, steering gates, program control, main gate, control logic, synchronizer, marker logic, start/stop circuitry, initialize circuitry, reset logic, and the power supply. The board provides the majority of interconnections between the plug-in boards and contains a large portion of the digital circuitry.

4.4.9.2 *Accumulator Counters.* The accumulator counters count a frequency applied to it and consist of one ECL decade circuit and four T^2L dual decade chips. The BCD output of the counters is fed to the latches. The 8th bit of the most significant decade drives a RS flip-flop which generates the overflow bit. The counter is reset by the clear line.

4.4.9.3 *Latches.* The latches receive the data from the counters in parallel form and store the data until required by the microprocessor. Data is transferred to the latches when $\overline{\text{UPDATE}}$ is false. Data is transferred from the latches to the microprocessor by a pulse train from either the interface ($\overline{\text{INTERFACE ACCUMULATOR CLOCK}}$) or the microprocessor ($\overline{\text{COMPUTER ACCUMULATOR CLOCK}}$), in serial form (ACCUMULATOR DATA).

4.4.9.4 *Timebase Counters.* The timebase counters consist of an ECL decade divider, a T^2L decade divider, a programmable, divide-by-10^N, MOS divider and a D flip-flop. In conjunction with in and out steering gates, the timebase counters can be programmed to divide a frequency routed to it by a factor of 10^0 to 10^9. The D flip-flop is used in all operating modes except the TIA function and provides reclocking of the timebase output.

4.4.9.5 *Main Gate.* The main gate is a dual input ECL NOR gate, one input of which receives the output of the counter steering logic and the other input receives the output of the control logic circuitry. The gate controls the flow of input pulses to the accumulator counter.

4.4.9.6 *Control Logic.* The control logic consists of two T^2L D flip-flops, two ECL D flip-flops, and an assortment of gates and inverters. The control logic generates the gate

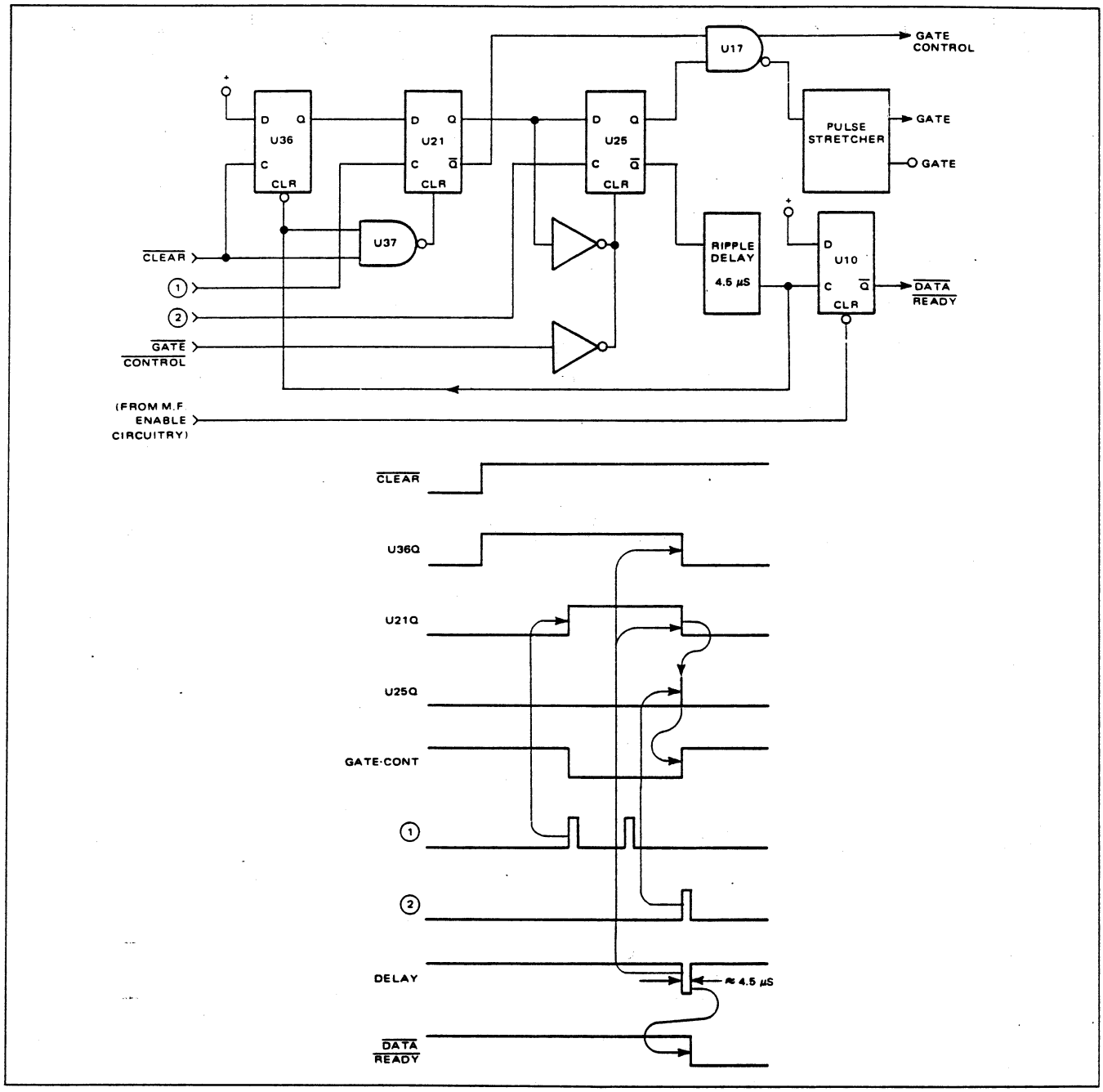


Figure 4.21 - Gate Control

control signal, the DATA READY signal, the gate light control signal, the GATE signal on the rear panel, and, with PARALLEL ENABLE, the UPDATE signal. Referring to figure 4.21, the circuitry is armed when CLEAR goes high setting U36Q true. A positive going edge at input (1) sets U21Q high and U21$\bar{Q}$ low setting the gate control signal false and enabling the GATE circuit. This state continues regardless of what the (1) input level is. A positive going edge at (2) sets U25Q high, setting the gate control signal false and inhibiting the GATE circuit. At the same time U25$\bar{Q}$ goes low generating a 4.5 microsecond negative going ripple delay pulse. The leading edge of the pulse clears U36 and U21 which in turn clears U25. The completion of the gate control also initiates the pulse stretcher. This delay circuit generates a 10 millisecond pulse that sets a minimum limit on the period that the gate line (used to drive the front panel GATE lamp) is on. This circuitry also buffers the output of the gate control line for use on the rear panel (GATE, INT). At the completion of the ripple delay pulse, the DATA READY line goes low informing the microprocessor and the interface that the data in the accumulator counters is complete.

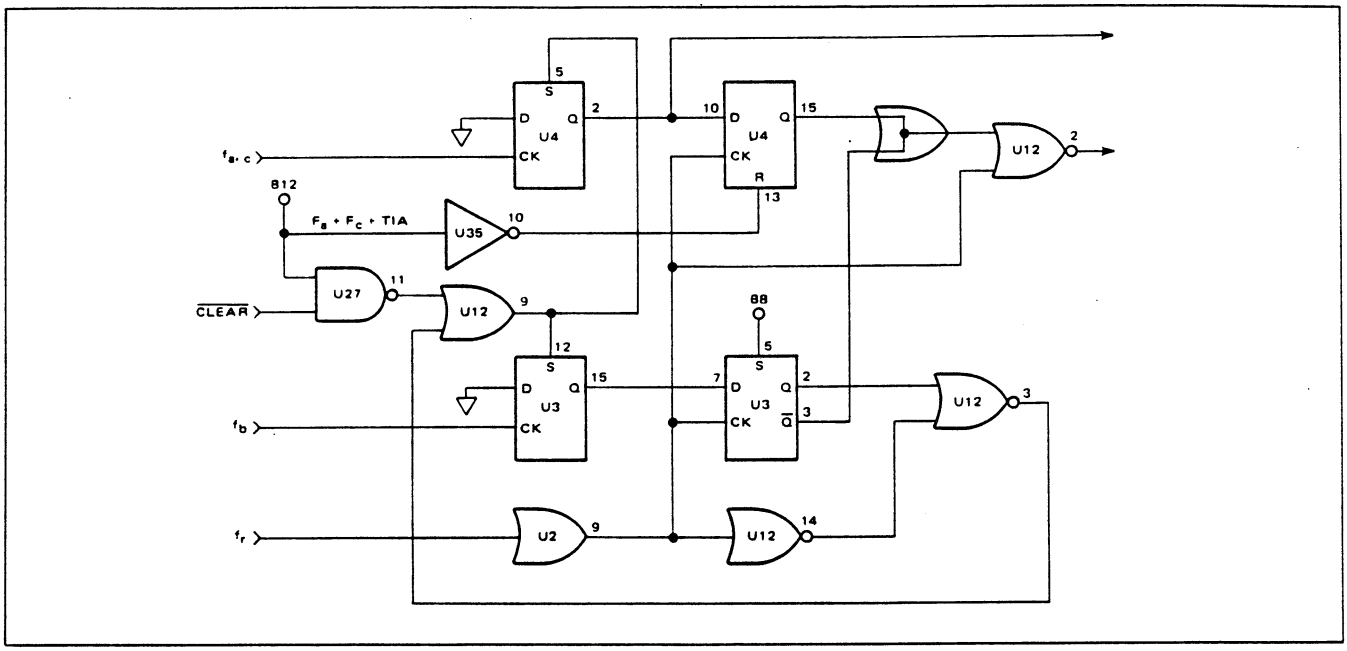
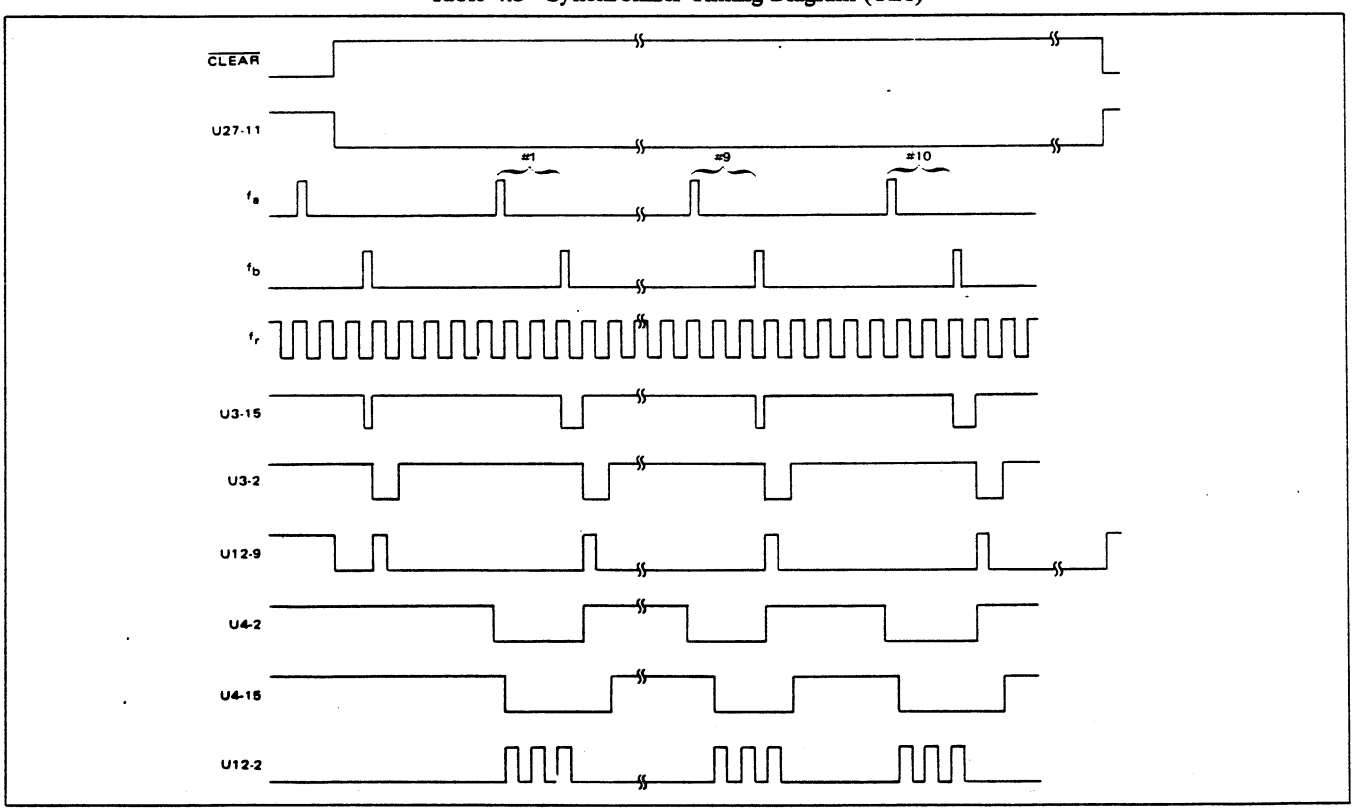


Figure 4.22 - Synchronizer

Table 4.3 - Synchronizer Timing Diagram (TIA)



4.4.9.7 *Synchronizer.* The synchronizer is used to synchronize the gate inputs to the internal clock for Time Interval Average measurements. The circuit, shown in figure 4.22, consists of four ECL D type flip-flops with ECL and T^2L gates.

4.4.9.7.1 The operating sequence starts when $\overline{\text{CLEAR}}$ goes high and an f_b pulse is received, arming the synchronizer circuitry. The sequence then proceeds as illustrated in table 4.3 and described in table 4.4.

Table 4.4 - Synchronizer Operation TIA

Step	Sequence	Note
1.	$\overline{\text{CLEAR}}$ goes high U27-11 goes low U12-9 goes low	During this period $\overline{\text{CLEAR}}$ goes high signaling the start of a new measurement cycle. The f_b signal input initiates the arming sequence which occurs in the following two clock pulses.
2.	f_b goes high (pulse) U3-15 (Q) goes low	
3.	f_r (clock) goes high U3-2 (Q) goes low U12-9 goes high U3-15 goes high	
4.	f_r (clock) goes low U12-9 goes low	
5.	f_r (clock) goes high U3-2 (Q) goes high	
6.	f_a goes high (pulse) U4-2 goes low	Steps 6-11 perform a single Time Interval measurement. This sequence of steps is repeated ten times or a multiple thereof depending on the timebase multiplier selected, to determine the Time Interval Average of the input signals.
7.	f_r (clock) goes high U4-15 goes low U12-2 clock signal	
8.	f_b goes high (pulse) U3-15 goes low	
9.	f_r (clock) goes high U3-2 goes low U12-9 goes high U3-15 goes high U4-2 goes high	
10.	f_r (clock) goes low U12-9 goes low	
11.	f_r (clock) goes high U3-2 goes high U4-15 goes high	
12.	$\overline{\text{CLEAR}}$ goes low U27-11 goes high U12-9 goes high	This step resets the logic circuitry at the completion of the TIA measurement cycle. At the completion of the $\overline{\text{CLEAR}}$ low signal, the entire sequence repeats starting with step 1.

4.4.9.8 *Program Control.* The program control consists of three 8-bit shift registers wired in series. The input data (control register data) and the shift clock (control register clock) signals originate at the μP. The program control circuit supplies the control data for the steering gates, control logic, and the timebase.

4.4.9.8.1 The control data is in binary form and is available across 24 control lines. The data changes according to function and timebase selected as shown in table 4.5.

4.4.9.9 *Steering Gates.* The steering gates are ECL NOR gates in every instance except timebase out. The purpose of

Table 4.5 - Control Register Codes

CONTROL REGISTER (HOME STATES)

		Timebase Control Bits									Mode Control Bits											
	B	2	4	13	19	16	17	18	14	15	1	3	5	6	7	8	9	10	11	12	20	21
FUNCTION	F_A	1	1	1	0	1	0	1	0	0	0	0	1	0	1	1	1	1	0	1	1	1
	F_C	1	1	1	0	1	0	1	0	0	1	0	1	0	1	1	1	1	0	1	1	1
	P	1	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	1	0	0	1	1
	TI	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	1	0
	PA	1	0	0	0	0	0	0	1	0	0	1	1	0	1	1	0	1	1	0	1	1
	TIA	1	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	1	1	1	1	0
	A/B	1	1	0	0	0	0	0	1	0	0	0	1	0	0	1	1	1	1	0	1	1
	TOT	1	1	0	0	0	0	0	0	1	0	0	1	1	1	1	0	1	1	0	0	1

	B	2	4	13	19	16	17	18	14	15
TIMEBASE (F_A, F_C, P, TI)	+ 1	C				1	1	1	0	0
	0					1	1	0	0	0
	− 1					1	0	1	0	0
	− 2					1	0	0	0	0
	− 3					0	1	1	0	0
	− 4					0	1	0	0	0
	− 5					0	0	1	0	0
	− 6	A				0	0	0	0	0
	− 7*	B				0	0	0	1	0
	− 8*	D				0	0	0	0	1

*P, TI only

A	2	4	13	19
P, TI	0	1	0	1
TIA, PA	1	0	0	1
F_A, F_C, A/B, TOT	1	1	0	1

B	2	4	13	19
TIA, PA	1	0	0	0
P, TI	0	1	0	0
OTHER	1	1	0	0

	B	2	4	13	19	16	17	18	14	15
MULTIPLIER (PA, TIA, A/B, TOT)	0	D				0	0	0	0	1
	+ 1	B				0	0	0	1	0
	+ 2	A				0	0	0	0	0
	+ 3	C				0	0	1	0	0
	+ 4					0	1	0	0	0
	+ 5					0	1	1	0	0
	+ 6					1	0	0	0	0
	+ 7					1	0	1	0	0
	+ 8					1	1	0	0	0
	+ 9					1	1	1	0	0

C	2	4	13	19
PA	1	0	1	0
TIA	1	0	0	1
P, TI	0	1	1	0
OTHER	1	1	1	0

D	2	4	13	19
PA, TIA, P, TI	1	0	0	0
A/B, TOT	1	1	0	0

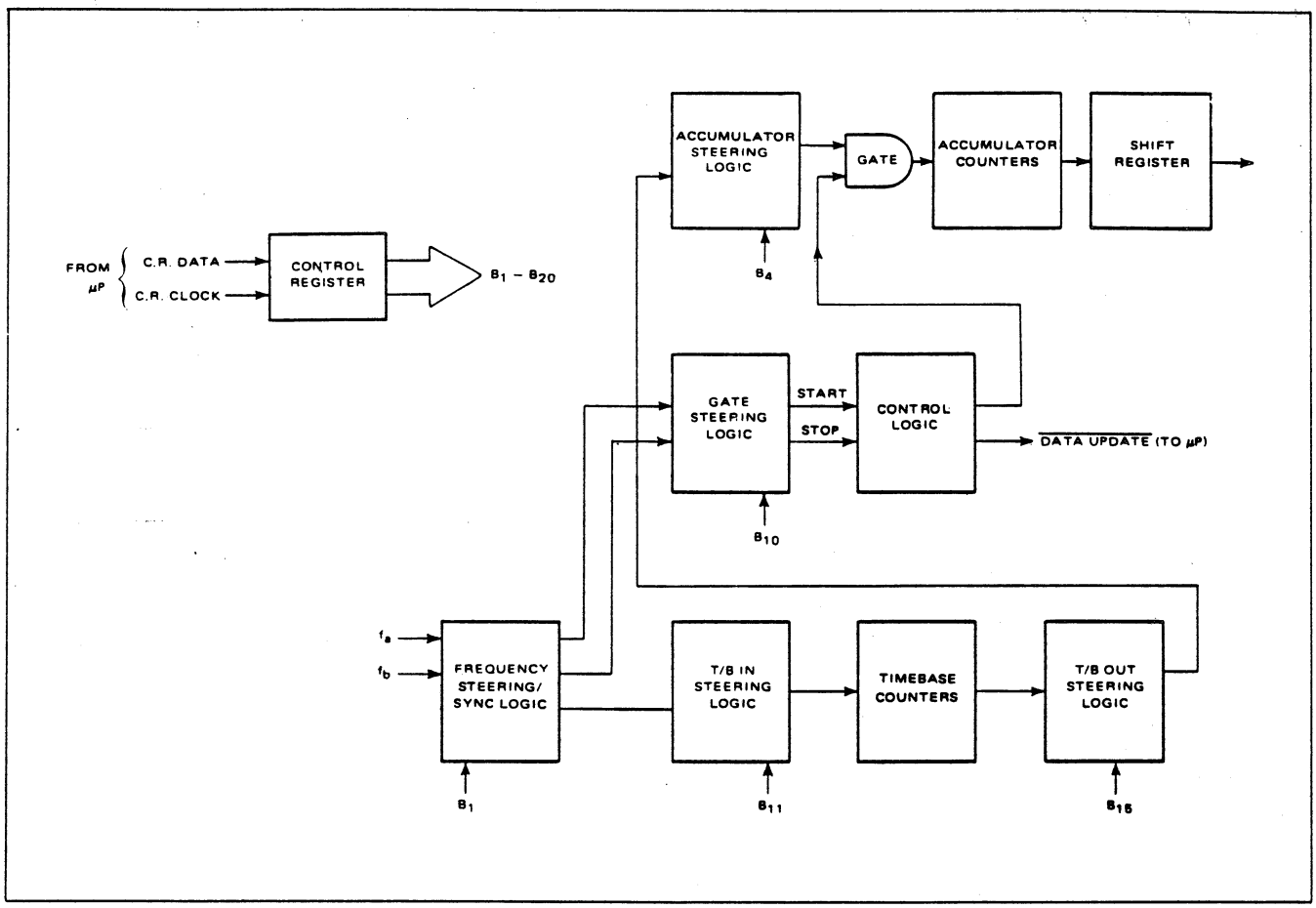


Figure 4.23 - Time Interval Signal Routing

the gates is to route the input signals and reference signals through the instrument according to the function selected.

4.4.9.10 Shown on figures 4.23 through 4.29 are the various signal routes used in the instrument for the different available functions. Also shown are the activated control lines for the particular function selected.

4.4.9.11 *Marker.* The marker logic consists of a dual ECL D type flip-flop and a differential amplifier. The circuit monitors the channel A and B input lines; when a pulse is received on channel A, the circuit generates a −12 volt level until a pulse is received on the channel B input.

4.4.9.11.1 The circuitry and timing are shown in figure 4.30. When the channel A line goes positive, the first flip-flop Q goes high setting the circuit output at −12. When the channel B line goes positive, the second flip-flop Q is set high, resetting the first flip-flop, which sets the circuitry output back to +3 volts, and resets the second flip-flop.

4.4.9.12 *Start/Stop.* The start/stop circuitry consists of a one-shot circuit, an R/S flip-flop and assorted gates. The circuit is used in the Totalize function and generates a pulse each time the start/stop (S/S) key is pressed on the keyboard. This sets the gate control line low and high, and controls the flow of pulses into the counter.

4.4.9.12.1 The circuitry is shown in figure 4.31. B20 is low, EXT gate is open (high), and $\overline{\text{REMOTE}}$ is high. The S/S switch is normally open causing the output of U26 to be low which causes the output of the F/F to be low and U29 output to be high. This is double inverted through U27 and U18 as a high level to the gate logic.

4.4.9.12.2 Pressing the S/S key sets U26 output high and generates a 7 ms negative going pulse at U31$\overline{\text{Q}}$. This sets the F/F output high but inhibits U29.

4.4.9.12.3 At the completion of the timeout, U29 output goes low causing U18 output to go low. This output remains low until the S/S key is released. Releasing the key resets the flip-flop and returns the circuit output to a high level.

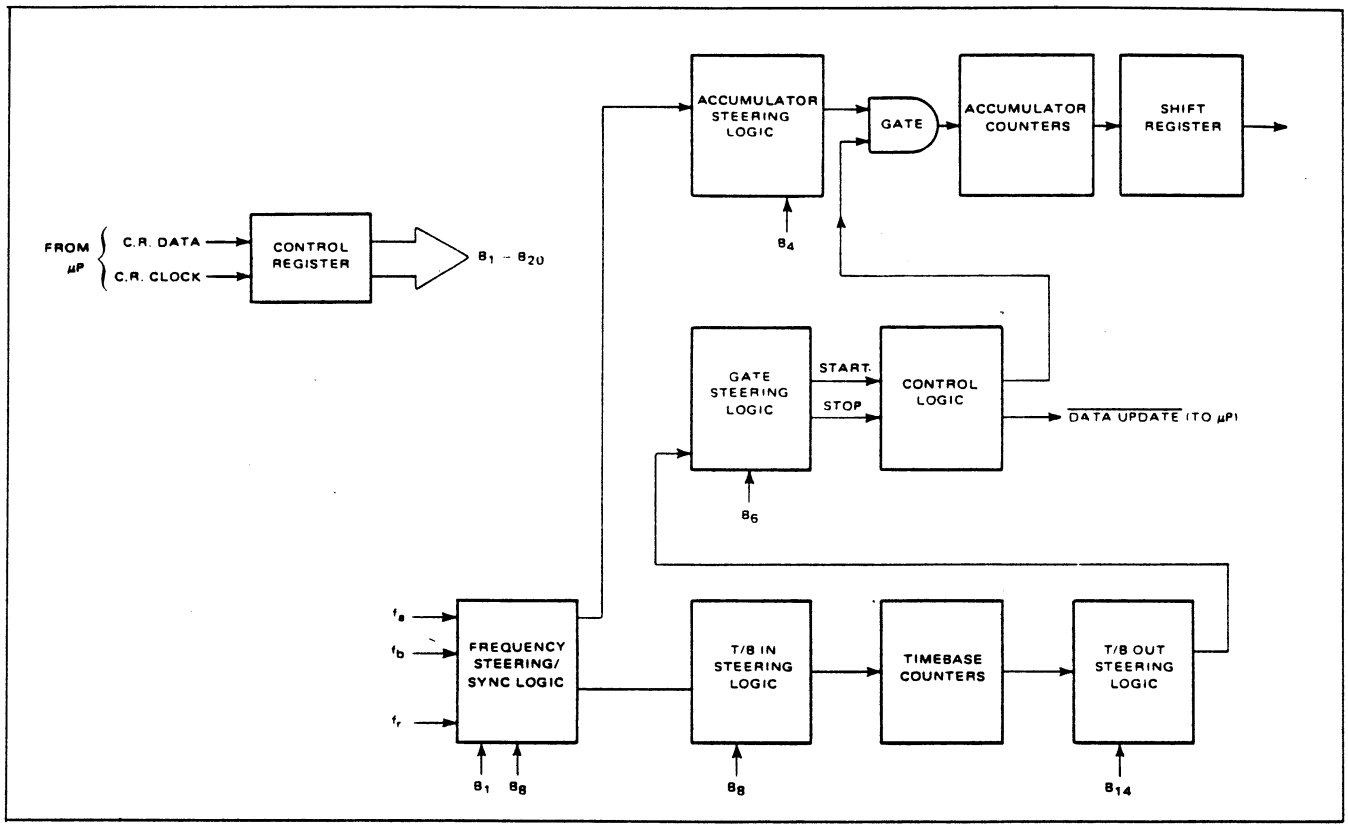


Figure 4.24 - Time Interval Average Signal Routing

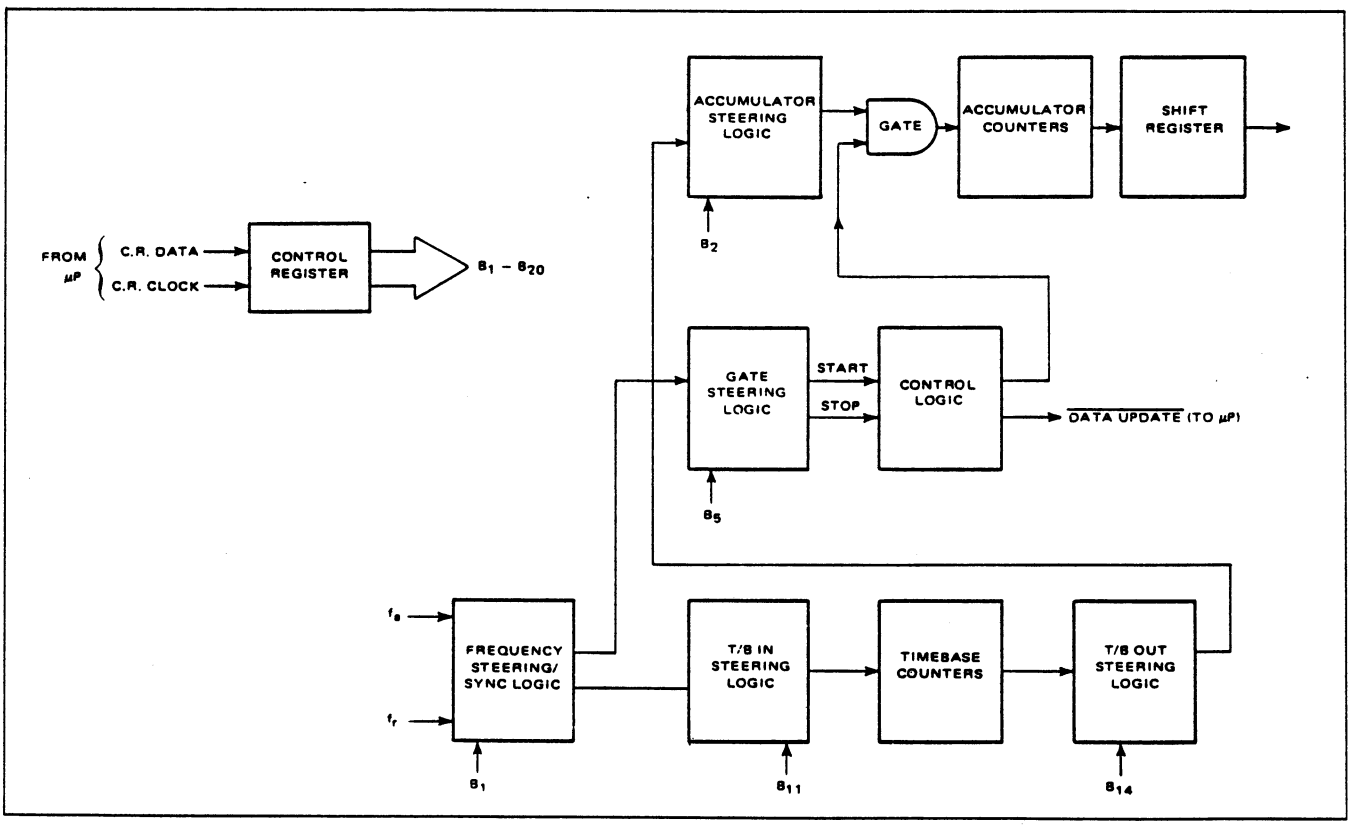


Figure 4.25 - Period Signal Routing

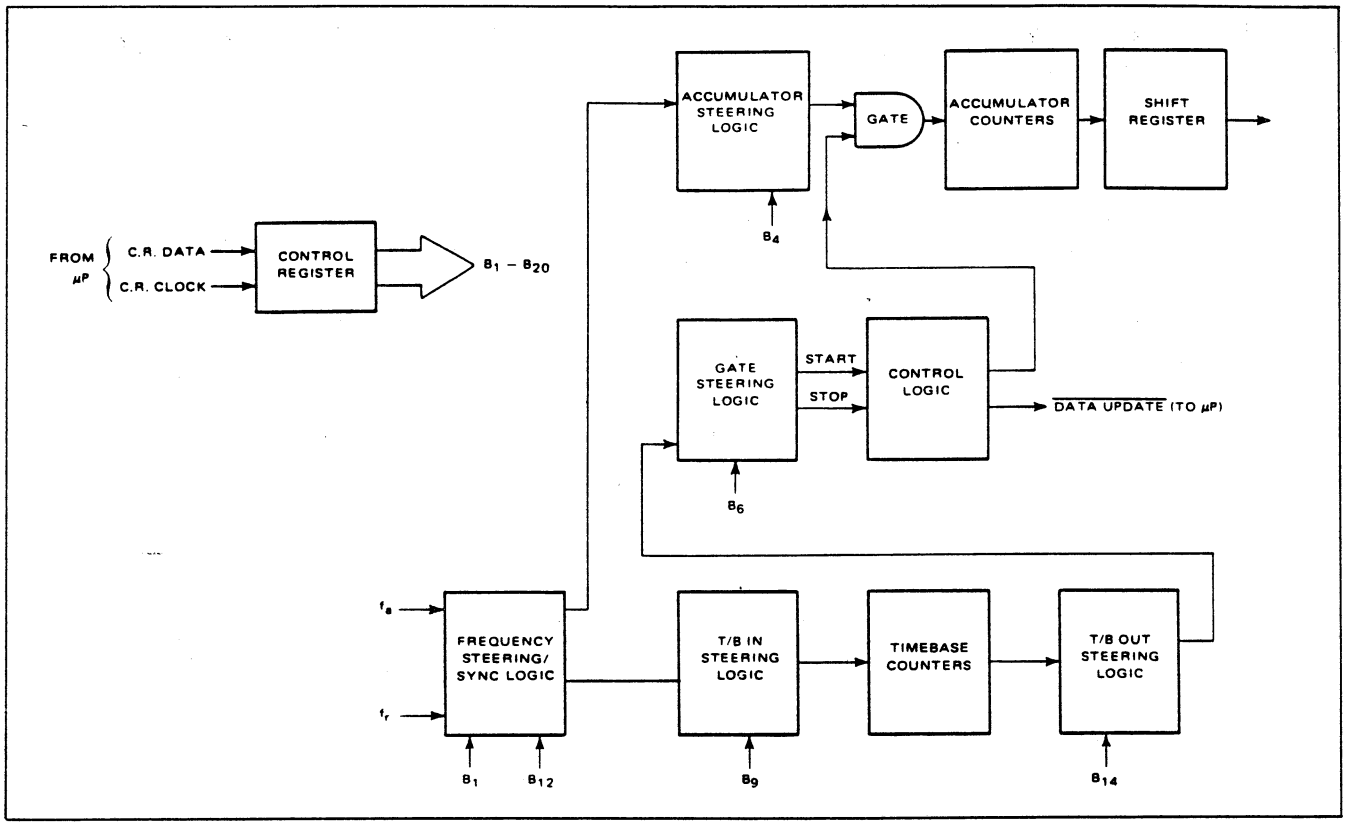


Figure 4.26 - Period Average Signal Routing

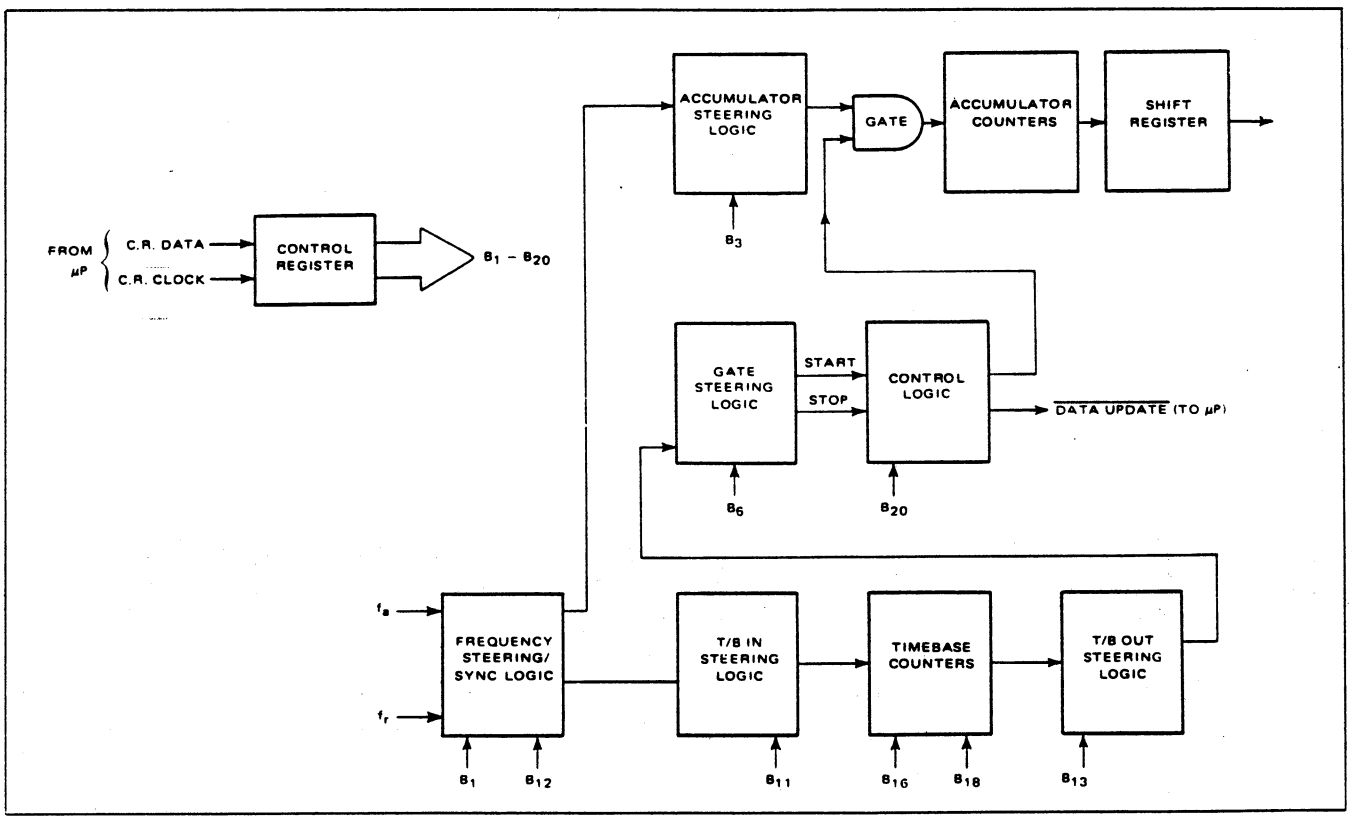


Figure 4.27 - Frequency A Signal Routing

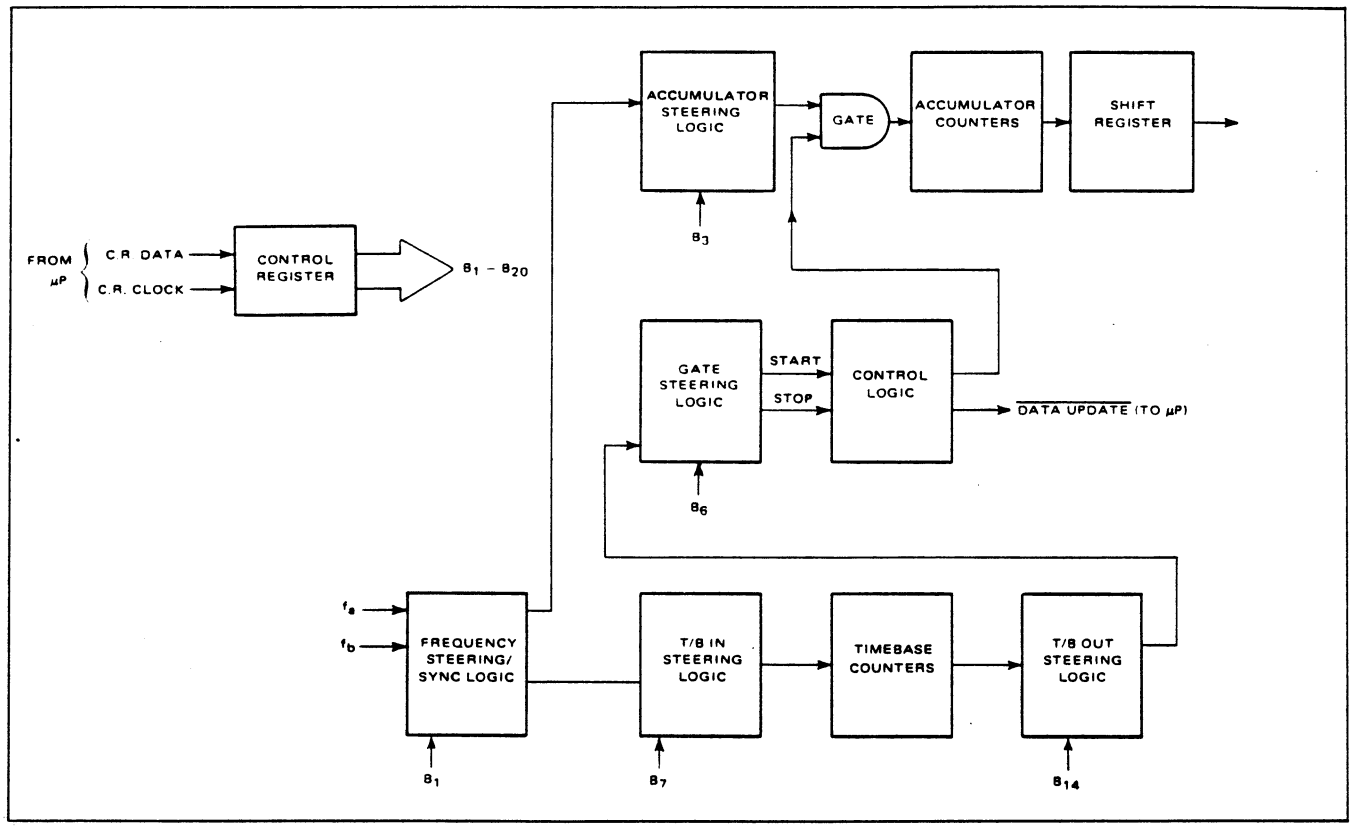


Figure 4.28 - A/B Ratio Signal Routing

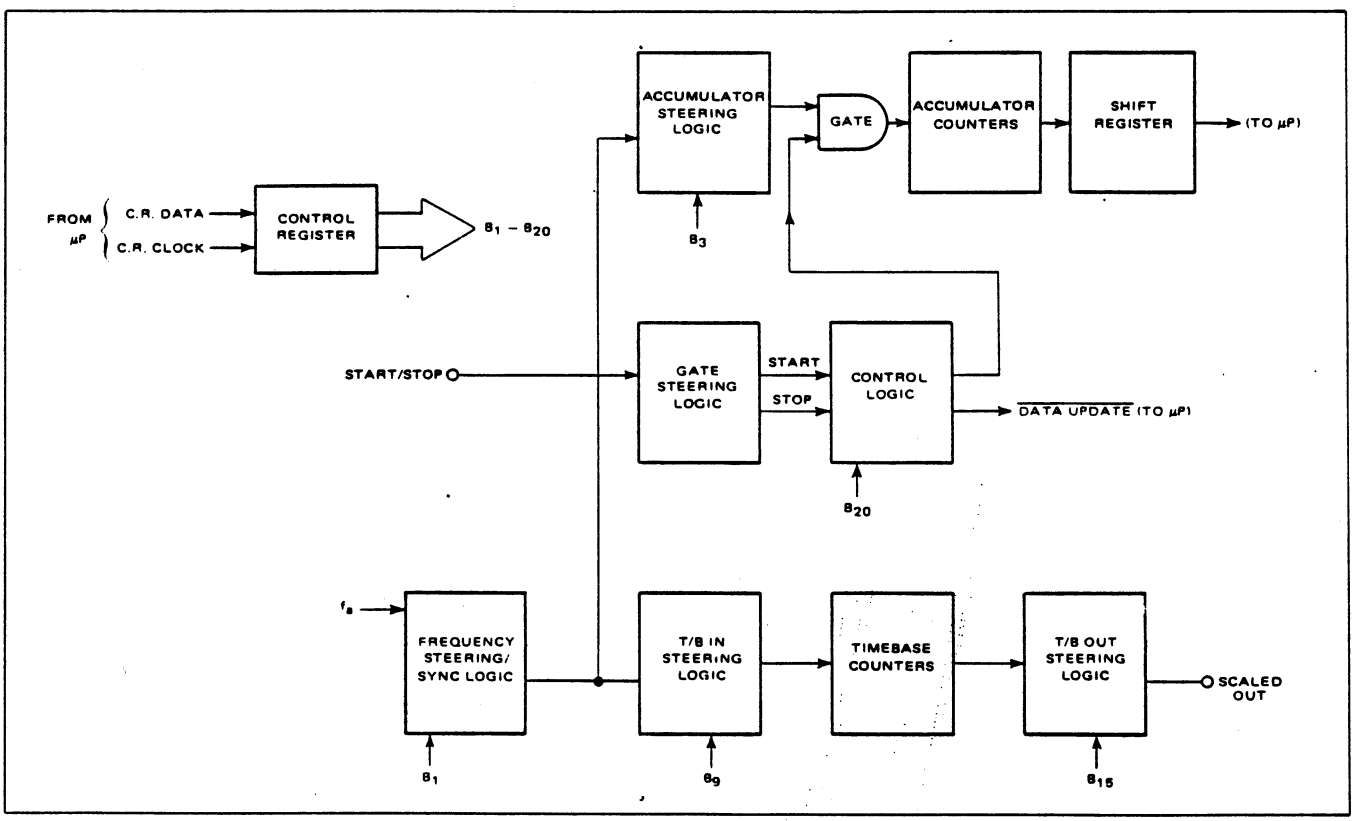


Figure 4.29 - Totalize Signal Routing

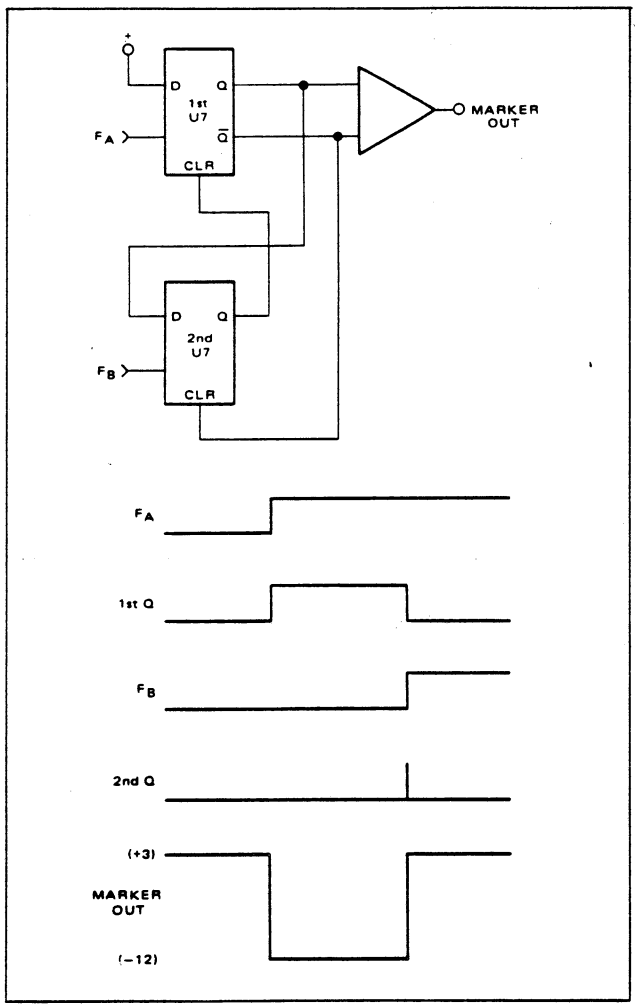


Figure 4.30 - Marker

4.4.9.13 *Initialize.* The initialize circuit is shown in Figure 4.32. When power is applied to the instrument flip-flop U10 is forced into preset (Q high) and RESET is held low for a portion of the RC time constant by the R13, C1 circuit.

4.4.9.13.1 Pressing the IT key generates a negative going level, inverted to a positive going level by U30 and causing the one-shot to generate a 7 millisecond negative going pulse. This pulse is double inverted by gates U30 and U29 resulting in a low $\overline{\text{RESET}}$ for the same time period. Pressing the IT key resets flip-flop U10 by supplying an inverted negative pulse to the clock input.

4.4.9.14 *Signal Detect.* The signal detect circuit consists of two ECL D flip-flops, each driving a transistor inverter. The signal detectors indicate when triggerable signals are being received from the signal conditioners and are used in conjunction with the μP to select the trigger levels.

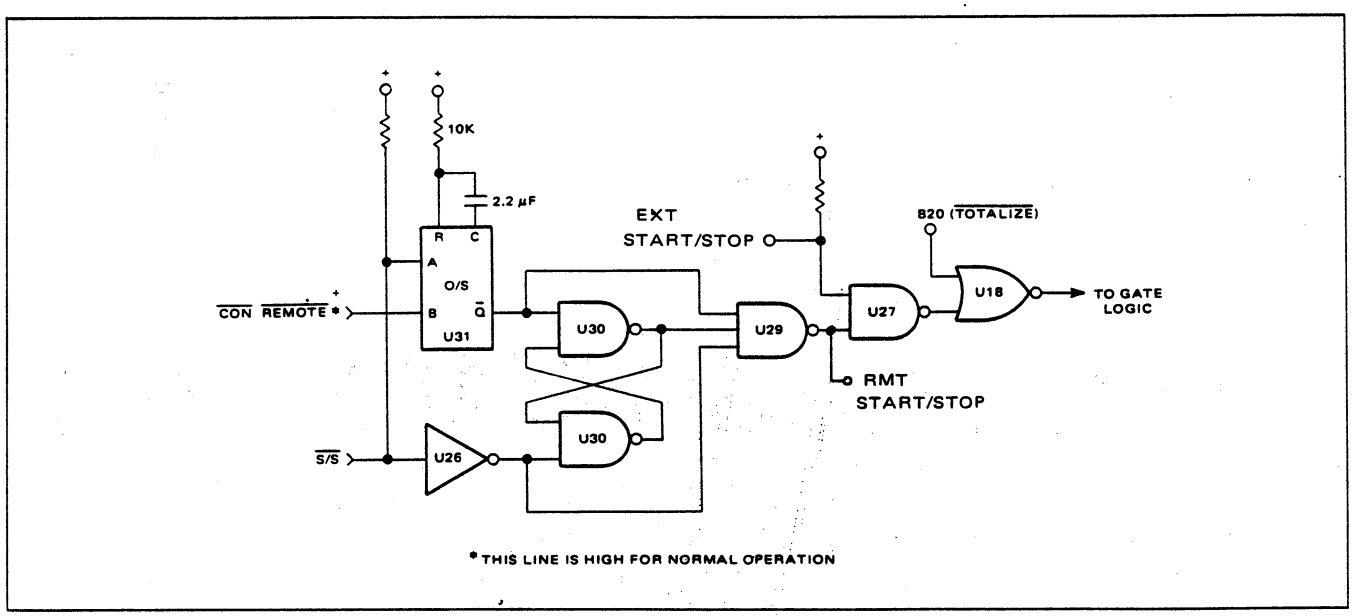


Figure 4.31 - Start/Stop Circuit

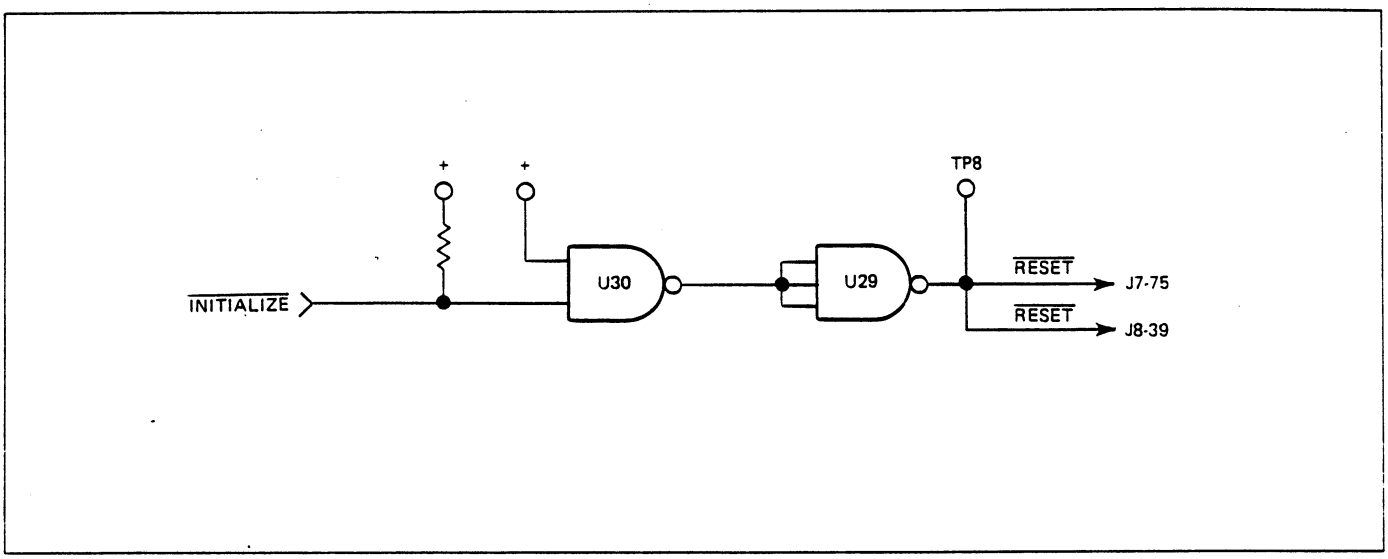


Figure 4.32 - Initialize Circuit

4.4.9.14.1 The circuitry is shown in figure 4.33. The clear line goes high at the completion of each measurement cycle and presets the flip-flop Q outputs true ($\overline{\text{GATE A}}$ and $\overline{\text{GATE B}}$ lines are set high). A positive going pulse at the input of the (A) flip-flop causes Q to go low and $\overline{\text{GATE A}}$ to go low. The operation of GATE B circuitry is the same.

4.4.9.15 *F_a/F_c Gate.* The F_a/F_c gate consists of two ECL dual input NOR gates. The first gate has inputs of f_a and B1; the second gate has inputs of the first gate output and $f_c/10$. With channel C selected, B1 is true, inhibiting the first gate and allowing the $f_c/10$ signal to pass through the second gate. For other functions B1 is false and f_a passes through both gates.

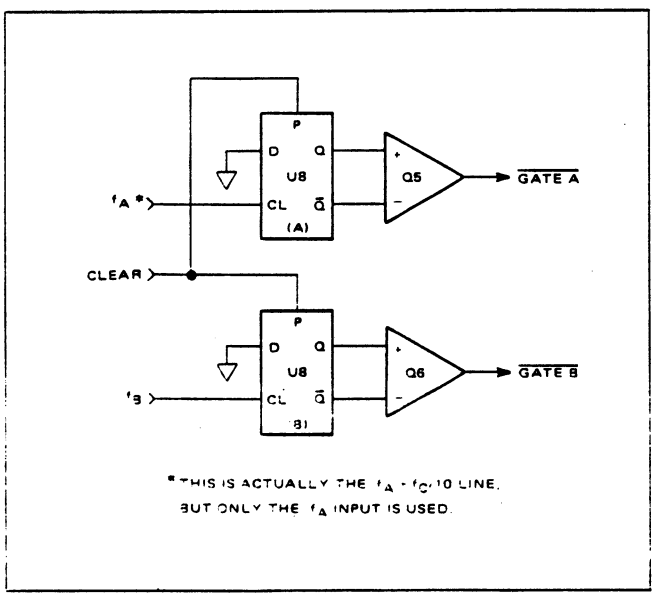


Figure 4.33 - Signal Detect

4.4.9.16 *Clear.* This circuit (figure 4.34) consists of an R/S flip-flop, a delay generator, and sundry inverters and gates. The circuitry generates a $\overline{\text{DATA READY RESET}}$ pulse and, after a delay of 50 milliseconds, generates a $\overline{\text{CLEAR}}$. The $\overline{\text{REMOTE}}$ line, when false, inhibits the $\overline{\text{M.F. ENABLE}}$ line from enabling the circuitry. A $\overline{\text{INT M.F. CLEAR}}$ or $\overline{\text{COMP M.F. CLEAR}}$ low generates a $\overline{\text{CLEAR}}$ low with no delay. The line from the NORM/HOLD switch supplies the current to the delay circuit. When the switch is set to HOLD or REMOTE is selected (see Initialize Circuit) this line is low and the delay circuit is inhibited.

4.4.9.17 *Power Supply.* The power supply consists of a power input module, line capacitors, power switch, transformer, rectifiers, ripple filters, regulators, bypass capacitors and an RF blocking choke. The supply provides the operating voltages for the standard instrument and all options except the oven reference oscillator options; these options have a separate internal supply.

4.4.9.18 Line voltage is applied through the power cable to the power input module. Capacitors C201 and C202 shunt line noise to ground. The "Hot" lead passes through fuse 201 in the module; then both input leads are routed through the DPDT power switch on the front panel. When the switch is on, power is applied to a built-in switch lamp to indicate power is applied.

4.4.9.19 The two power leads are routed back from the power switch to the power module line voltage selector board that determines the routing to the power transformer.

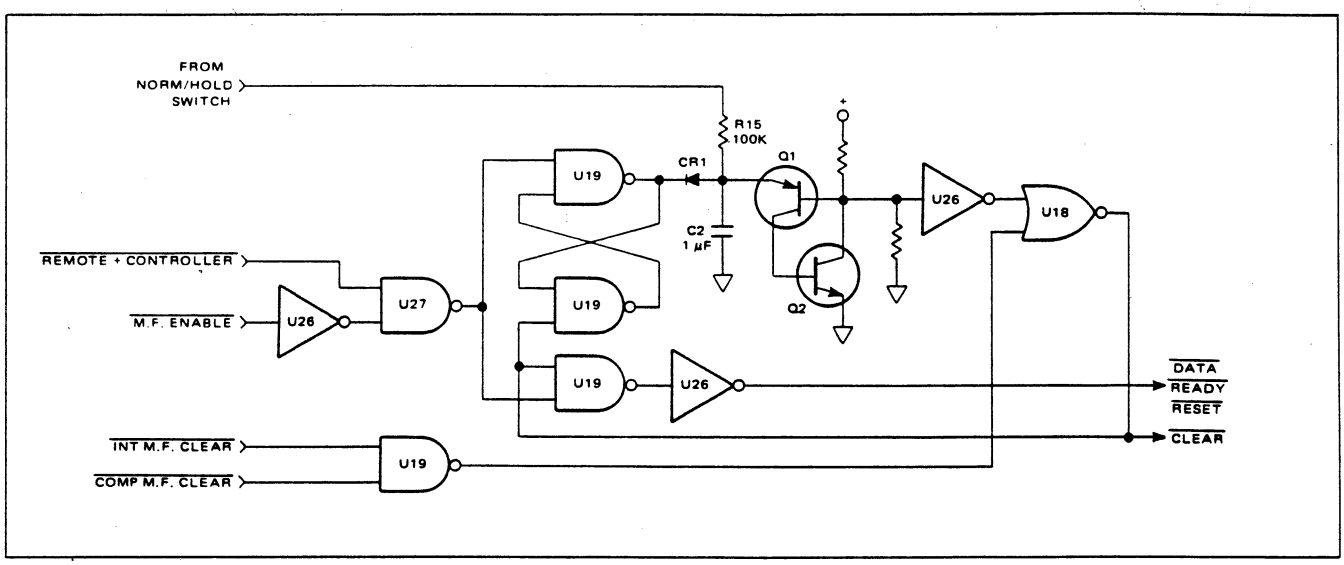


Figure 4.34 - Clear Circuitry

4.4.9.20 Two secondary windings are used; one for the 5.0 and 5.2 volt supplies and the other winding for the +12 and −12 volt supplies. The 5 volt supplies are powered by a positive full wave rectifier, filtered by two 10,000 μF capacitors and a 2.2 μF capacitor. The output is routed to four integrated five volt regulators, three wired to provide a fixed +5 volt output and one wired to provide an adjustable 5.2 volt supply. The 5.2 volt supply is used to power the ECL circuits in the instrument.

4.4.9.21 The other winding drives a positive and a negative full wave rectifier. The plus supply powers a fixed +12 volt integrated regulator and the minus supply powers a fixed −12 volt integrated regulator.

4.5 REFERENCE OPTION SUPPLY.

4.5.1 The reference option supply is a single printed circuit board that plugs into the mainframe board at location J10. The supply provides power for the option 22 or 24 reference oscillators and is included when these options are specified. The supply provides a regulated 28 volts to the options as long as the power cable is connected to the line regardless of the position of the front panel power switch.

4.5.2 The supply consists of a 110/220 volt line select switch (the supply precedes the line voltage select card in the power module; this switch must be set separately to the proper line position), transformer, bridge rectifier, 1250 μF filter capacitor and an adjustable 28 volt integrated regulator.

4.6 HIGH SPEED INTERFACE FUNCTIONAL OPERATION (OPTION 56).

4.6.1 A functional block diagram of the high speed interface is presented in figure 4.35. The major functional circuits of the interface are the Command Register, Function Control Logic, and the Measurement Data Register. In remote (computer controlled) operation, the computer transmits commands to the counter to select the operating mode and measurement parameters. The computer then instructs the counter to make measurements and place the measurement data on the computer interface data bus.

4.7 CONTROL AND STATUS SIGNALS.

4.7.1 The high speed interface and counter are controlled by the computer through signal lines and program instruction commands. The counter and interface respond to the computer through status signal lines and the Parallel format (47-bit) or 16-Bit MUX bus. The sequence of information is controlled by the computer control lines and the counter status lines. The two broad categories of data interchange between the computer and counter are termed READ and WRITE operations.

4.7.2 Each of these operations requires the signal and response routine that is termed the "Handshake" routine. The handshake timing sequence for these modes is illustrated in timing diagrams presented in figures 4.38 and 4.39. The function and description of each of these control and status signals is presented in tables 4.6 and 4.7. As shown in figure 4.35 the control and status signals are

routed to or emanate from the Function Control Logic of the interface and are single-line signals. These signals are used to synchronize the operation of the computer and counter.

4.8 CONTROL SIGNAL DESCRIPTION.

4.8.1 Communication between the counter and computer is controlled by signal lines which carry control and status signals. A description of these signals and their functions is presented in tables 4.6 and 4.7.

4.8.2 The sequence of control and status signals exchanged between the computer and the counter during Program Cycle is illustrated in figure 4.38.

4.8.2.1 *Trigger Status Cycle.* One of the command words transmitted to the counter is the Trigger word. The Trigger word defines the triggering parameters to be used by the counter in performing a measurement. There are instances when the computer will have occasion to interrogate the counter for information regarding the triggering parameters presently in use by the counter. For example, the computer might program the counter to operate in "Auto Trigger" mode. The computer program may be written to issue new programming command instructions to the counter which include known triggering parameters for the signal under measurement. The computer can request transmission of the trigger status word by the counter and then use the information transmitted to generate the new counter program instructions. This transfer of operating parameters is a Write operation in that the data flow is toward the computer but it is related to the Read operation in that it includes information concerning operating parameters of the counter. The transfer operation that transmits such information is termed the Trigger Status Cycle and is illustrated in figure 4.39. The format and content of the Trigger Word is the same regardless of whether it is transmitted by the counter as a status word or transmitted by the computer as a command word.

4.8.2.2 *Measurement Cycle Timing.* The counter is capable of operating in two modes: microprocessor speed and high speed. It is also capable of operating in two I/O data formats: Parallel and 16-Bit MUX format. Selection of one of these is controlled by a DTDP switch on the interface board (S1). For this reason there are four separate sequences of measurement control and status signals. These timing sequences are illustrated in figures 4.40 through 4.43. Measurement transfer times (not including measurement time) are 35 μsec for high speed, 25 msec for μprocessor speed, and 50 msec for μprocessor speed with display.

4.9 COMPUTER PROGRAMMING CONSIDERATIONS.

4.9.1 Use of the Model 9000A Counter in minicomputer applications requires consideration of the various operating modes, speeds, and input/output formats available to the user. The operating modes for the Model 9000A Counter are presented in the Operation section of this Instruction Manual. Information concerning the operating speeds and I/O data format of the Option 56 High Speed Interface is presented in the following paragraphs and illustrations.

4.9.1.1 *Program Cycle.* Control of the counter is accomplished by transmitting program instruction command words to the Command Register of the high speed interface. As shown in figure 4.35, the input to this register is a 16-bit parallel word from the data bus. This programming of the counter may require several such words depending on the operation commanded.

4.9.1.1.1 The issuance of a series of instruction words is the equivalent of the manual entry of instructions through the control keyboard. For example, the computer can issue a single 16-bit command word which will tell the counter: (1) the function selected, e.g. "Measure frequency of signal on input channel A," (2) the timebase or multiplier value and its sign to be used, (3) triggering instructions "channel A–, AC coupling mode, trigger on positive going signal," (4) channel-tie instructions "common" or "separate," and (5) whether to invert the measurement data before presenting it to the computer.

4.9.1.1.2 The transfer of program instruction commands to the counter takes place during a Program Cycle. This operation is consistent regardless of the format or speed in use for measurement. The format of the bits within the command word vary depending on the type of command word given. Details of the word structure are presented in subsequent paragraphs.

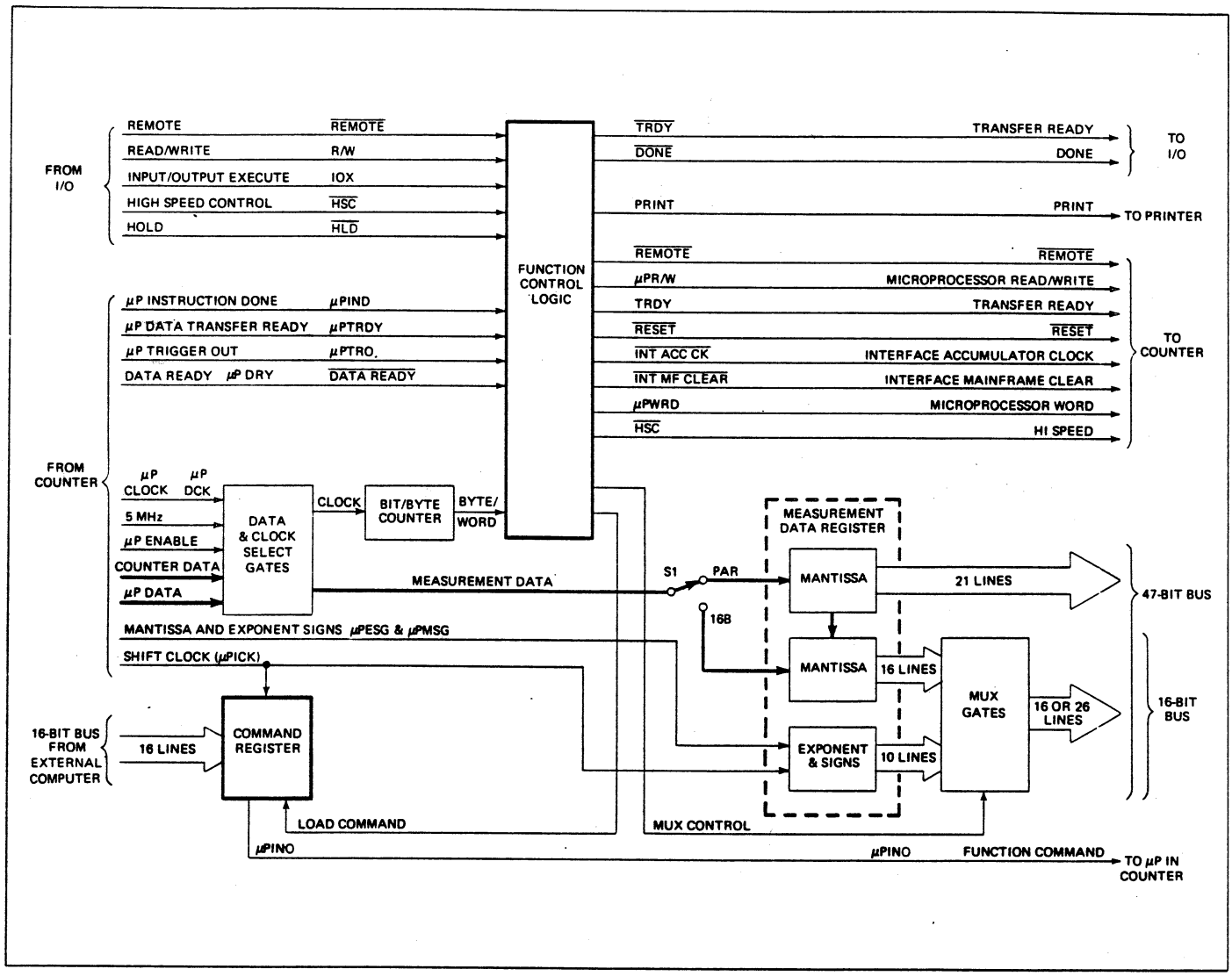
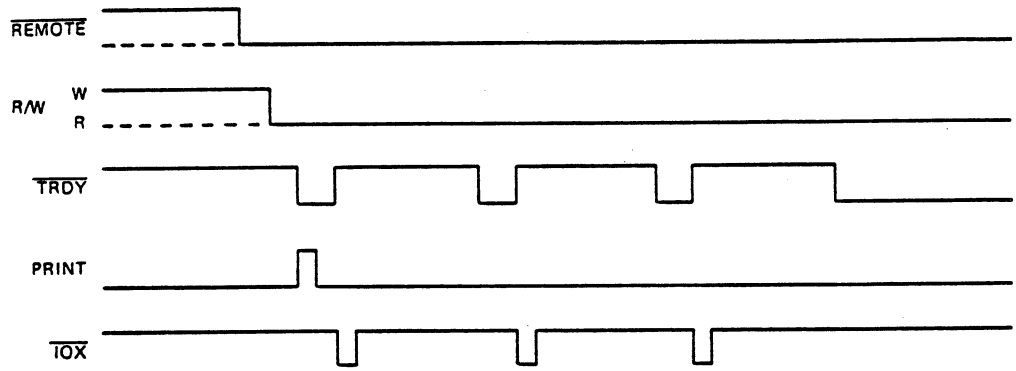
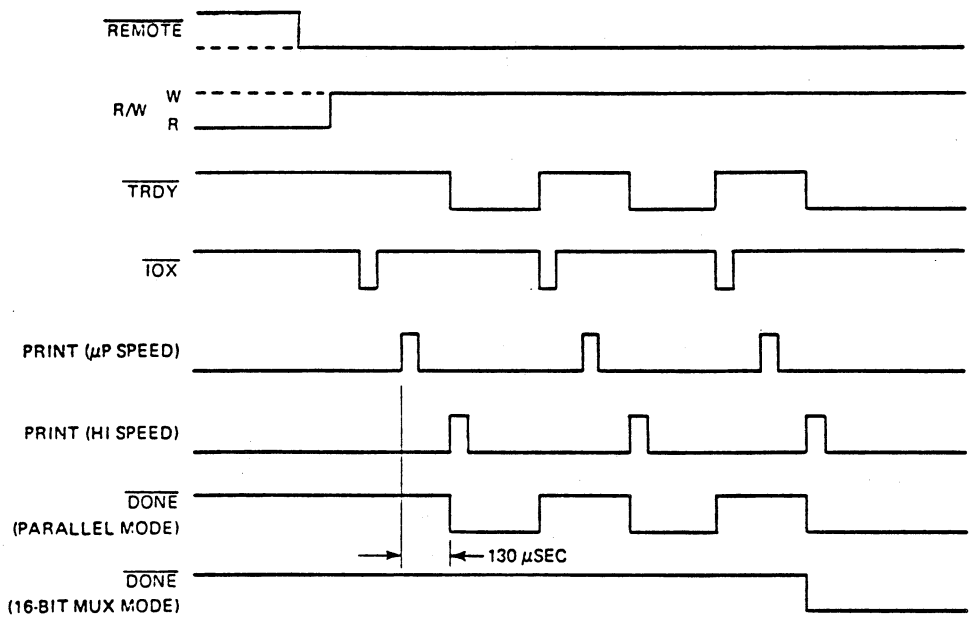


Figure 4.35 - Interface Functional Block Diagram



$\overline{\text{Remote}}$	Line must be down at all times when the computer has control of the counter
R/W	Goes low to indicate to counter that the following operation is programming
$\overline{\text{TRDY}}$	Counter signals "Transfer Ready" to computer
Print	In the read mode print appears coincident with the first $\overline{\text{TRDY}}$ after R/W goes low
$\overline{\text{IOX}}$	Must only be given when $\overline{\text{TRDY}}$ is low. It indicates to counter that a programming word is present at the input lines.

Figure 4.36 - Read Mode Handshake Timing



$\overline{\text{REMOTE}}$	Must be low at all times when the computer has control of the counter
R/W	Low indicates that a measurement is being called for by the computer
$\overline{\text{IOX}}$	Commands the counter to update measurement data
$\overline{\text{TRDY}}$ or PRINT	Indicates data is available at the interface
$\overline{\text{DONE}}$	Indicates that a complete measurement has been made available at the interface.

Figure 4.37 - Write Mode Handshake Timing

Table 4.6 - Control Signal Functions

Mnemonic	Description and Function
$\overline{\text{REMOTE}}$	REMOTE. This signal is set low when the computer is to control the operation of the counter.
R/W	READ/WRITE. Instructs the counter to prepare to make measurements (when set high) or to prepare to receive programming command words (when set low) upon receipt of the INPUT/OUTPUT EXECUTE (IOX) control signal.
IOX	INPUT/OUTPUT EXECUTE R/W Low: negative going IOX signal indicates to the counter that the computer has placed a 16-bit programming command word on the bus and that the counter is to read-in the command. R/W High: instructs the counter to make a new measurement and make the measurement data available on the bus. In Parallel mode, the counter will make the measurement and place the measurement data on the 47-bit data bus. The counter then lowers the $\overline{\text{DONE}}$ status line. In 16-Bit MUX mode, the counter will make the measurement and place the first 16-bit byte of measurement data on the 16-bit data bus. After the computer accepts the first byte the counter places the next byte on the bus. This is repeated until all measurement data has been multiplexed in three bytes to the computer. A new measurement will be automatically initiated when the 4th IOX command is transmitted. The counter then lowers the $\overline{\text{DONE}}$ status line.
$\overline{\text{HSC}}$	HIGH SPEED CONTROL. A low level on this signal line will cause the counter to send unprocessed measurement data at the high speed transfer rate regardless of previous program command instructions, i.e., front panel display or arithmetic manipulation. To use this feature the R/W line must be set to the READ (low) condition before the $\overline{\text{HSC}}$ is changed. The R/W line is then returned to the WRITE (hi) condition and the counter will operate at the high speed. Instructions are not destroyed however, and the counter may be returned to the microprocessor speed (and function) by setting R/W low, returning the $\overline{\text{HSC}}$ to high and then setting the R/W back to high.
$\overline{\text{HLD}}$	HOLD. This signal resets the counter and initiates a new measurement. It must appear only after a TRANSFER READY (TRDY) or PRINT signal has been transmitted.

Table 4.7 - Status Signal Functions

Mnemonic	Description and Function
$\overline{\text{TRDY}}$	TRANSFER READY. Indicates to the computer that the counter is ready to transfer data to or from the computer. This signal has three discrete meanings depending upon the R/W mode and the interface format configuration: READ mode (R/W low, regardless of format) setting the $\overline{\text{TRDY}}$ line low indicates to the computer that the counter is ready to transfer a program instruction into the counter. WRITE mode (R/W high) in Parallel format operation the counter sets the TRDY line low to indicate that a measurement has been taken and the data is available at the 47-bit bus. WRITE mode (R/W high) in 16-bit MUX format operation the counter sets the TRDY line low to indicate that a 16-bit byte of information is available at the 16-bit I/O bus lines.
$\overline{\text{DONE}}$	DONE. A low level signal on this line indicates to the computer that a complete measurement data transfer has been completed. In the Parallel mode the DONE signal occurs simultaneously with the TRDY signal. In the 16-Bit MUX mode the DONE signal occurs after the last 16-bit byte of measurement data has been placed on the I/O lines.
PRINT	PRINT. This signal is a 5 μsec positive-going pulse provided for use with the slower machines such as calculators and printers. It has the same meaning as the TRDY signal but the timing within the high speed interface is such that the PRINT signal should not be used in high speed minicomputer applications. See figure 4.39 and note the difference in timing between TRDY and PRINT. This time difference exists only in the microprocessor speed mode.

SECTION 5 MAINTENANCE

5.1 INTRODUCTION.

5.1.1 This section contains information necessary to check the calibration of the Model 9000A, to perform calibration adjustments, and to troubleshoot the instrument in case of a malfunction.

5.1.2 The calibration check section is used to verify that the instrument is within its rated accuracy specifications. This type of check would be used by the customers receiving inspection to determine acceptance for specification validation purposes as to indicate if calibration is required.

5.1.3 The calibration adjustment section covers the procedures necessary to restore the Model 9000A to its rated accuracies. The procedure consists of voltage adjustments to: the +5.2 volt power supply, the Digital-to-Analog-Converter (D.A.C.), and the signal conditioners hysteresis compensation circuitry; sensitivity; and frequency response and; frequency accuracy adjustments of the reference frequency multipliers and reference oscillator (standard or options).

5.1.4 The troubleshooting section contains information to isolate and identify assemblies or circuits and (or) components that have malfunctioned. This section is divided into Unit Performance tests and Subassembly Performance tests.

5.1.5 The Unit Performance tests are designed to check the instrument by function to isolate the malfunction to a replaceable assembly or assembly circuit. The Subassembly Performance tests are designed to check the operation of an assembly or its circuits and isolate the malfunction to an individual component or circuit.

5.2 FUNCTION AND TIMEBASE CHECKS.

5.2.1 The function and timebase checks use the internal reference frequency to test for the proper display responses. Refer to Table 5.1 for the appropriate settings and responses.

Table 5.1 - Function and Timebase Check

POWER ON - SET KEYBOARD SWITCH TO TEST

Keyboard	Function	Display Units	Gate Time Multiplier	Readout/Remarks	Ch A Status	Ch B Status
No Entry	TI	μ Sec	−8 Sec	.05 * (Home State)	100 DC ↑ 000	100 DC ↓ 000
TL, AU	TI			Ch A Status		
TL, AU	TI			Ch B Status		
7	TI	μ Sec	−7 Sec	.1 (or see below)		
	TI	Sec	−7 Sec	.		
6	TI	Sec	−6 Sec	.		
5	TI	Sec	−5 Sec	.		
4	TI	Sec	−4 Sec	.		
3	TI	Sec	−3 Sec	.		
2	TI	Sec	−2 Sec	.		
1	TI	Sec	−1 Sec	.		
0	TI	Sec	0 Sec	.		
1	TI	Sec	1 Sec	.		
AV	TIA	n Sec	1	50.* (Home State)		
0	TIA	μ Sec	0	.05		
2	TIA	n Sec	2	50.0		
3	TIA	n Sec	3	50.00		
4	TIA	n Sec	4	50.000		
5	TIA	n Sec	5	50.0000		
6	TIA	n Sec	6	50.00000		
7	TIA	n Sec	7	50.000000		
8	TIA	n Sec	8	50.0000000		
9	TIA	Sec	9	O/F . ⊾ (100 Sec Gate)		
P	P	μ Sec	−8 Sec	.10 (Home State)		
7	P	μ Sec	−7 Sec	.1		
6	P	Sec	−6 Sec	.		
5	P	Sec	−5 Sec	.		
4	P	Sec	−4 Sec	.		
3	P	Sec	−3 Sec	.		
2	P	Sec	−2 Sec	.		
1	P	Sec	−1 Sec	.		
0	P	Sec	0 Sec	.		
1	P	Sec	1 Sec	.		
AV	PA	n Sec	1	100. (Home State)		
0	PA	μ Sec	0	.10		
2	PA	n Sec	2	100.0		
3	PA	n Sec	3	100.00		
4	PA	n Sec	4	100.000		
5	PA	n Sec	5	100.0000		
6	PA	n Sec	6	100.00000		
7	PA	n Sec	7	100.000000		
8	PA	Sec	8	O/F . ⊾ (10 Sec Gate)		
9	PA	Sec	9	O/F . ⊾ (100 Sec Gate)		

*Note: In test, TI or TIA, the counter is measuring the internal oscillator's signal. This signal's duty cycle is 50% ± 10%, therefore the readings may vary (i.e., in TI .04 or .06 μSec readings are normal, in TIA 40 or 60 nSec readings are normal).

Table 5.1 - Function and Timebase Check (continued)

Keyboard	Function	Display Units	Gate Time Multiplier	Readout/Remarks	Ch A Status	Ch B Status
FA	FA	MHz	−1 Sec	10.00000 (Home State)		
0	FA	MHz	0 Sec	10.000000		
1	FA	MHz	1 Sec	10.0000000		
CS, 2	FA	MHz	−2 Sec	10.0000		
3	FA	MHz	−3 Sec	10.000		
4	FA	MHz	−4 Sec	10.00		
5	FA	MHz	−5 Sec	10.0		
6	FA	MHz	−6 Sec	10.		
FC	FC	Hz	−1 Sec	. (Home State)		
0	FC	Hz	0 Sec	.		
1	FC	Hz	1 Sec	.		
CS, 2	FC	Hz	−2 Sec	. No Input Sig.		
3	FC	Hz	−3 Sec	.		
4	FC	Hz	−4 Sec	.		
5	FC	Hz	−5 Sec	.		
6	FC	Hz	−6 Sec	.		
RA	A/B		1	1.0 (Home State)		
0	A/B		0	1.		
2	A/B		2	1.00		
3	A/B		3	1.000		
4	A/B		4	1.0000		
5	A/B		5	1.00000		
6	A/B		6	1.000000		
7	A/B		7	1.0000000		
8	A/B		8	1.00000000		
9	A/B		9	O/F . ⊾ (100 Sec Gate)		
TO	TO	m	1	. (Home State)		
SS	TO	M	1	. Display counts, . overflows @ 100 Sec., continues counting		
0	TO		0	.		
SS	TO	M	0	. Display counts, overflows @ 100 Sec., continues counting		
2, SS	TO	M	2	.		
3, SS	TO	M	3	.		
4, SS	TO	M	4	.		
5, SS	TO	M	5	.		
6, SS	TO	M	6	.		
7, SS	TO	M	7	.		
8, SS	TO	M	8	.		
9, SS	TO	M	9	.		
SS	TO	M	9	. Display count stops		
Test SW to Common	TO		9	. (Common Lite)		

5.3 CALIBRATION ADJUSTMENT.

5.3.1 *INTRODUCTION AND DESCRIPTION.* This procedure covers the calibration of the Dana Microprocessing Timer/Counter. The procedure consists of: voltage adjustments of the Digital-to-Analog Converters (DACs), the +5.2 volt power line, and the hysteresis compensation circuitry; sensitivity adjustments of the signal conditioning circuits; frequency response adjustments of the attenuators and; frequency accuracy adjustments of the reference frequency multipliers and reference oscillator.

5.3.2 The location of the reference oscillator adjustment depends on whether the instrument is equipped with the standard or one of the two available options.

5.4 REQUIRED EQUIPMENT.

5.4.1 A list of equipment required to perform the procedure is provided in table 5.2.

5.5 DISASSEMBLY, CALIBRATION.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC Power source.

5.5.1 Access to the calibration points is obtained by removal of the instrument bottom cover. The cover is held in place by the four captive screws located in each corner. After loosening these screws, the cover can be lifted by pressing up on the cover through access holes at the bottom of the rear panel.

5.6 PRELIMINARY OPERATION.

5.6.1 The following steps must be performed before the calibration procedure is started.

a. Check line voltage.

b. Verify that proper voltage and fuse rating have been chosen for the instrument. If the instrument

Table 5.2 - Required Equipment

NOTE

Minimum use specifications are the principal parameters required for performance of the calibration, and are included to assist in the selection of alternate equipment. Satisfactory performance of alternate items shall be verified prior to use. All applicable equipment must bear evidence of current calibration.

Item	Minimum Use Specification	Calibration Equipment
1. Frequency Standard	1 MHz, 5 MHz or 10 MHz ($3X10^{-10}$ accuracy)	
2. Oscilloscope	100 MHz Bandwidth	TEK 454
3. Voltmeter	4-digit resolution, 10 MΩ or greater input resistance, ± .05% accuracy	Racal-Dana 4002
4. Signal Generator	100 Hz – 100 MHz 1V adjustable	HP651B Racal-Dana 9081
5. Signal Generator	100 MHz – 512 MHz (9035A only)	Racal-Dana 9081
6. Square Wave Generator	50V P.P. @ 10 kHz	TEK 105
7. Alignment Tool	Blade (non-metallic)	General Cement 9300
8. BNC T-Connector		
9. RF Millivoltmeter	10 KHz – 1.5 GHz	Racal-Dana 9301A
10. Pulse Generator	8 ns pulse width	Datapulse 112 or 110B

is equipped with an optional reference oscillator, check the option power supply line selector.

c. Connect the power cord to the line. Set the power switch (PWR) to ON and provide 1/2 hour for temperature stabilization.

d. Refer to the operating manuals provided with the calibration equipment to be used and provide appropriate warmup time as required.

e. Review the calibration procedure and verify that all necessary equipment and hardware are assembled. Preset controls as given below.

NORM/HOLD	NORM	
SEP/TEST/COM	SEP	
"FUNCTION"	F_A	
TRIGGER STATUS	CH A	CH B
SLOPE	↑	↓
AC/DC	DC	DC
TL	000	000

5.7 CALIBRATION POINTS.

5.7.1 The calibration points are located on the main PC board, signal conditioning modules, and reference. The locations are shown in figure 5.6.

5.8 PROCEDURE.

5.8.1 The calibration procedure is designed to keep the instrument operating within the published specifications for indefinite periods of time. The order of adjustment has been determined to produce the least interaction between adjustments. For best results, the procedure should be followed as presented.

5.8.2 Power Supply (Main Logic Board).

a. Reference voltmeter to GND pin (see figure 5.6).

b. Monitor +5.2 volt line and adjust R61 for a voltmeter reading of +5.2 volts ± .05 volts.

5.8.3 DAC.

a. Program +3V trigger level for channel A. With a voltmeter, monitor CH A T/L output on rear panel.

b. Adjust + full scale potentiometer R3 for a voltmeter reading of +3.000 volts ± .003 volts.

c. Program –3V trigger level for channel A.

d. Adjust – full scale potentiometer R15 for a voltmeter reading of –3.000 volts ± .003 volts.

e. Program +3V trigger level for channel B. With a voltmeter, monitor CH B T/L output on rear panel.

f. Adjust + full scale potentiometer R4 for a voltmeter reading of +3.000 volts ± .003 volts.

g. Program –3V trigger level for channel B.

h. Adjust – full scale potentiometer R16 for a voltmeter reading of –3.000 volts ± .003 volts.

i. Perform the checks listed in Table 5.3.

5.8.4 Reference Board (Assembly No. 406768)

CAUTION

If your Reference Assy. PCB is numbered 406179, not 406768, the following two-step procedure does **not** apply. Using the procedure will probably damage the assembly board. **Rather**, use the procedure for Reference Assy. PCB 406179 which is provided in the Addendum (alternate paragraph 5.8.4) at the front of this manual.

a. With an oscilloscope referenced to TP1, monitor TP2 and adjust C23 for an oscilloscope display as shown in figure 5.1.

b. Monitor TP3 and adjust C30 for an oscilloscope display of maximum amplitude at 100 MHz, as shown in figure 5.2.

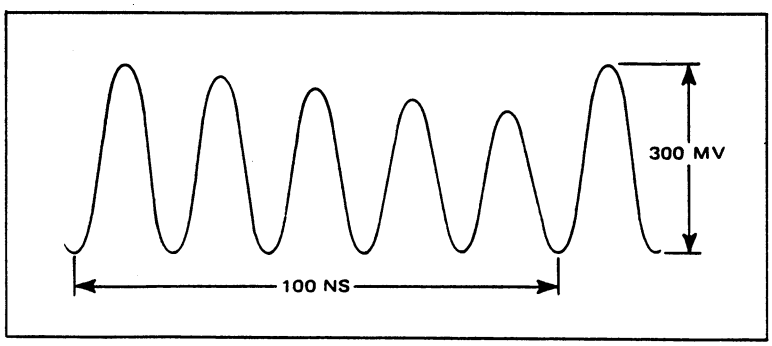


Figure 5.1 - 5th Harmonic Output

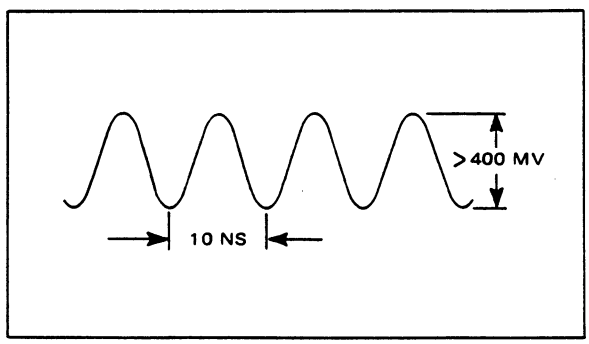


Figure 5.2 - 100 MHz Signal

Table 5.3 - Trigger Level Cal Check

Keyboard	Function	Display Units	Gate Time Multiplier	DMM Reading	Ch A Status	Ch B Status
TI	TI	Sec	–8 Sec		1 AC↑ 0.00	1 AC↓ 0.00
Connect a DMM to J216 (Ch. A trigger level) referenced to J215 (trigger level common) on the 9000 rear panel.						
CH A:TL, 3,.,1,9,TL	TI	Sec	–8 Sec	+3.19 ±0.0125	1 AC↑ 3.19	
CH A:TL, 2,.,0,0,TL	TI	Sec	–8 Sec	+2.00 ±0.0125	1 AC↑ 2.00	
CH A:TL, 1,.,0,0,TL	TI	Sec	–8 Sec	+1.00 ±0.0125	1 AC↑ 1.00	
CH A:TL, 0,.,0,0,TL	TI	Sec	–8 Sec	±0.00 ±0.0125	1 AC↑ 0.00	
CH A:TL,CS, 1,.,0,0,TL	TI	Sec	–8 Sec	–1.00 ±0.0125	1 AC↑–1.00	
CH A:TL,CS, 2,.,0,0,TL	TI	Sec	–8 Sec	–2.00 ±0.0125	1 AC↑–2.00	
CH A:TL, CS,3,.,2,0,TL	TI	Sec	–8 Sec	–3.20 ±0.0125	1 AC↑–3.20	
Connect the DMM to J214 (Ch B trigger level) referenced to J215 (trigger level common) on the 9000 rear panel.						
CH B:TL, 3,.,1,9,TL	TI	Sec	–8 Sec	+3.19 ±0.0125		1 AC↓ 3.19
CH B:TL, 2,.,0,0,TL	TI	Sec	–8 Sec	+2.00 ±0.0125		1 AC↓ 2.00
CH B:TL, 1,.,0,0,TL				+1.00 ±0.0125		1 AC↓ 1.00
CH B:TL, 0,1,0,0,TL				±0.00 ±0.0125		1 AC↓ 0.00
CH B:TL,CS, 1,.,0,0,TL				–1.00 ±0.0125		1 AC↓–1.00
CH B:TL,CS, 2,.,0,0,TL				–2.00 ±0.0125		1 AC↓–2.00
CH B:TL,CS, 3,.,2,0,TL				–3.20 ±0.0125		1 AC↓–3.20
CH A:TL,AU					1 AC↑ 0*	
CH B:TL,AU						1 AC↓ 0*
Remove DMM from J214 (Ch. B trigger level) and J215 (trigger level common). Connect the Reference In (J203) to a 1, 5, or 10 MHz House Reference or Synthesizer Output with an output of 1 volt RMS. The "EXT REF" annunciator in the "STATUS" window of the front panel must light, if the external frequency is within ± 10 ppm of the 1, 5, or 10 MHz.						

*Attenuation is not specified.

Table 5.4 - Sensitivity Cal Check

Keyboard	Function	Display Units	Gate Time Multiplier	Readout/Remarks	Ch A Status	Ch B Status
RA, 5	A/B		5	.	1 DC ↑ 0.01	1 DC ↓ 0.01
CH A:AC	A/B		5	.	1 AC ↑ 0.01	1 DC ↓ 0.01
CH B:AC	A/B		5	.	1 AC ↑ 0.01	1 AC ↓ 0.01
CH A:TL 0,.,0,0,TL	A/B		5	.	1 AC ↑ 0.00	1 AC ↓ 0.01
CH B:TL,0, .,0,0,TL	A/B		5	.	1 AC ↑ 0.00	1 AC ↓ 0.00
	Connect Ch. A to a 50Ω termination to a frequency source. Increase the output of the frequency source until a ratio of 1. appears on the display. The input sensitivity is: 0 to 1 MHz ≤ 25 mV RMS 1 MHz to 50 MHz ≤ 50 mV RMS 50 MHz to 100 MHz ≤ 100 mV RMS NOTE: This checks the sensitivity of Ch. A and Ch. B signal conditioners.					
	A/B		5	1.00000	1 AC ↑ 0.00	1 AC ↓ 0.00
	Remove input cable to Ch. A.					
FC	FC	Hz	−1 Sec	.	1 AC ↑ 0.00	1 AC ↓ 0.00
	Connect the Ch. C input to a signal source and increase the output until the "In Range" annunciator lites on the front panel. The Ch. C sensitivity from 100 MHz to 512 MHz ≤ 15 mV RMS.					
	FC	MHz	−1 Sec	239.9999	1 AC ↑ 0.00	1 AC ↓ 0.00
	Remove the Ch. C input cable. Example above is 240 MHz.					

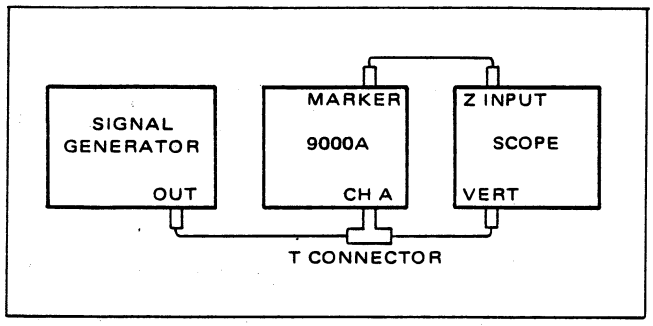


Figure 5.3 - Marker Hookup

5.8.5 Signal Conditioning Circuit, Channel A and B.

5.8.5.1 *Sensitivity.*

a. Set TL to 0.00 (1V range) for both channel A and B. Select F_A, + Slope, DC Coupled, Separate Mode, Timebase 10^{-1} Sec.

b. Apply a 1V RMS, 100 Hz signal to the channel A input connector and verify a reading of 100 Hz.

c. Reduce input voltage until no gating occurs.

d. Toggle the channel A slope switch between + and – and adjust potentiometer R58 on channel A signal conditioner for a display in both + and – slope with the least amount of input signal.

e. Select A/B, multiplier +1, and common mode. Set input to 1V RMS and verify a counter display of 1.0.

f. Reduce input voltage until no gating occurs.

g. Toggle the channel B slope switch between + and – and adjust potentiometer R58 on channel B signal conditioner for a display in both + and – slope with the least amount of input signal.

h. Perform the checks listed in Table 5.4.

5.8.5.2 *Hysteresis Compensation.*

a. Select TI, common mode. Channel A: + Slope, DC Coupling, Trigger Level + 0.00V; Channel B: – Slope, DC Couple, Trigger Level – .05V. Set vertical gain of oscilloscope to 20 mV/division and sweep to center of reticle.

b. Apply a 100 Hz @ .3V P.P. signal to the channel A input and the oscilloscope vertical input; connect the marker output on the back of the counter to the oscilloscope Z axis (see figure 5.3).

c. Toggle the channel A slope switch between + and – and adjust potentiometer R48 on the channel A signal conditioner for the same trigger levels at both positions of the slope switch.

d. Adjust R58 on the channel A signal conditioner for a trigger point of zero volts.

e. Set channel A for a trigger level of 0.05V. Set channel B for a trigger level of 0.00.

f. Toggle the channel B slope switch between + and – and adjust potentiometer R48 on the channel B signal conditioner for the same trigger levels at both positions of the slope switch.

g. Adjust R58 on the channel B signal conditioner for a trigger point of zero volts.

h. Select A/B, multiplier +6. Set the trigger level on channel A and channel B for 0.00V.

i. Apply a 100 mV RMS, 100 MHz signal to the channel A input connector and verify a counter display of 1.000000.

5.8.5.3 *Attenuator.*

a. Select channel A 10 volt range and apply a 10 kHz 20V P.P. square wave signal to channel A input.

b. With the oscilloscope, monitor pin 8 of U3 and adjust C6 (both on the channel A signal conditioner) for a waveform flatness within ±40 mV. Refer to waveform shown in figure 5.4.

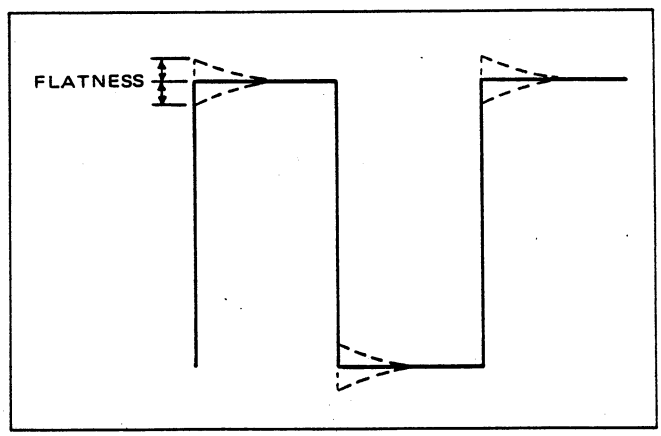


Figure 5.4 - Square Wave Signal

c. Select channel A 100 volt range and increase the amplitude of the 10 kHz to 50V P.P.

d. Adjust C3 on channel A signal conditioner for a waveform flatness to within ±10 mV.

e. Repeat steps b, c, and d for channel B.

Table 5.5 - Internal Reference Oscillators

Oscillator	Aging Rate	Temperature Stability	Stability
Standard	$<3x10^{-7}$/mo.	$<5x10^{-6}/^{o}C$ $0^{o}C$ to $+50^{o}C$	$<1x10^{-7}$ with 10% line V variation
Option 22A	$<3x10^{-9}$/day*	$<3x10^{-9}/^{o}C$ $0^{o}C$ to $+50^{o}C$	$<2x10^{-8}$ with 10% line V variation
Option 24A	$<5x10^{-10}$/day*	$<6x10^{-10}/^{o}C$ $0^{o}C$ to $+50^{o}C$	$<1.5x10^{-9}$ with 10% line V variation

*After 3 months of continuous operation.

5.8.6 Prescaler (Model 9035A only).

a. Set potentiometer R31 to the center of its mechanical span and R19 fully clockwise. Note that the IN-RANGE indicator on the front panel is lit.

b. Adjust R19 counterclockwise until IN-RANGE indicator goes out and continue counterclockwise for ≈ 1/20 of a revolution.

c. Apply a 100 MHz signal at 15 millivolts RMS to the channel C input and verify the IN-RANGE indicator lights. Repeat at 50 MHz intervals to 500 MHz.

d. If counter readings appear noisy (not caused by the frequency source), adjust potentiometer R31 clockwise until noise abates and repeat step c.

5.8.7 Internal Reference.

5.8.7.1 There are three internal reference oscillators available for the Series 9000A. (See Table 1.2.)

5.8.7.2 The calibration adjustment for the standard oscillator is a single variable capacitor adjustment, accessible at the rear panel (OSC ADJ). The options have two adjustments (COARSE and FINE), accessible at the rear panel.

5.8.7.3 *Reference Oscillator Frequency Check.*

a. Select the following control settings:

FUNCTION	F_A
TIMEBASE	10
CHANNEL A SLOPE	↑
COUPLING	DC
TL	0.00
SEP/TEST/COM	COM

FAKEY
0 gives 6 digits
SLOPE SWITCH
DC SWITCH
TRIGGER LEVEL

b. Connect the 1 MHz frequency standard to the channel A input.

c. The difference between the internal reference oscillator and the 1 MHz frequency standard can be determined by the following equation:

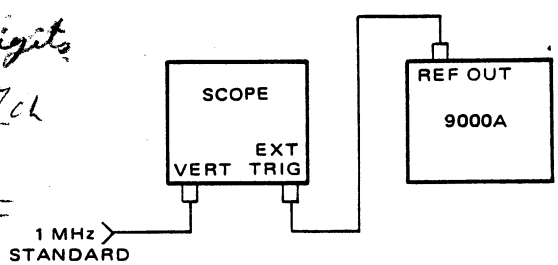
Internal Oscillator Frequency = (2E6-display) x 10

d. Some examples of various counter readings and the frequency difference that is indicated are shown below:

Counter Display	Internal Reference Osc.
9.9999950 E3	10,000.050 kHz
10.0000000 E6	10,000.000 kHz
10.0000025 E6	9,999.975 kHz

5.8.7.4 *Adjustment Procedure.*

a. Connect the 1 MHz 1V RMS frequency standard to the vertical input of the oscilloscope, and connect the REF OUT signal from the back panel of the counter to the external trigger of the oscilloscope (see wiring diagram below).



b. Set scope controls as follows:

TRIGGER	
SLOPE:	+
COUPLING:	AC
SOURCE:	EXT
SWEEP MODE	
NORM TRIGGER	
SWEEP:	.05 μS
CHANNEL INPUT:	AC
volts/div	Depends on amplitude of frequency standard
TRIGGER LEVEL:	center of mechanical span

c. Adjust trigger level for an oscilloscope display of the frequency standard output.

d. If the instrument is equipped with the standard reference oscillator, adjust OSC ADJ for a oscilloscope display that is as stationary as possible (does not drift to the left or right).

e. If the instrument is equipped with option 22 or 24 high stability reference oscillator, remove the two protective metal caps from the COARSE and FINE adjustment access holes in the back panel. Using the two exposed controls, perform the procedure outlined in step e.

f. To determine the drift rate of the calibrated instrument, measure the time it takes the oscilloscope pattern to drift 5 divisions on the oscilloscope. The oscillator drift can be determined from figure 5.5.

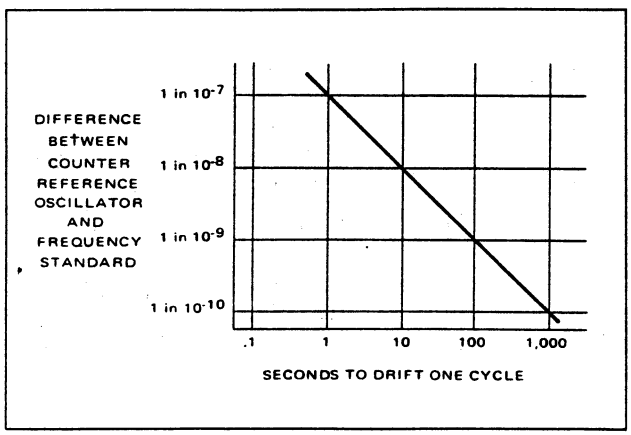


Figure 5.5 - Oscillator Drift

5.8.8 External Reference Circuit Check.

5.8.8.1 Supply a 1 Megahertz reference signal at 1.5 volts RMS to the rear panel EXT REF connector and verify that the EXT REF light on the front panel is lit. Reduce the input level to 1 volt RMS and verify that the front panel EXT REF light is still on.

5.8.8.2 Supply inputs of 5 and 10 MHz at 1V RMS and repeat the same procedure.

5.9 MAINTENANCE DISASSEMBLY.

5.9.1 Always disconnect the power cord from the instrument when disassembling beyond the calibration stage or when boards are to be removed. Power may be restored to the instrument with boards removed for troubleshooting purposes without damage to the instrument. Also remove power before inserting boards.

5.9.1.1 *Tools Required.* Besides a phillips screwdriver the following tools may be required depending on what is to be disassembled.

	Name	Suggested Type
1.	Long nose pliers	–
2.	Soldering iron	35 watt
3.	Solder	Rosin Core
4.	Solder remover	Solda Pult

5.9.2 Replacing Front Panel LEDs.

a. Lay the 9000A on its side. Loosen the four captive corner screws on the bottom cover and remove cover. Repeat the process on the top cover.

b. Disconnect cables to the signal connector boards and prescaler (9035A only).

c. Remove the four button head phillips screws holding the front panel to the bottom frame.

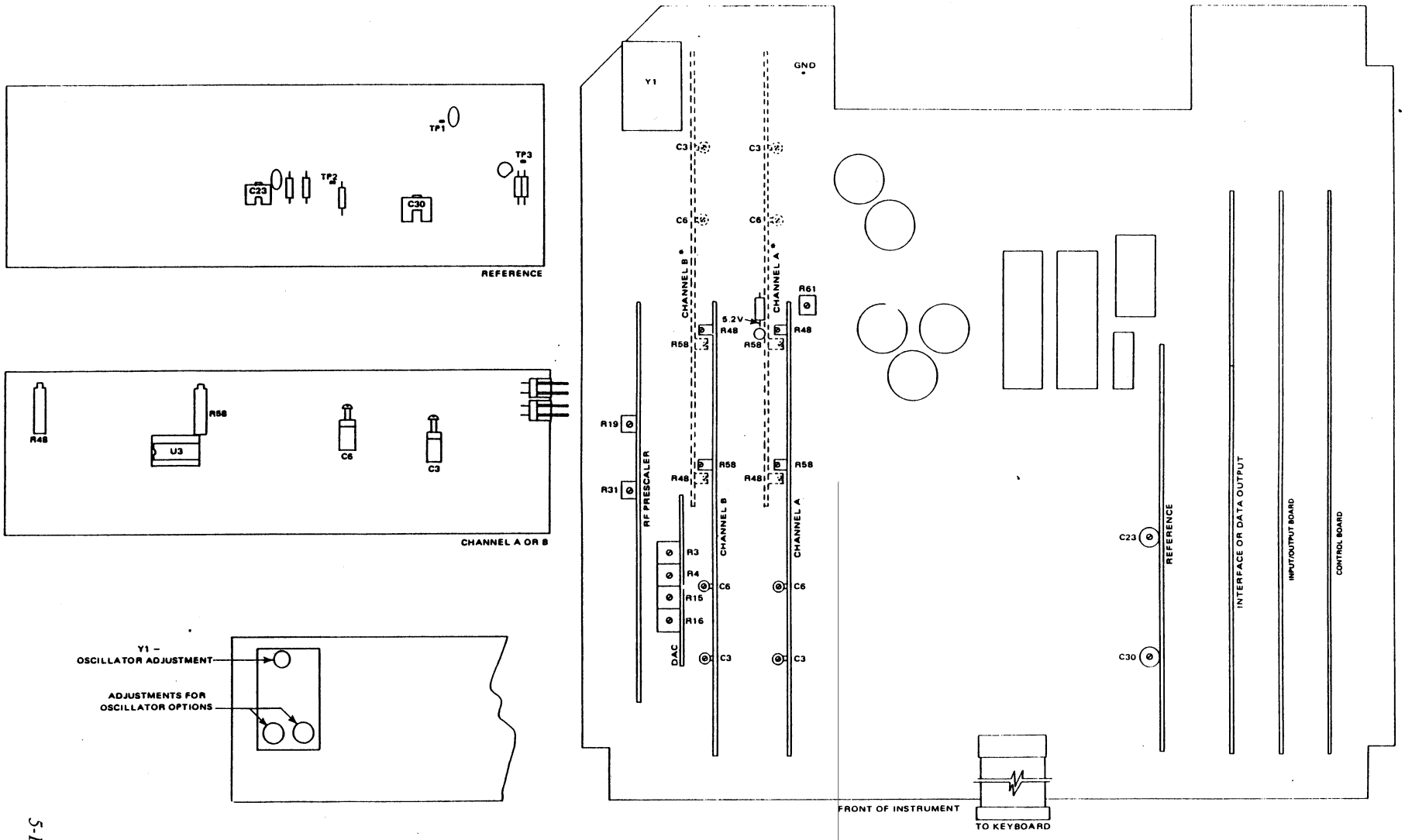


Figure 5.6 - Calibration Points

d. Remove the four button head phillips screws holding the front panel to the top frame.

e. Pull keyboard out as far as track will allow.

f. Press front panel display board assembly out from case.

g. Remove 5 phillips screws mounting display board to front panel and separate. Seven segment LEDs are socket mounted and can be unplugged. LED lamps are unsoldered for removal.

5.10 UNIT PERFORMANCE TESTS.

5.10.1 The unit performance tests are established by function, which follows an input signal or signals from the input terminals through to the input of the main logic PCB. The selected function determines what route must be established by the signal conditioners (FA and (or) FB), prescaler (FC), and internal reference (100 MHz) to perform the desired measurement.

5.10.2 The Model 9000A operation is dependent upon the microprocessor and its keyboard inputs to format measurement routines for proper operation.

5.10.3 When a failure occurs in a counter that is configured for remote operation in a system, the first consideration must be to determine if the malfunction is due to the circuits of the Model 9000A or the system interface (hard/software).

5.10.4 The problem for the repair and/or calibration facility is to qualify proper operation; which, if tested on the bench, cannot fully verify system interface unless a controller is available to exercise interface commands and responses.

5.10.5 The first series of tests will be preliminary checks to insure that entries to the keyboard address the computer and main logic PCB to provide predictable responses, visually, on the front panel and at key test points in the Model 9000A. This will assure that the keyboard and display assemblies are basically performing.

NOTE

The keyboard for pulse parameter (Option 11) is limited by the number of replacement components to the (6) slide switches, (5) diodes, and the MCS-4 IC, U1. If any of the keyboard switches fail, such as a short; the assembly must be replaced with a factory unit.

NOTE

When reference designators are called out as test points for plug-in assemblies and access to these are limited physically; the instrument must be turned off, assembly removed, replaced on an extender, and powered-up again. The extender board kit, P/N 406-857, contains 5 boards used to extend the following: 406851 - Prescaler and Signal Conditioner (J1 & J3/J4), 406852 - DAC & Oscillator Option Power Regulator (J2 & J10), 406853 - Reference (J5) 406854 - Interface Options (J6).

Table 5.6 - Preliminary Unit Performance Test

Remove bottom cover and PC board retainer.	
Keyboard slide switches	
Normal/Hold	Normal
Sep/Test/Com	Test
Ch A: Slope	↑
Coupling	DC
Ch B: Slope	↓
Coupling	DC
Power Switch	On

Table 5.7 - Keyboard Entry/Display Response Preliminary Unit Performance Test

Keyboard	Function	Display Units	Gate Time Multiplier	Display/Remarks	Ch A Status	Ch B Status	
	TI	μ Sec	−8 Sec	.05 *	100 DC ↑ 000	100 DC ↓ 000	Gate Test
AV	TIA	n Sec	1	50. *	100 DC ↑ 000	100 DC ↓ 000	
CK(HOLD)	TIA	n Sec	8	888.88888888	100 DC ↑ 888	100 DC ↓ 888	
9	TIA	p Sec	9	. O/F after 100 Sec	100 DC ↑ 000	100 DC ↓ 000	
8	TIA	n Sec	8	50.0000000			
7	TIA	n Sec	7	50.000000			
6	TIA	n Sec	6	50.00000			
5	TIA	n Sec	5	50.0000			
4	TIA	n Sec	4	50.000			
3	TIA	n Sec	3	50.00			
2	TIA	n Sec	2	50.0			
1	TIA	n Sec	1	50.			
0	TIA	μ Sec	0	.05			
P	P	μ Sec	−8 Sec	.10			
1/X	P	MHz	−8 Sec	10.			
AV	PA	n Sec	1	100.			
FA	FA	MHz	−1 Sec	10.00000			
FC	FC	Hz	−1 Sec	.			
RA	A/B	Blank	1	1.0			
TO	TO	m	1	.			
SS	TO	M	1	Starts counting, O/F @ 100 Sec., continues counting			
SS	TO	M	1	Stops count.			
RS	TO		1	Clears display count.			
TL,0,1,2	TO		1	Ch A .	100 012		
3,4,5	TO		1	Ch A .	100 345		
6,7,8	TO		1	Ch A .	100 678		
9,0,1	TO		1	Ch A .	100 901		
2,.,3,4	TO		1	Ch A .	1 2.34		
5,.,6,7	TO		1	Ch A .	1 5.67		
8,9,.,0	TO		1	Ch A .	10 89.0		
1,2,.,3,CS	TO		1	Ch A .	10 −12.3		
4,5,.,6	TO		1	Ch A .	10 −45.6		
7,8,.,9	TO		1	Ch A .	10 −78.9		
Repeat from TL, 0, 1, 2 for Channel B							
↓,AC	TO		1	Ch A .	↓ AC		
↑,AC	TO		1	Ch B .		↑ AC	
COM	TO		1	.			COM
TI	TI	Sec	−8 Sec	.			
Connect Channel A to 1V @ 1 KHz (Scope Cal Out)							
⎍ Opt. 11 or 12	TI	μ Sec	−8 Sec	50X.XX (50%-Ch A & Ch B)	1 DC ↑ 0.50	1 DC ↓ 0.50	
Ch A & Ch B slope, coupling, sep/test/com switches are disabled.							

*Note: In test, TI or TIA, the counter is measuring the internal oscillator's signal. This signal's duty cycle is 50% ± 10%, therefore the readings may vary (i.e., in TI .04 or .06 μSec readings are normal, in TIA 40 or 60 nSec readings are normal).

Table 5.7 - Keyboard Entry/Display Response Preliminary Unit Performance Test (continued)

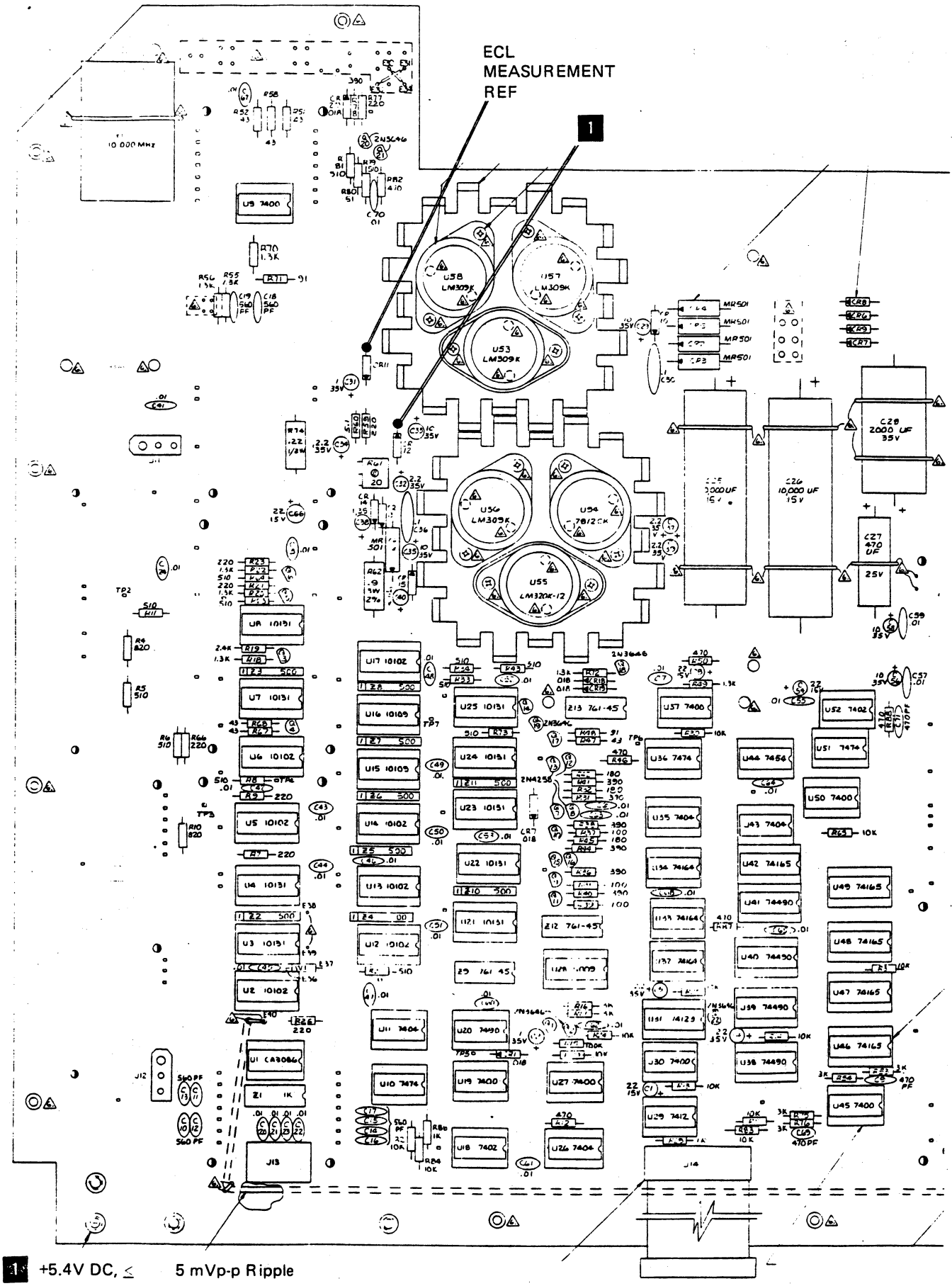
Keyboard	Function	Display Units	Gate Time Multiplier	Display/Remarks	Ch A Status	Ch B Status
⌐	TI	μ Sec	−8 Sec	.3X(10%-A, 90%-B)	1 DC ↑ 0.10	1 DC ↑ 0.90
¬	TI	μ Sec	−8 Sec	1.4X(90%-A, 10%-B)	1 DC ↓ 0.90	1 DC ↓ 0.10
FA	FA	KHz	−1 Sec	1.00	1 AC ↓ 0.90	1 AC ↑ 0.10
TL,AU	FA	KHz	−1 Sec	1.00	1 AC ↓ 0.00	1 AC ↑ 0.10
HOLD	FA	KHz	−1 Sec	1.00	1 AC ↓ 0.00	1 AC ↑ 0.10
RS	Takes a new read when depressed (gate flashes one time).					
RM	RM = Return to manual for option 55, Remote for option 56.					
Remove Ch. A input cable.						

Table 5.8 - Preliminary Main Logic, Reference and DAC Unit Performance Tests

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
NOTE: Main Logic PCB ECL Voltage Measurement Referenced to CR11 (Anode)					
	ECL Supply Voltage	CR12 (Cathode) Main Logic PCB	1	Fig 5.7	+5.4 VDC ≤ 50 mV p-p Ripple
No ECL voltage, go to main logic power supply subassembly performance test.					
Extend the Reference PCB with Pin 406853, Extender PCB					
Keyboard: IT, (Ch A) TL, AU, (Ch B) TL, AU					Note: Reference PCB Measurements are Referenced to TP1
	10 MHz (TCRO)	U2-12	A	Fig 5.8	Waveform #1
	10 MHz Drive	U2-3	B	Fig 5.8	Waveform #2
	10 MHz Output	U2-8	C	Fig 5.8	Waveform #3
	50 MHz Drive	TP2	D	Fig 5.8	Waveform #4
	100 MHz Clock Out	TP3	E	Fig 5.8	Waveform #5
Connect the Ext. Ref. in (J203) to a 1, 5, or 10 MHz (± 10 ppm) @ 1V RMS sinewave on the rear panel					Front panel Ext. Ref. LED annunciates
	Ext. Ref. Input C1, 5, or 10 MHz	U1-1	F	Fig 5.8	1, 5, or 10 MHz Waveform #6
	1, 5, or 10 MHz Ext. Ref. (TTL)	U1-8	G	Fig 5.8	1, 5, or 10 MHz Waveform #7
	Signal Detector/Gate Out (10 MHz)	U2-1	H	Fig 5.8	Waveform #8
	100 MHz Clock Out	TP3	E	Fig 5.8	Waveform #5
Remove Ext. Ref. In Signal					Front panel LED goes out
Reference PCB waveforms unavailable, see reference subassembly performance test.					
Extend the DAC PCB with P/N 406852 Extender PCB					Note: DAC measurements are referenced to J2-5
	DAC Supply Voltage	U1-9	1	Fig 5.9	+5.2 VDC ± 0.1 VDC
	DAC Output/Summing Mode	U4-4	2	Fig 5.9	0 VDC ± 15 mV
Keyboard: (Ch A) TL, 0, ., 5, 0, TL					Front Panel: Ch A status indicates 0.50
	DAC Output Voltage	W-1	3	Fig 5.9	+0.50 VDC ± 0.0125 VDC
Keyboard: (Ch A) TL, 0, ., 5, 0, CS, TL					Front Panel: Ch A status indicates −0.50

Table 5.8 - Preliminary Main Logic, Reference and DAC Unit Performance Tests (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	DAC Output Voltage	W-1	3	Fig 5.9	–0.50 VDC ±0.0125 VDC
Keyboard: (Ch B) TL, 0, ., S, 0, TL					Front Panel: Ch B status indicates 0.50
	DAC Output Voltage	W-2	4	Fig 5.9	+0.50 VDC ±0.0125 VDC
Keyboard: (Ch B) TL, 0, ., 5, 0, CS, TL					Front Panel: Ch B status indicates –0.50
	DAC Output Voltage	W-2	4	Fig 5.9	–0.50 VDC ±0.0125 VDC
DAC PCB voltages unavailable, see DAC subassembly performance test.					



1 +5.4V DC, ≤ 5 mVp-p Ripple

Figure 5.7 - Main Logic Preliminary Unit Performance Test Points

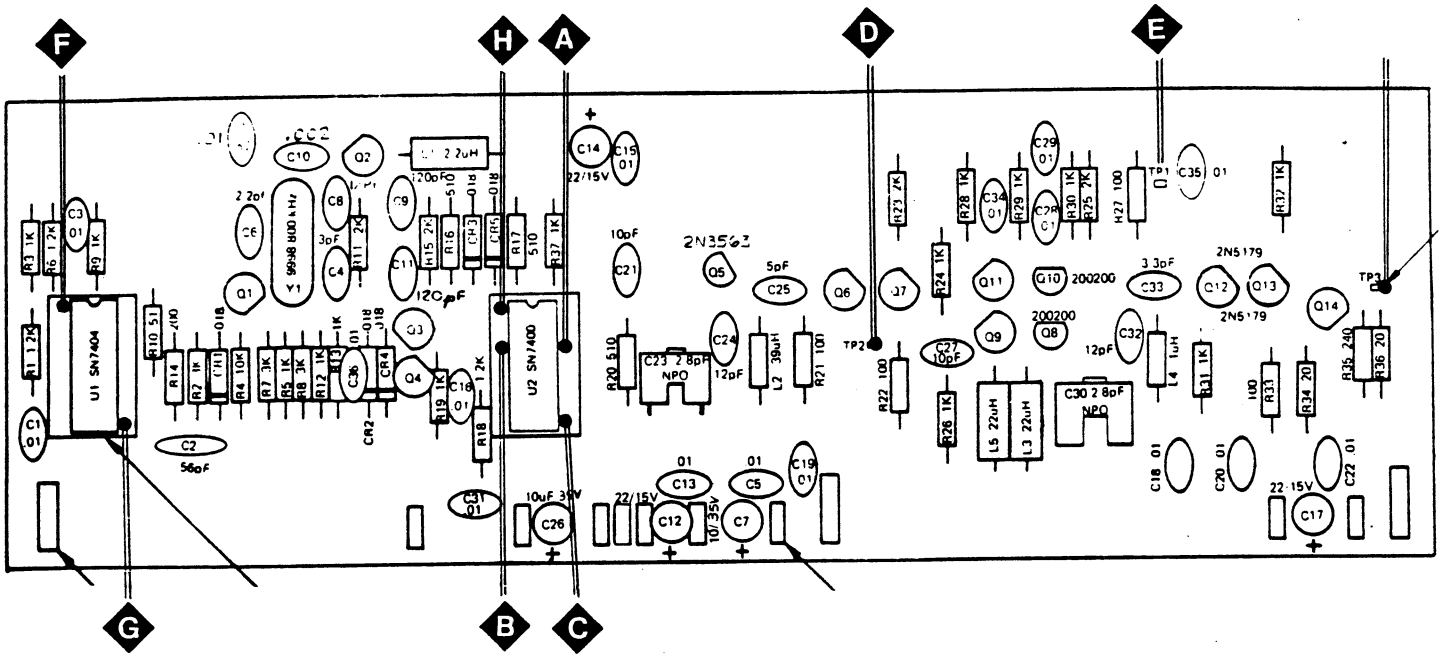


Figure 5.8 - Reference PCB Preliminary Unit Performance Test Points

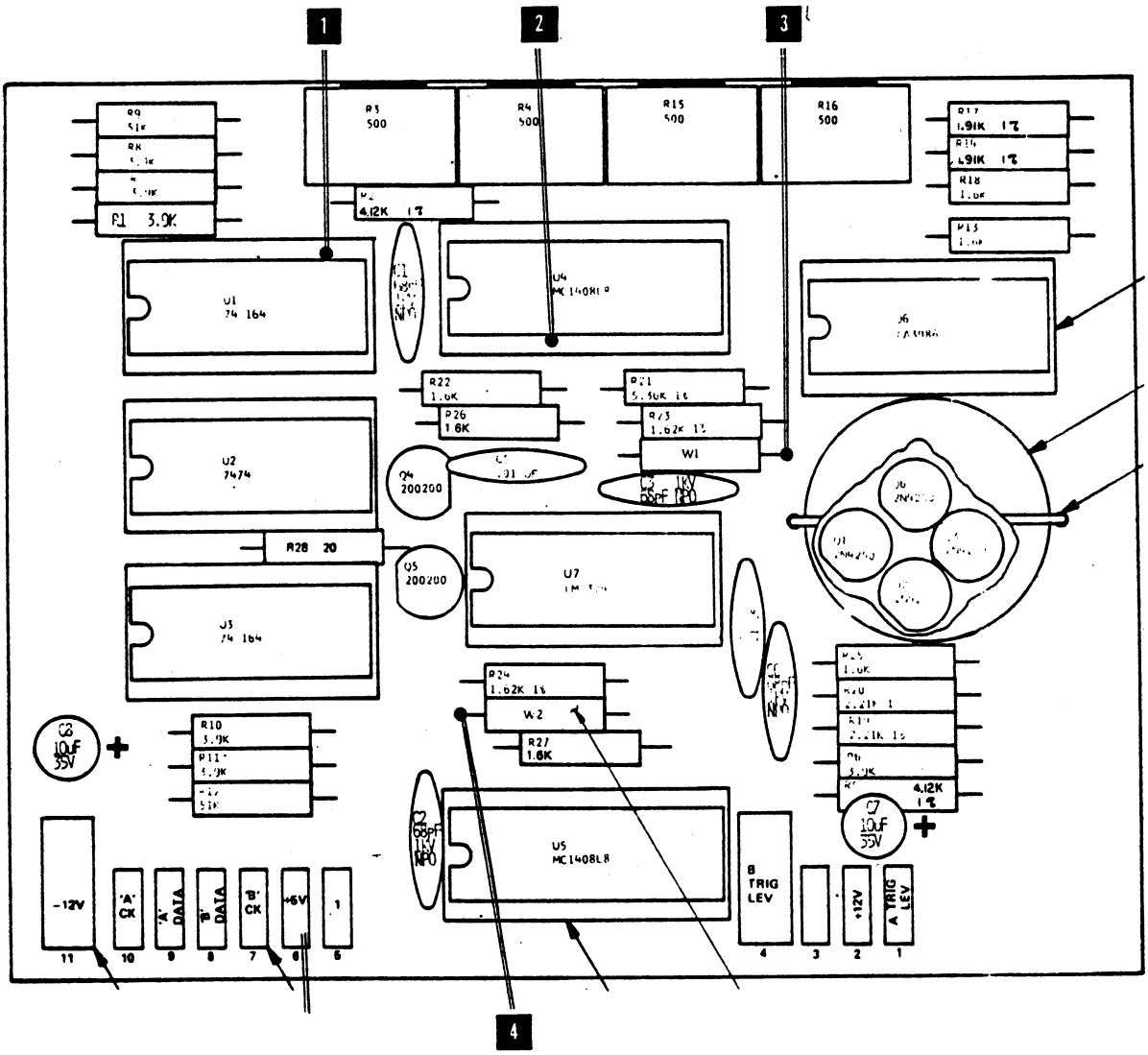
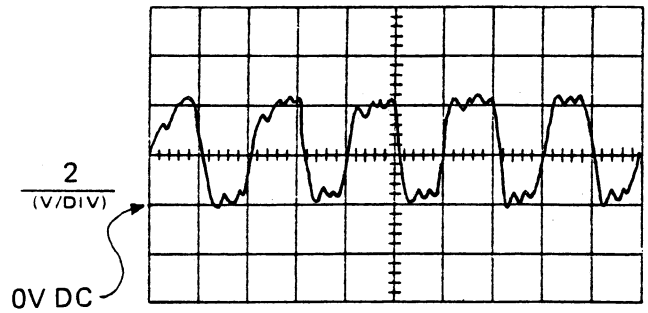


Figure 5.9 - DAC PCB Preliminary Unit Performance Test Points

WAVEFORMS FOR REFERENCE PCB PRELIMINARY UNIT
PERFORMANCE TEST

1 (NO.) U2-12

10 MHz (TCRO)



50 nSEC/DIV

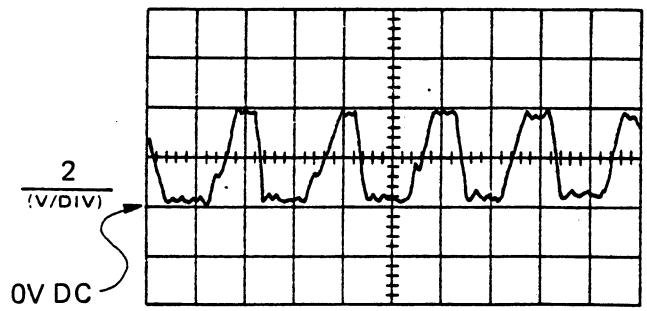
2 (NO.) U2-3

10 MHz DRIVE

50 nS/DIV

3 (NO.) U2-8

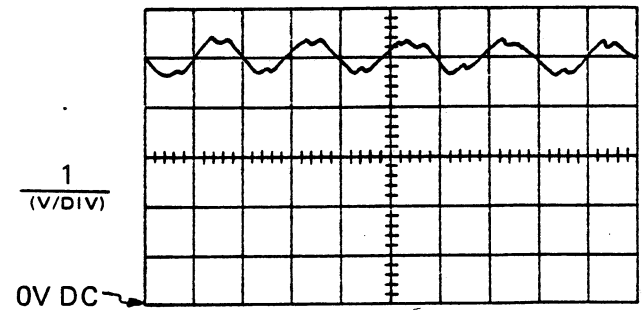
10 MHz OUTPUT



50 nSEC/DIV

4 (NO.) TP2

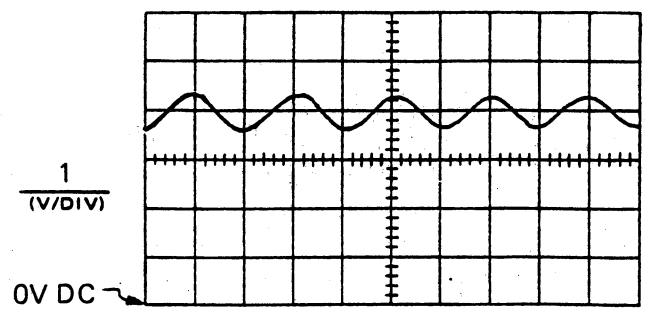
50 MHz DRIVE



10 nSEC/DIV

5 (NO.) TP3

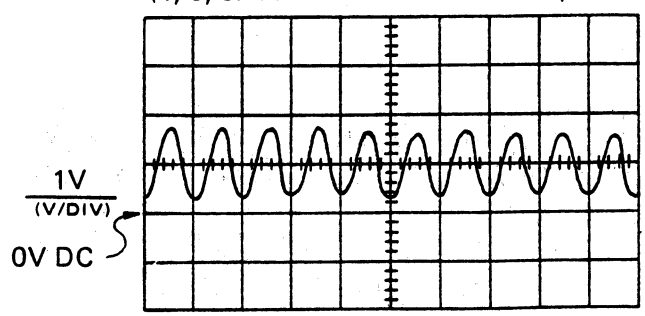
100 MHz OUT



(S/DIV)

6 (NO.) U1-1

EXT REF INPUT
(1, 5, or 10 MHz 1V RMS INPUT)



1 MHz EXT REF IN USE 1 μSEC/DIV
5 MHz EXT REF IN USE .2 μSEC/DIV
10 MHz EXT REF IN USE .1 μSEC/DIV

WAVEFORMS FOR REFERENCE PCB PRELIMINARY UNIT PERFORMANCE TEST (Continued)

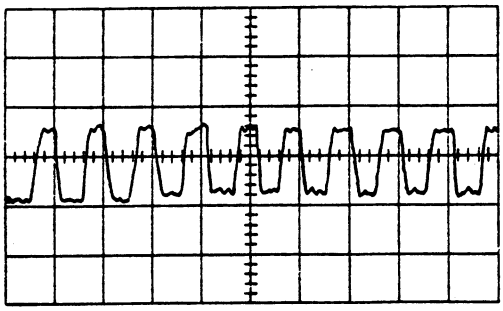
7 (NO.)

U1-8 EXT REF (TTL)

1, 5, or 10 MHz

2 (V/DIV)

0V



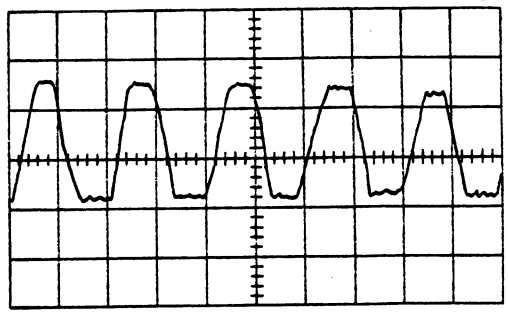
1 MHz EXT REF IN = 1 μSEC/DIV
5 MHz EXT REF IN = .2 μSEC/DIV
10 MHz EXT REF IN = .1 μSEC/DIV

8 (NO.)

U2-1 SIGNAL DETECTOR/GATE

(10 MHz)

2 (V/DIV)



50 nSEC/DIV

Table 5.9 - Frequency A (FA) Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Extend the Ch A sig cond with P/N 406851 extender PCB					Note: Measurement reference for Ch A sig cond is TP1
Ch A switches: Slope: Coupling: Sep/Test/Com: Sep Norm/Hold: Norm Keyboard: IT (Initialize) FA					Note: Sig cond assy shields must be removed for test
					Note: Scope trig on plus edge of TP7, "GATE"
					Note: Main logic measurement reference is CR11 (ANODE)
Apply a square wave input signal of 1V @ 1 KHz to Ch A (Scope Cal) Keyboard: (Ch A) TL, AU	Sig cond input signal	J17 (center pin)	A	Fig 5.11	Waveform #1
	Amplifier input	Q1a (gate)	B	Fig 5.11	Waveform #2
	Buffered input	U3-8	C	Fig 5.11	Waveform #3
	DAC output	Q1b (gate)	1	Fig 5.11	Ch A status voltage ±0.0125 VDC (approx. +0.5 VDC)
	+ slope (TTL)	R42/43 junction	2	Fig 5.11	TTL 1 (≥ 2.4 VDC)
	– slope drive	U1-8	3	Fig 5.11	TTL 0 (≤0.8 VDC)
	–slope signal	U2-4	4	Fig 5.11	≤ VDC
	+ slope drive	U2-14	D	Fig 5.11	Waveform #4
	+ slope signal	U2-2	E	Fig 5.11	Waveform #5
Ch A switch: Slope:	+ slope (TTL)	R42/43 junction	2	Fig 5.11	TTL 0 (≤ 0.8 VDC)
	– slope drive	U1-8	F	Fig 5.11	Waveform #6
	– slope signal	U2-4	G	Fig 5.11	Waveform #7
	+ slope drive	U2-14	5	Fig 5.11	≤ 0.8 VDC
	+ slope signal	U2-2	6	Fig 5.11	≤ VDC
	TI · TIA	CR14 (cathode)	7	Fig 5.11	TTL, 1 (≥ +2.4 VDC)
Ch A switch: Slope:	ECL signal out	U2-3	H	Fig 5.11	Waveform #8
Sig. cond. voltages and waveforms unavailable, see sig. cond. subassembly performance test					
	Main logic control register bits	U32, 33, 34 (see pin # in chart below)	1	Fig 5.12	Verify logic levels (TTL) 1 = ≥ +2.4 VDC, 0 = ≤ +0.8 VDC

Table 5.9 - Frequency A (FA) Unit Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard

HOME STATE		(PI+TI) + 10 nSec	PA + TIA + (TI+P) 10 nSec	P + PA + TI	TIA	$\overline{32}$	$\overline{31}$	$\overline{30}$	100 nSEC	10 nSec
		TIMEBASE MULTIPLIER CONTROL								
	FUNCT	2	4	13	19	16	17	18	14	15
	FA	1	1	1	0	1	0	1	0	0
	U NO.	33				34				
	PIN	6	5	4	3	5	4	3	13	12

	FC	P + TI + PA + TIA	$\overline{P}$	P + TI + TO	$\overline{A/B}$	$\overline{TIA}$	$\overline{PA + TO}$	$\overline{TI}$	PA + TIA + N_B + TO	FA + FC + TIA	$\overline{TO}$	$\overline{TI + TIA}$
	MODE CONTROL											
	1	3	5	6	7	8	9	10	11	12	20	21
	0	0	1	0	1	1	1	1	0	1	1	1
	32							33				
	6	5	4	3	13	12	11	10	13	12	11	10

	Signal detect ECL output	U6-2	A	Fig 5.12	Waveform #1
	100 MHz reference	U2-9	B	Fig 5.12	Waveform #2
	Gate input signal	U15-14	C	Fig 5.12	Waveform #3
	Time base steering out signal	U44-8	D	Fig 5.12	Waveform #4
	CLEAR	TP5	E	Fig 5.12	Waveform #5
	GATE	U17-9	F	Fig 5.12	Waveform #6
	Decade counter in	U41-15	G	Fig 5.12	Waveform #7
	UPDATE	U43-12	H	Fig 5.12	Waveform #8
	Accumulator clock	U50-11	I	Fig 5.12	Waveform #9
	Accumulator data	U46-9	J	Fig 5.12	Waveform #10

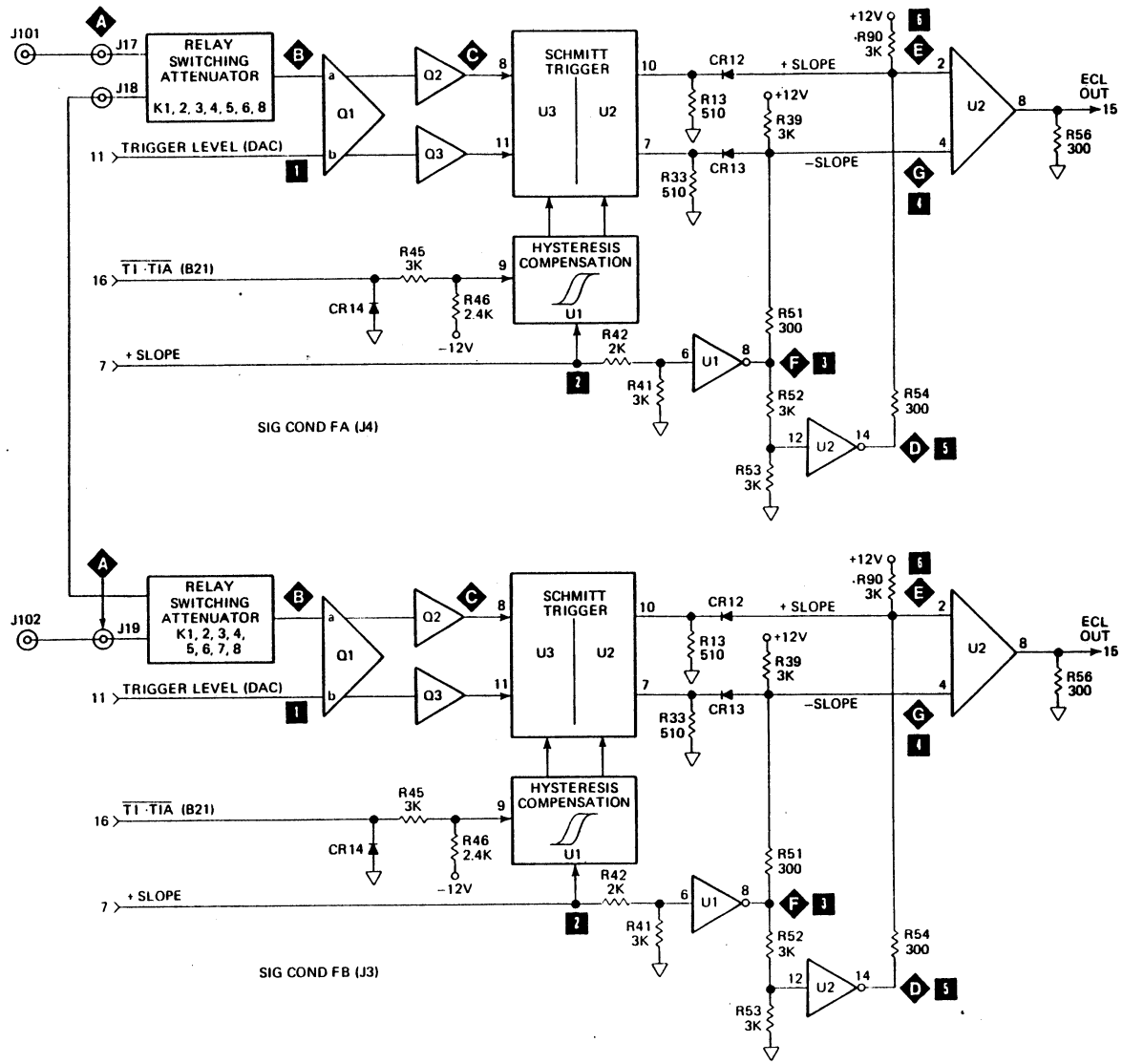


Figure 5.10 - Frequency A (Frequency B) Functional Block Diagram

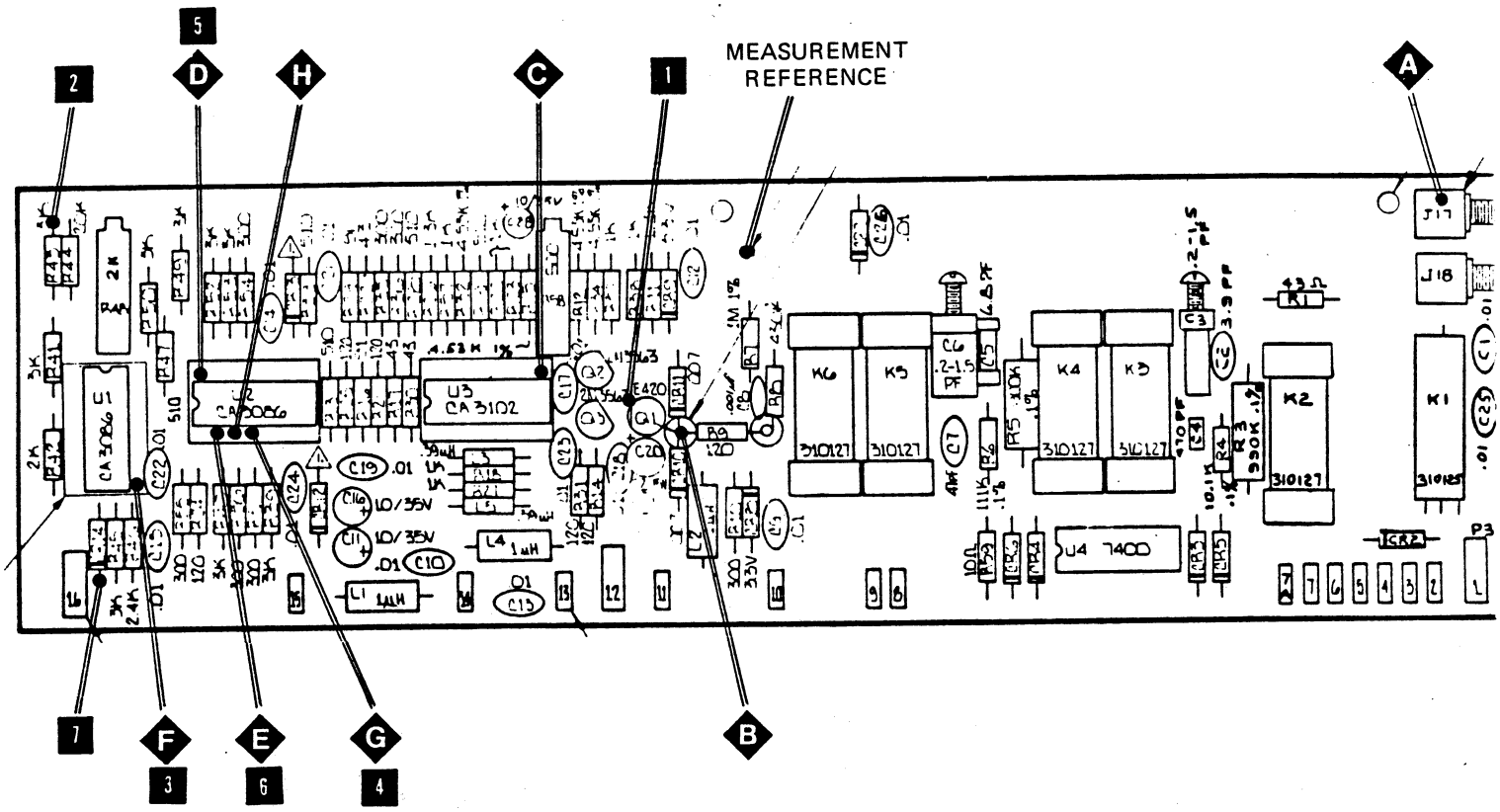


Figure 5.11 - Frequency A (FA Sig Cond) Unit Performance Test Points

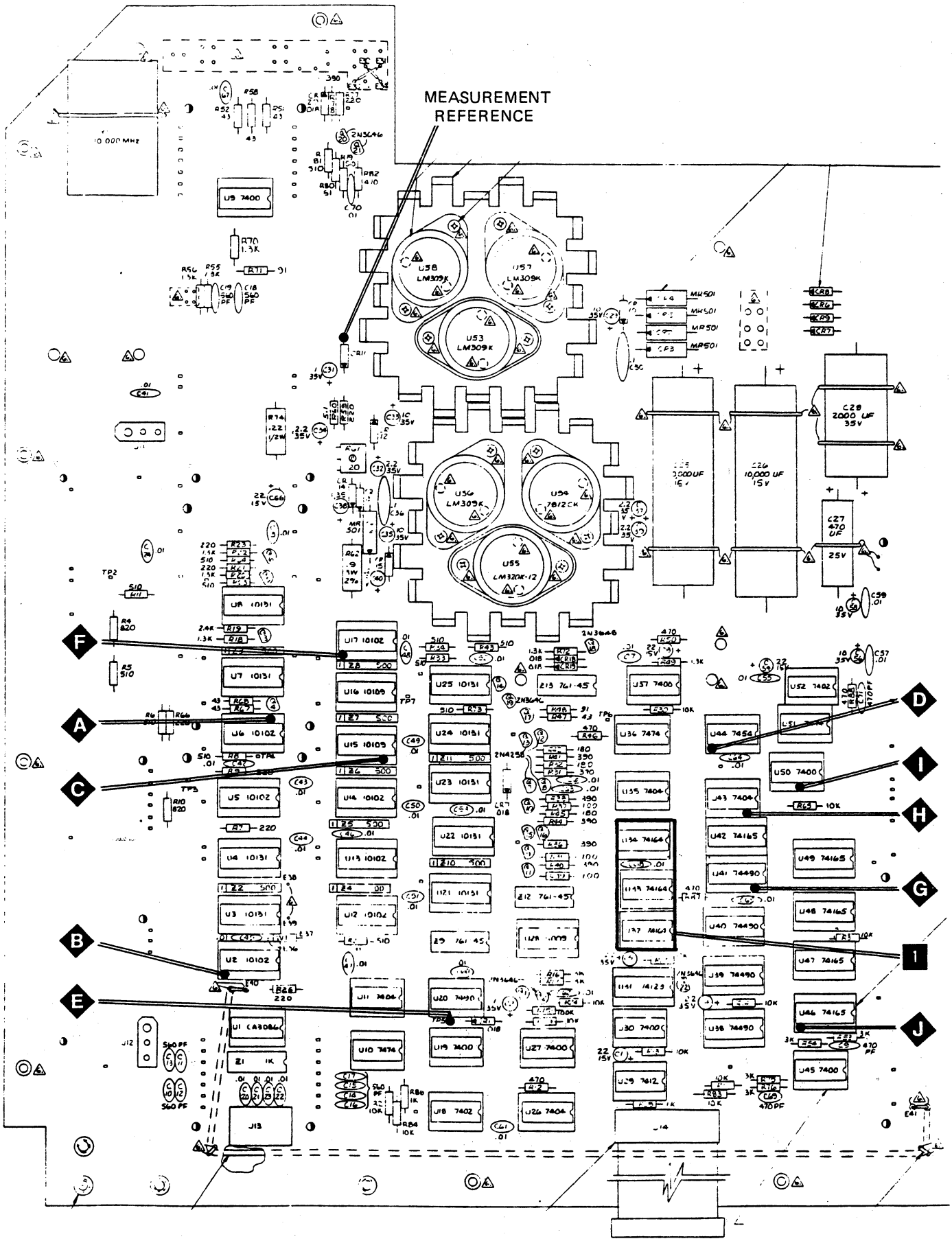
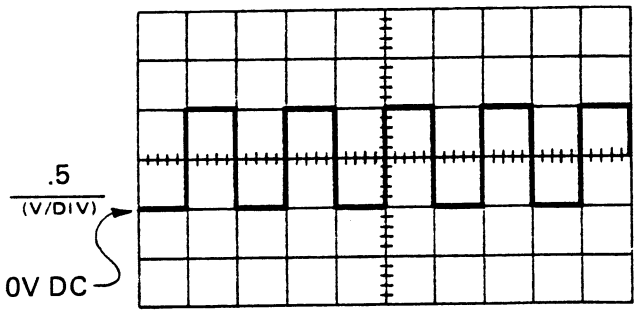


Figure 5.12 - Frequency A (Main Logic) Unit Performance Test Points

WAVEFORMS FOR FREQUENCY A (FA SIG COND)
UNIT PERFORMANCE TEST

1 (NO.) J17 (CENTER PIN)

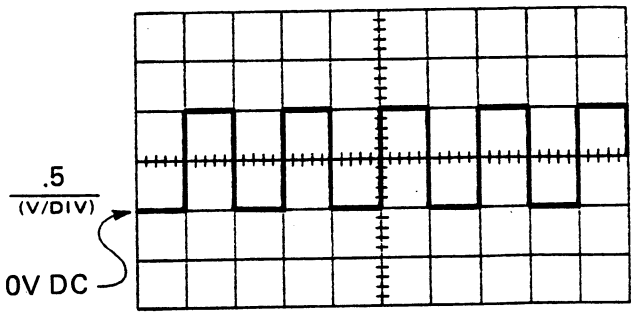
INPUT



.5 mSEC/DIV

2 (NO.) Q1a (GATE)

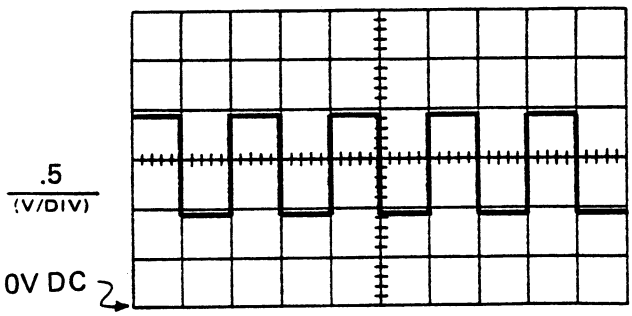
AMP INPUT



.5 mSEC/DIV

3 (NO.) U3-8

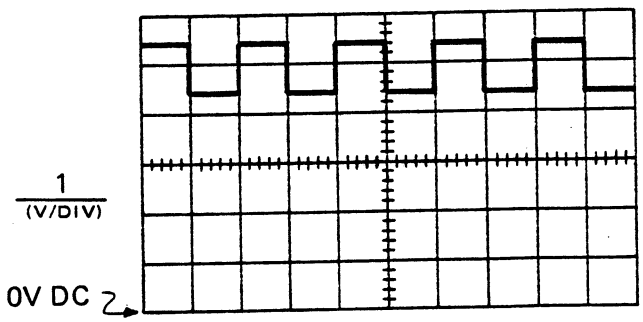
BUFFERED INPUT



.5 mSEC/DIV

4 (NO.) U2-14

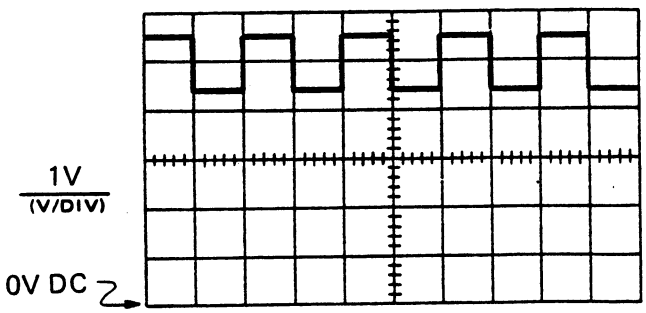
+ SLOPE DRIVE



.5 mSEC/DIV

5 (NO.) U2-2

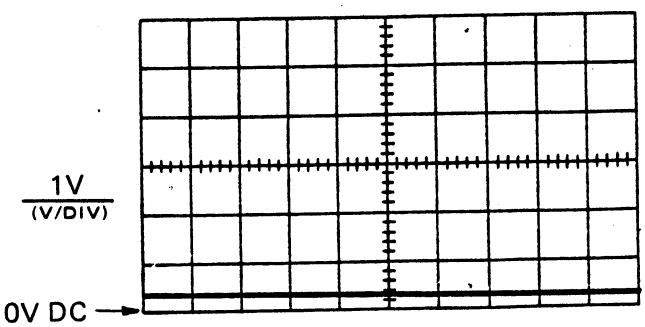
+ SLOPE SIGNAL



.5 mSEC/DIV

6 (NO.) U1-8

– SLOPE DRIVE

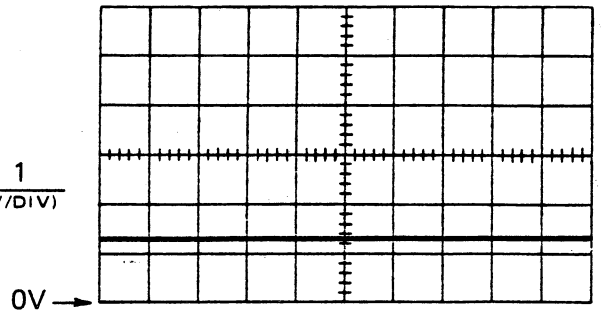


.5 mSEC/DIV

WAVEFORMS FOR FREQUENCY A (FA SIG COND) UNIT PERFORMANCE TEST (Continued)

7 (NO.) U2-4

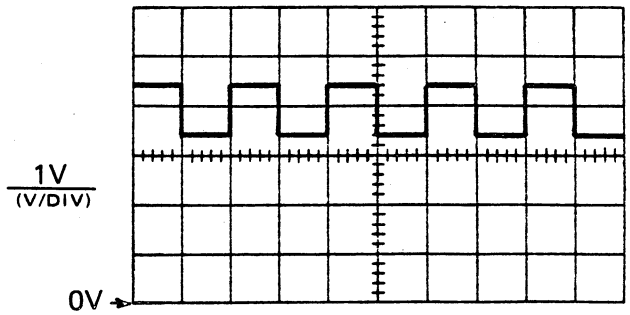
– SLOPE SIGNAL



.5 mSEC/DIV

8 (NO.) U2-3

ECL SIGNAL OUT

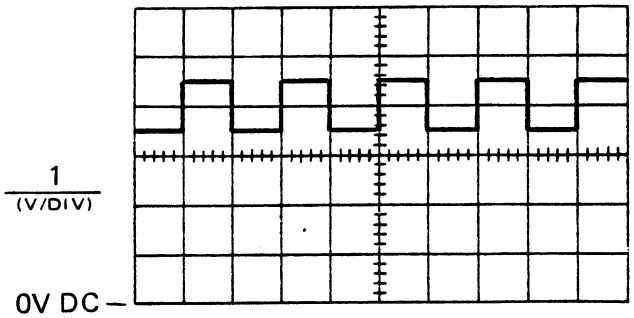


.5 mSEC/DIV

WAVEFORMS FOR FREQUENCY A (MAIN LOGIC)
UNIT PERFORMANCE TEST

1 (NO.) U6-2

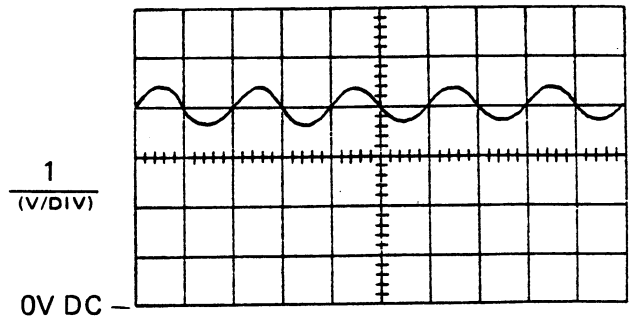
SIG DET ECL OUT



.5 mSEC/DIV

2 (NO.) U2-9

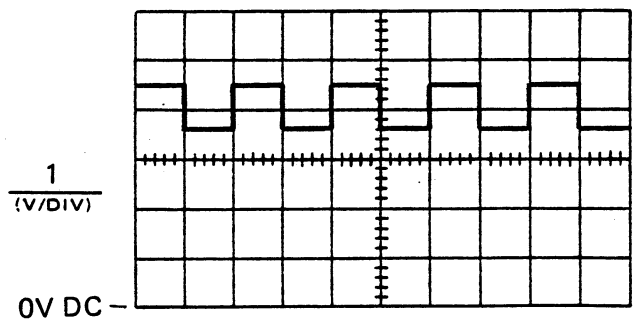
100 MHz REFERENCE
(USE INTERNAL TRIGGER SOURCE ON SCOPE)



5 nSEC/DIV

3 (NO.) U15-14

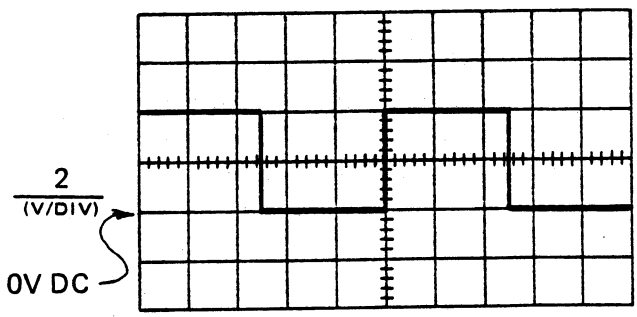
GATE INPUT SIGNAL
(TRIGGER SCOPE ON TP7)



.5 mSEC/DIV

4 (NO.) U44-8

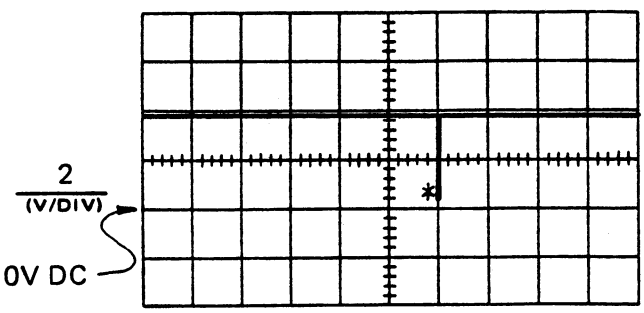
TIME BASE STEERING OUT SIGNAL



20 mSEC/DIV

5 (NO.) TP5

$\overline{\text{CLEAR}}$

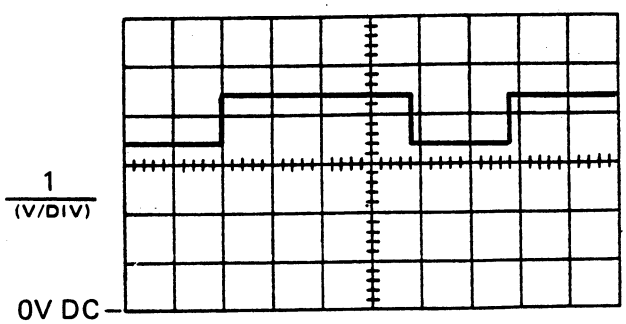


* NOTE
P.W. ≈ 50 μSEC

20 mSEC/DIV

6 (NO.) U17-9

$\overline{\text{GATE}}$

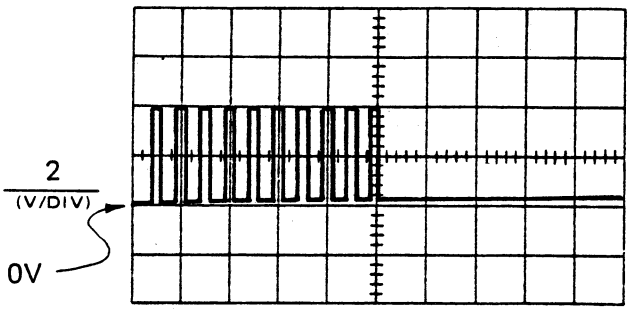


50 mSEC/DIV

WAVEFORMS FOR FREQUENCY A (MAIN LOGIC)
UNIT PERFORMANCE TEST

7 (NO.) U41-15

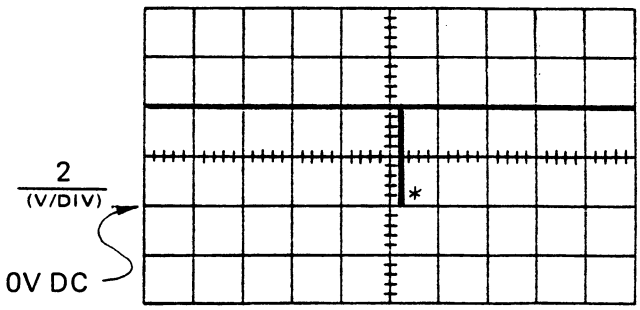
DECADE COUNTER IN



20 mSEC/DIV

8 (NO.) U43-12

$\overline{\text{UPDATE}}$

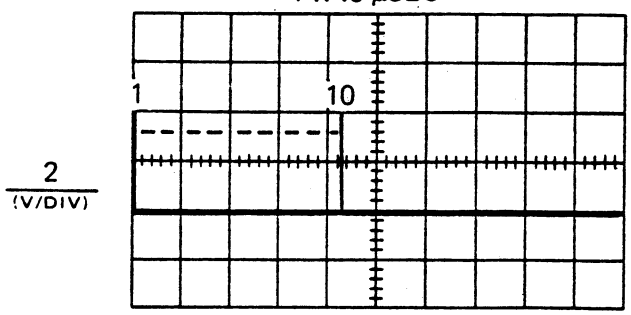


*NOTE
P.W. ≈ 12 μSEC

.2 mSEC/DIV

9 (NO.) U50-11

ACCUMULATOR CLOCK*
(10 GROUPS OF PULSES W/4 PULSES)
PW .6 μSEC



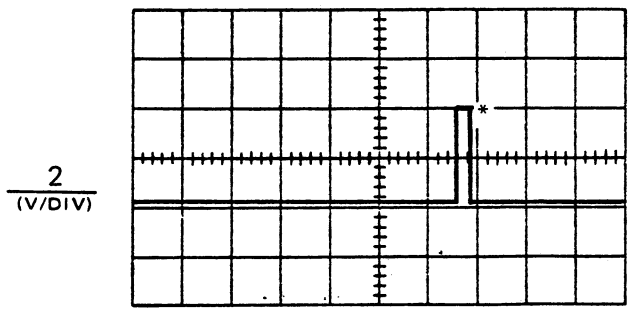
NOTE

USE INTERNAL TRIGGER "↑" SLOPE

.5 mSEC/DIV

10 (NO.) U46-9

ACCUMULATOR DATA*



NOTE

USE "↓" EDGE OF TP7 FOR EXT TRIG SOURCE

.5 mSEC/DIV

*APPROX POSITION OF PULSE.
PULSE POSITION WILL VARY ≈ 3.5 DIV.
PW 33 μSEC

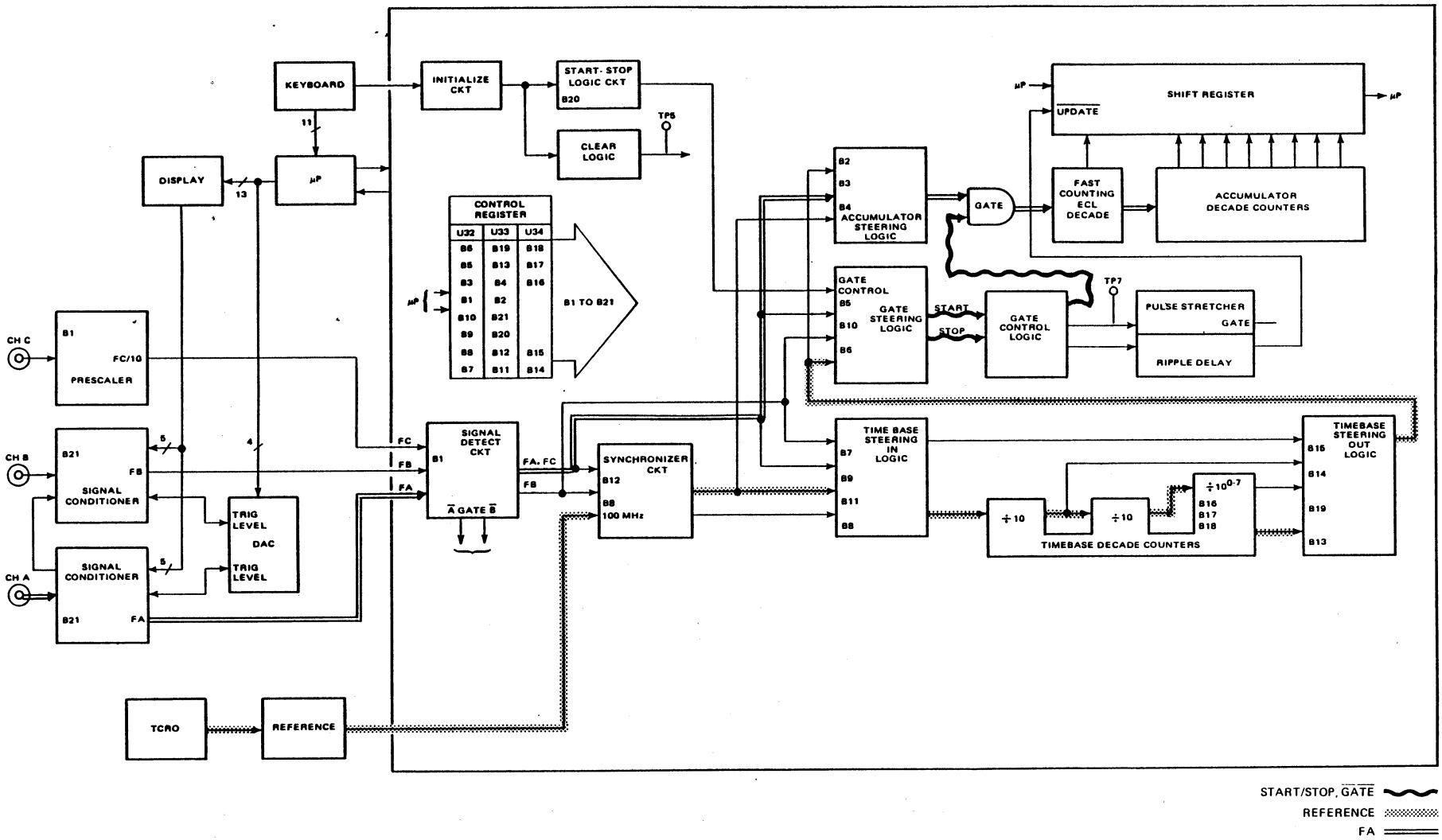


Figure 5.13 - Frequency A (FA) Single Thread Diagram

Table 5.10 - Frequency C (FC) Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
See preliminary unit performance test for main logic ECL supply voltage and reference PCB tests. DAC PCB not used for frequency C.					
Extend the (FC) pre-scaler assy with P/N 406851 extender PCB					Note: Measurements referenced to TP1 on prescaler PCB
Keyboard: IT (Initialize) FC					Note: The prescaler shields can be removed for test
Apply an input signal of 100 MHz @ 50 mV RMS to the Ch C input					"IN-RANGE" below status on the front panel must be annunciated
	ECL supply voltage (+12V)	C52 (+ lead)	1	Fig 5.15	+12.0 VDC ± 0.05 VDC
	Signal input	F1/C2 junction	A	Fig 5.15	Waveform #1
	1st amp output	U4-1	B	Fig 5.15	Waveform #2
	2nd amp output	U2-10	C	Fig 5.15	Waveform #3
	÷ 10 output	U2-4	D	Fig 5.15	Waveform #4
	AGC input	TP2	2	Fig 5.15	+0.6 VDC ± 0.1 VDC
	AGC output	R11/12 junction	3	Fig 5.15	+5.3 VDC ± 0.05 VDC
	FC logic enable	Q5 (emitter)	4	Fig 5.15	+0.5 VDC ± 0.05 VDC
	FC gate enable	U3-12	5	Fig 5.15	ECL low (≤ +3.6 VDC
	$\overline{\text{IN-RANGE}}$	Q7 (collector)	6	Fig 5.15	TTL 0 (≤ 0.8 VDC)
	FC/10 output	U3-15	E	Fig 5.15	Waveform #5
Prescaler voltages and waveforms unavailable, see prescaler subassembly performance test.					
	Main logic control register bits	U32, 33, 34 (See pin # in following chart)	1	Fig 5.16	Verify logic levels (TTL) 1 = ≥ +2.4 VDC 0 = ≤ +0.8 VDC

Table 5.10 - Frequency C (FC) Unit Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard

HOME STATE

	(PI+TI) + 10 nSec	PA + TIA + (TI+P) 10 nSec	P + PA + TI	TIA	2^2	2^1	2^0	100 nSEC	10 nSec	FC	P + TI + PA + TIA	$\overline{P}$	P + TI + TO	$\overline{A/B}$	$\overline{TIA}$	$\overline{PA + TO}$	$\overline{TI}$	PA + TIA + N_B + TO	FA + FC + TIA	$\overline{TO}$	$\overline{TI + TIA}$
	TIMEBASE/MULTIPLIER CONTROL									MODE CONTROL											
FUNCT	2	4	13	19	16	17	18	14	15	1	3	5	6	7	8	9	10	11	12	20	21
FC	1	1	1	0	1	0	1	0	0	1	0	1	0	1	1	1	1	0	1	1	1
U NO.	33				34					32							33				
PIN	6	5	4	3	5	4	3	13	12	6	5	4	3	13	12	11	10	13	12	11	10

	Signal detect FC/10 ECL out	U6-2	A	Fig 5.16	Waveform #1
	100 MHz reference	U2-9	B	Fig 5.16	Waveform #2
	ECL counter input signal	U14-14	C	Fig 5.16	Waveform #3
	Timebase steering out signal	U44-8	D	Fig 5.16	Waveform #4
	$\overline{CLEAR}$	TP5	E	Fig 5.16	Waveform #5
	$\overline{GATE}$	U17-9	F	Fig 5.16	Waveform #6
	Decade counter input (TTL)	U41-15	G	Fig 5.16	Waveform #7
	$\overline{UP\ DATE}$	U43-12	H	Fig 5.16	Waveform #8
	Accumulator clock	U50-11	I	Fig 5.16	Waveform #9
	Accumulator data	U46-9	J	Fig 5.16	Waveform #10

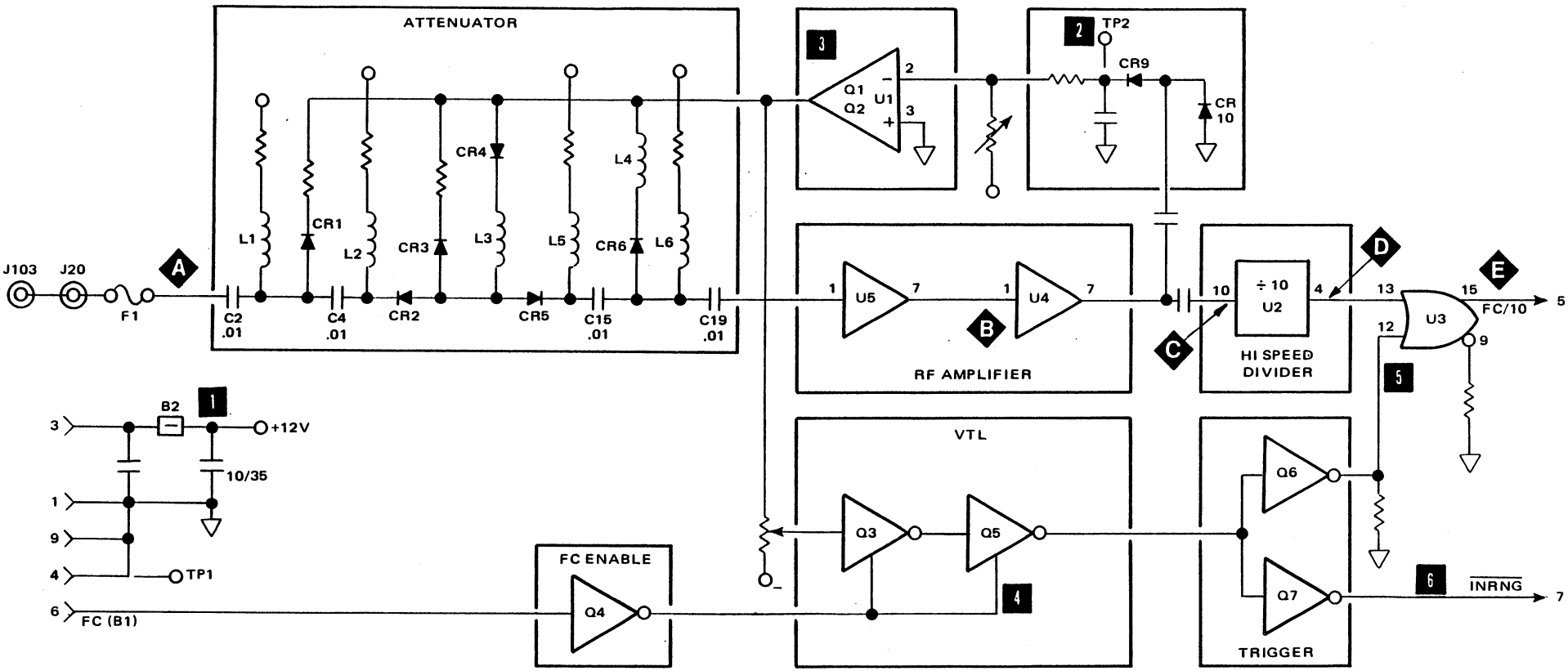


Figure 5.14 - Frequency C (Prescaler) Functional Block Diagram

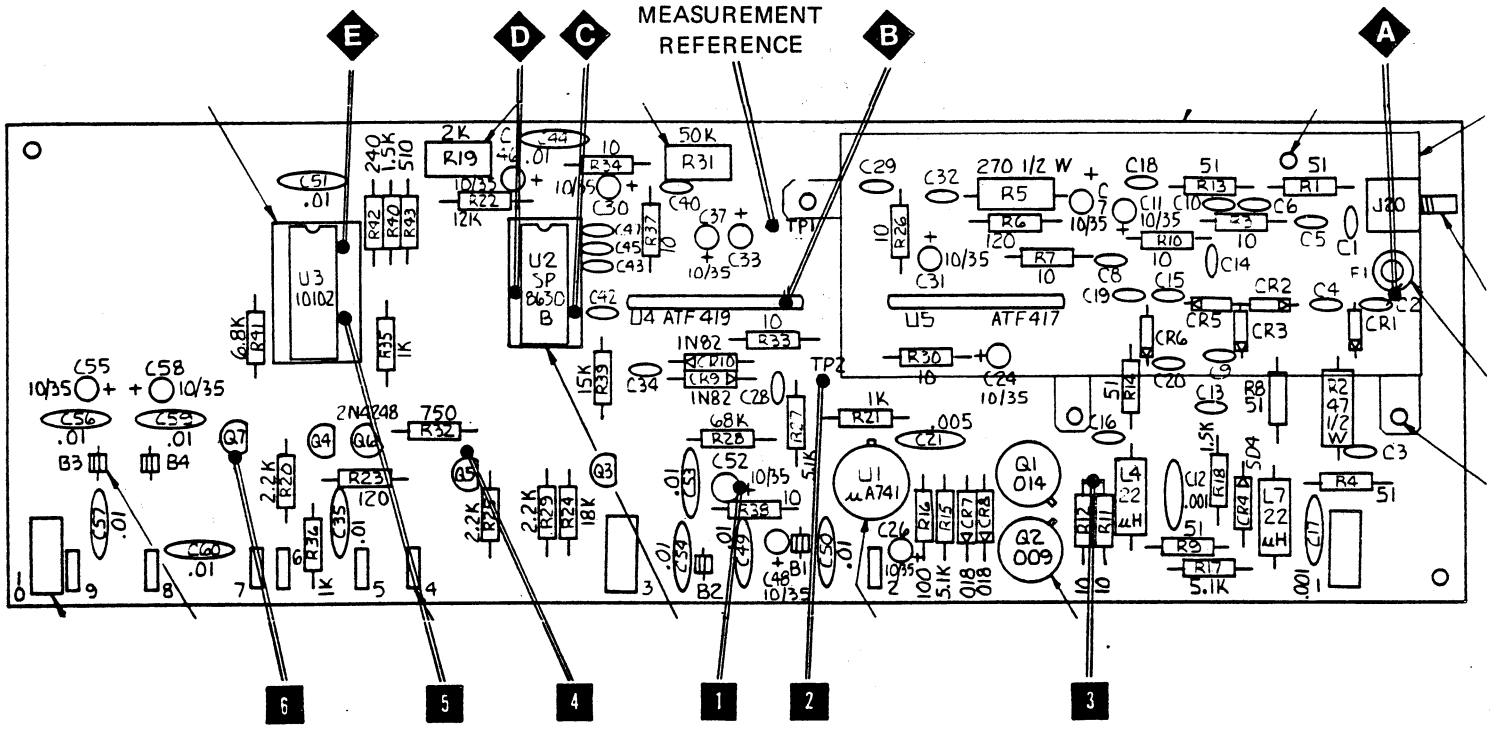
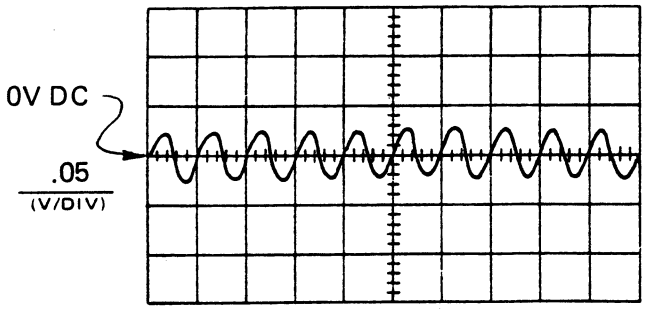


Figure 5.15 - Frequency C (Prescaler) Unit Performance Test Points

WAVEFORMS FOR FREQUENCY C (PRESCALER)
UNIT PERFORMANCE TEST

1 (NO.) F1/C2

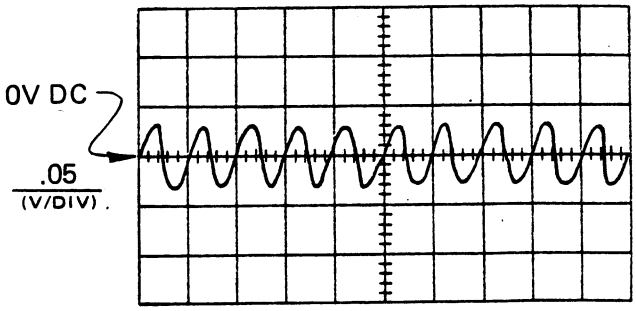
SIGNAL INPUT



10 nSEC/DIV

2 (NO.) U4-1

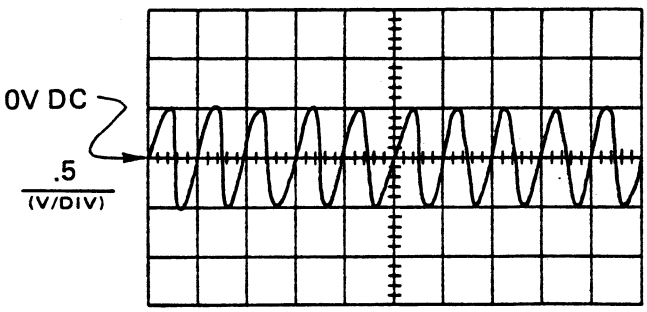
1ST AMP OUT



10 nSEC/DIV

3 (NO.) U2-10

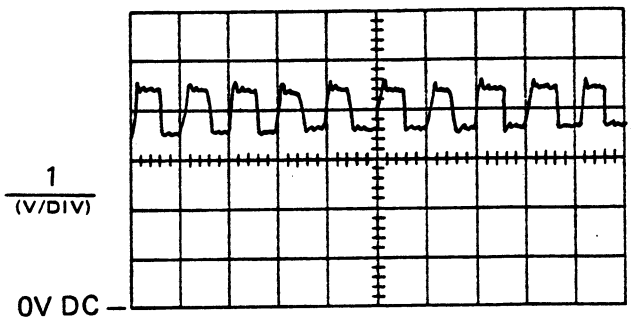
2ND AMP OUT



10 nSEC/DIV

4 (NO.) U2-4

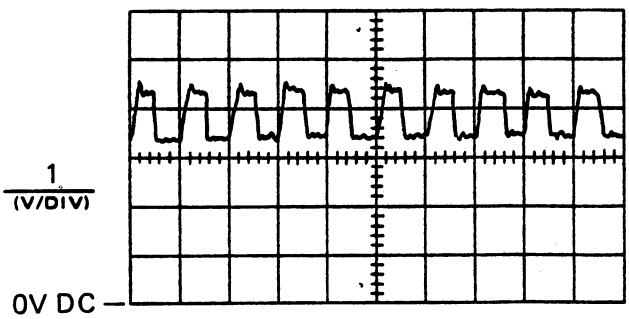
÷10 OUTPUT



100 nSEC/DIV

5 (NO.) U3-15

FC/10 OUTPUT



100 nSEC/DIV

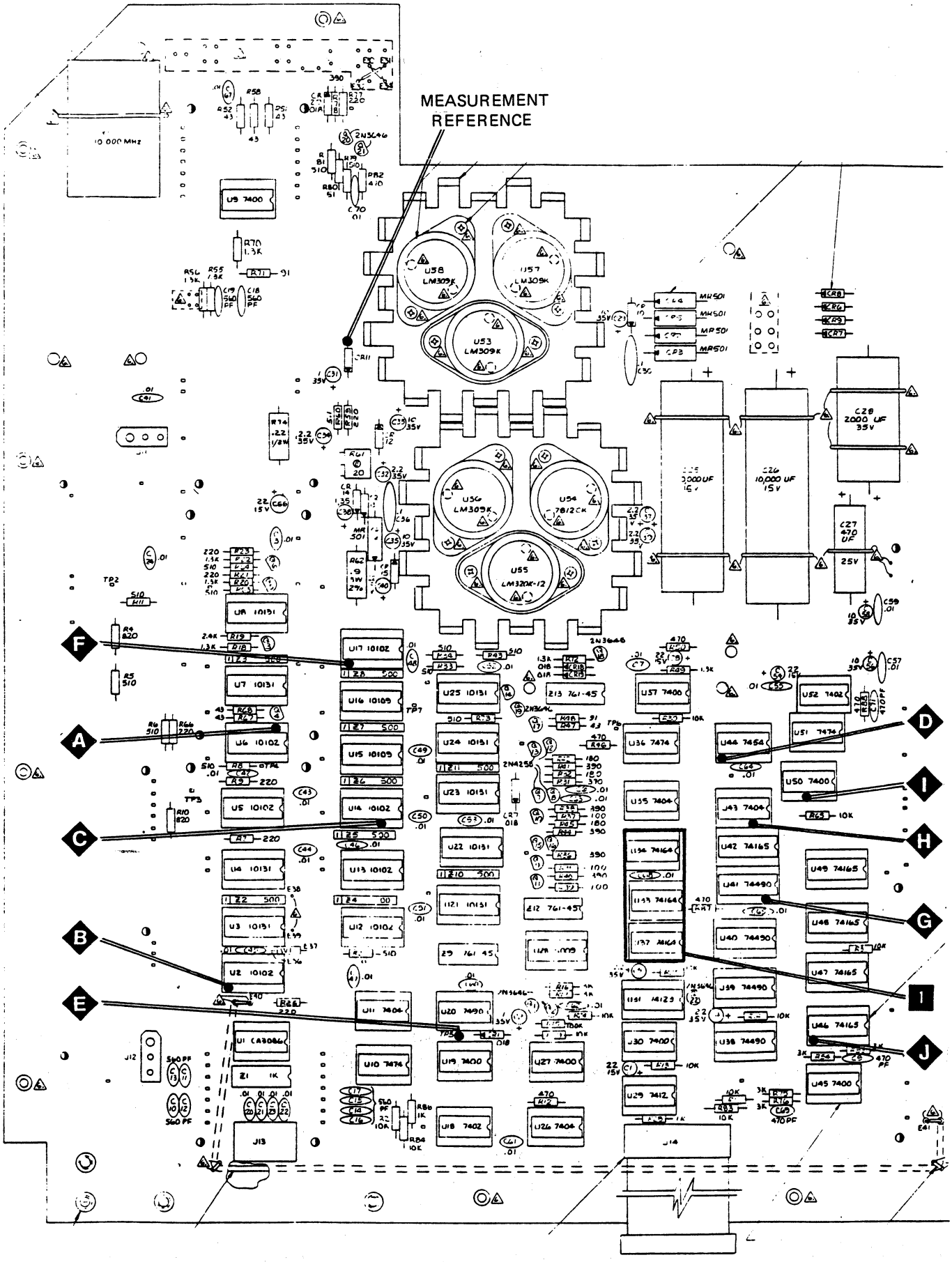
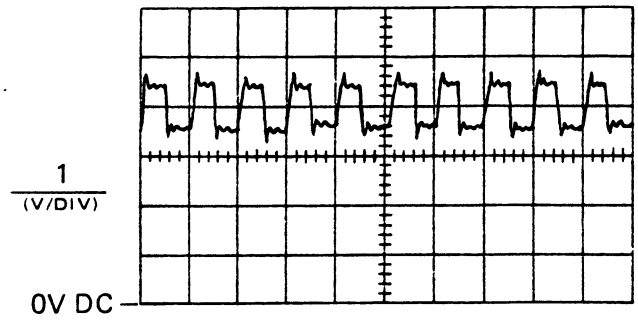


Figure 5.16 - Frequency C (Main Logic) Unit Performance Test Points

WAVEFORMS FOR FREQUENCY C (MAIN LOGIC)
UNIT PERFORMANCE TEST

1 (NO.) U6-2

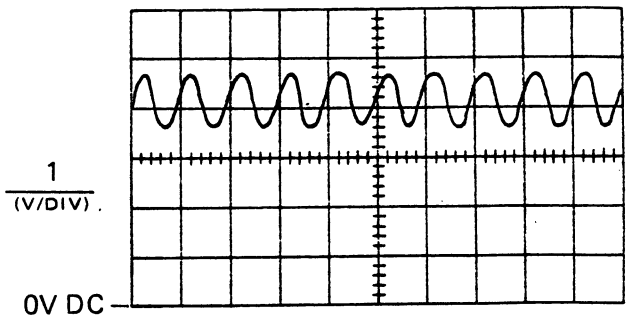
SIGNAL DETECT FC/10 ECL OUT



.1 mSEC/DIV

2 (NO.) U2-9

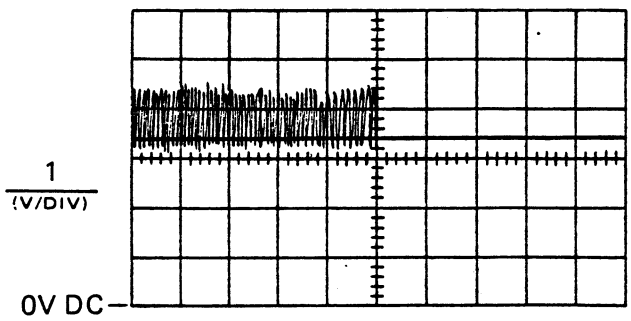
100 MH REFERENCE



10 nSEC/DIV

3 (NO.) U14-14

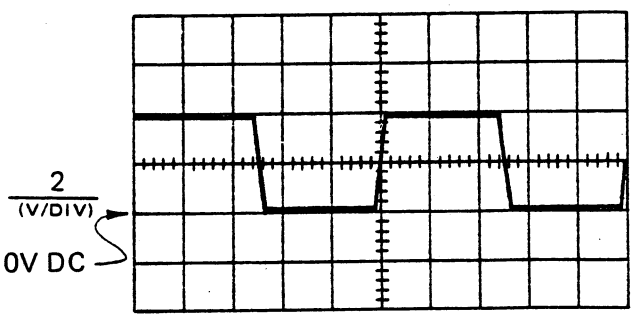
ECL COUNTER INPUT
(TRIG ON " " EDGE OF TP7)



20 mSEC/DIV

4 (NO.) U44-8

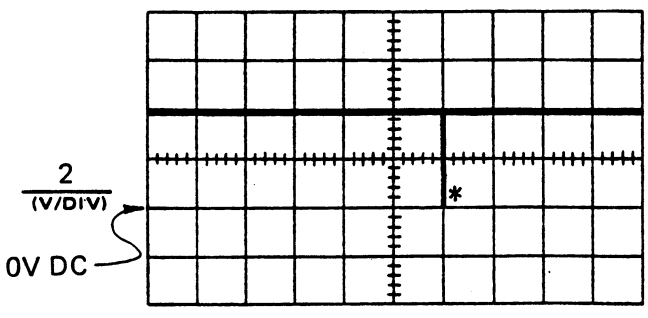
TIMEBASE STEERING OUT SIGNAL



20 mSEC/DIV

5 (NO.) TP5

$\overline{\text{CLEAR}}$

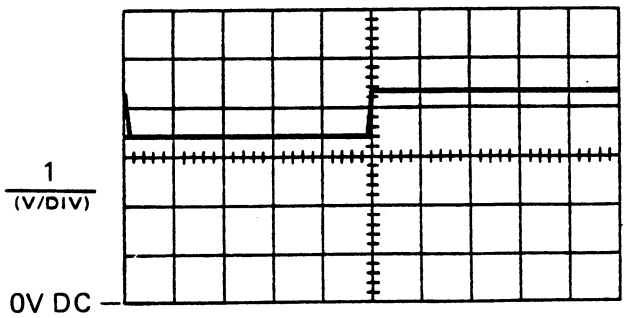


20 mSEC/DIV

*NOTE: PW≈ 50 μSEC

6 (NO.) U17-9

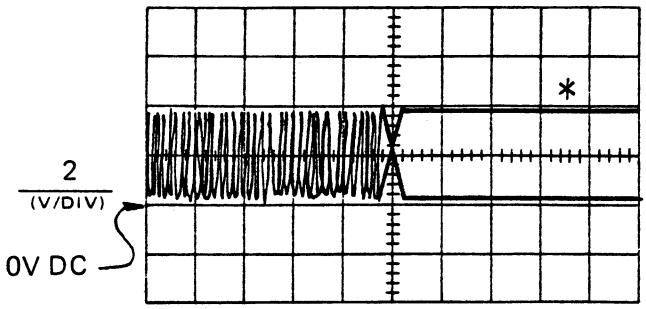
$\overline{\text{GATE}}$



20 mSEC/DIV

WAVEFORMS FOR FREQUENCY C (MAIN LOGIC) UNIT PERFORMANCE TEST (Continued)

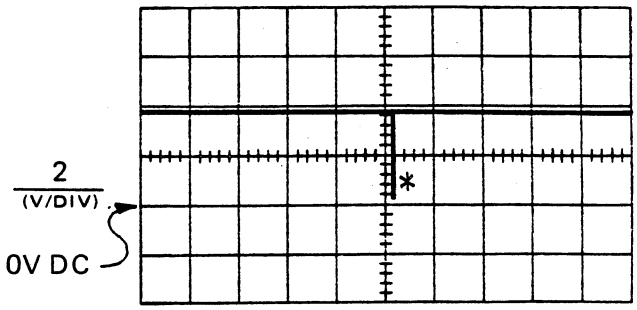
7 (NO.) U41-15
DECADE COUNTER INPUT
(1 PULSE WIDTH x .2 μSEC AND PER ≈100 nSEC)



20 mSEC/DIV

* NOTE:
SIGNAL CAN END IN HI OR LOW STATE

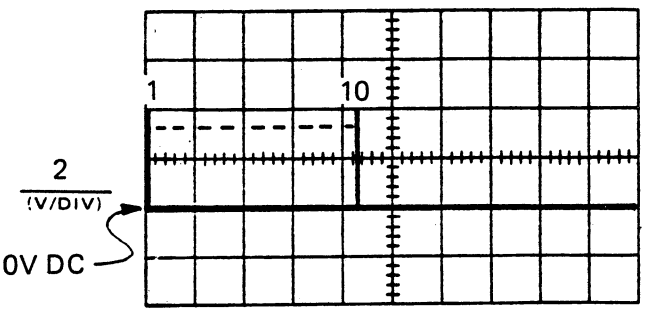
8 (NO.) U43-12
UPDATE



.5 mSEC/DIV

NOTE: PN ≈12 μSEC

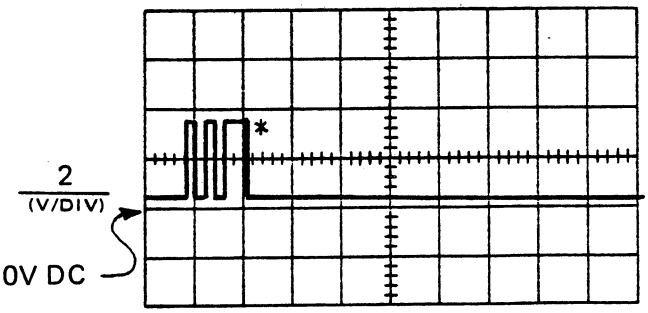
9 (NO.) U50-11
ACCUMULATOR CLOCK*
(USE INT TRIG↑EDGE)



.5 mSEC/DIV

*NOTE:
SIGNAL IS 10 GROUPS OF 4 PULSES PER GROUP

10 (NO.) U46-9
ACCUMULATOR DATA
(USE EXT TRIG "↓" EDGE OF TP7)



1 mSEC/DIV

NOTE:
WAVEFORM WILL VARY WITH FREQUENCY IN
@ FC = 100.0000 MHz ONLY 1 PULSE WILL APPEAR

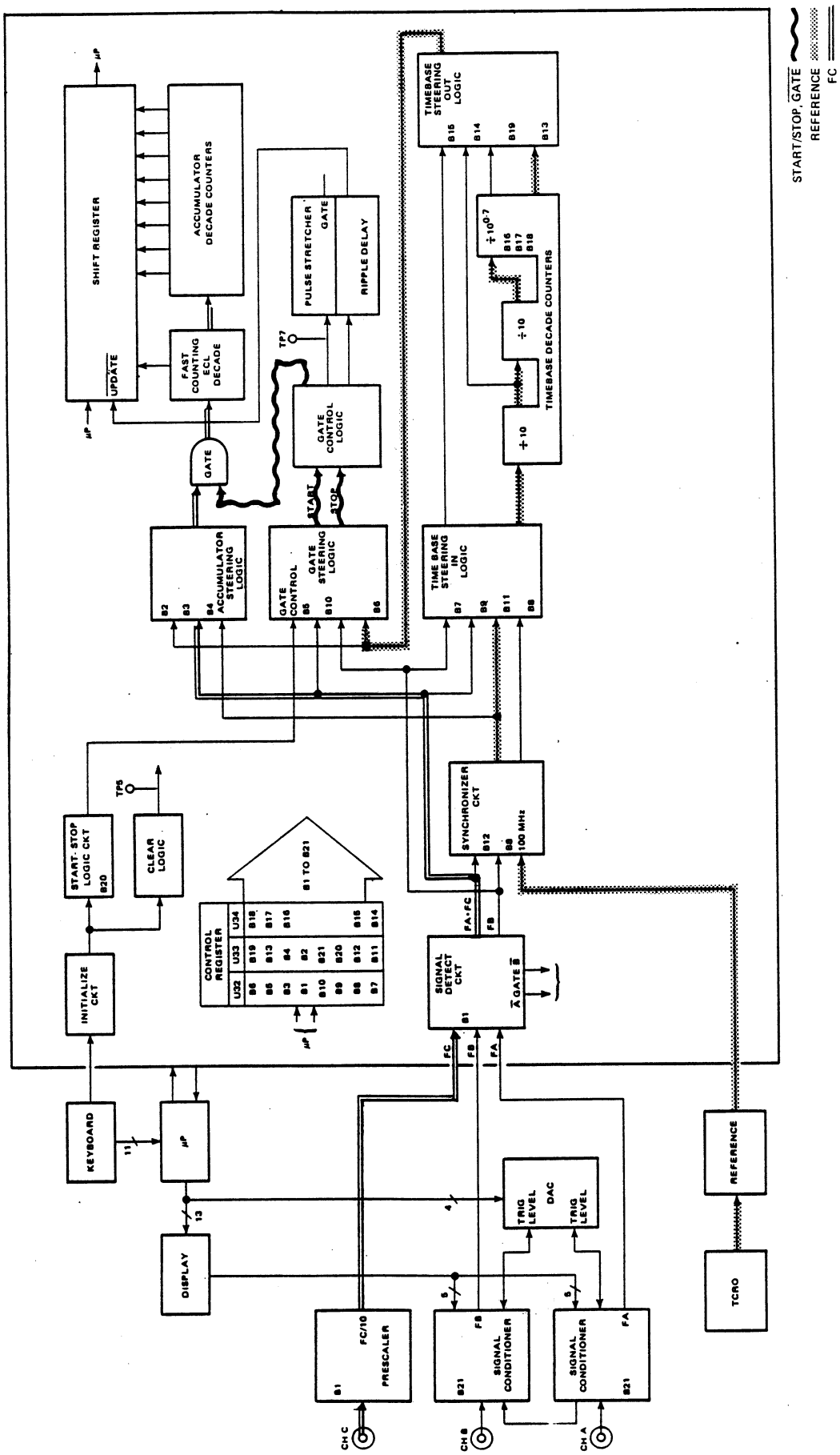


Figure 5.17 - Frequency C (FC) Single Thread Diagram

Table 5.11 - Period (P) Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
See preliminary unit performance test for main logic ECL supply voltage, reference PCB, and DAC PCB tests.					
See Frequency A (FA) unit performance test for Channel A signal conditioner tests.					
Keyboard switches: (Ch A) Normal/Hold: Hold Slope: Coupling: DC Set/Test/Com: Sep Keyboard: IT (initialize) P					Note: Measurement reference for main logic PCB @ CR11 (Anode) Note: Scope trigger on plus edge of TP7 (Gate)
Apply a square wave input signal of 1V @ 1 KHz to Ch A (scope cal signal) Keyboard: (Ch A) TL, AU					
	Main logic control register bits	U32, 33, 34 (see chart for pin location)	1	Fig 5.18	Verify logic levels (TTL) 1 = ≥ +2.4 VDC 0 = ≤ +0.8 VDC

HOME STATE		(PI+TI) + 10 nSec	PA + TIA + (TI+P) 10 nSec	P + PA + TI	TIA	2^2	2^1	2^0	100 nSEC	10 nSec	FC	P + TI + PA + TIA	$\overline{P}$	P + TI + TO	$\overline{A/B}$	$\overline{TIA}$	$\overline{PA + TO}$	$\overline{TI}$	PA + TIA + N_B + TO	FA + FC + TIA	$\overline{TO}$	$\overline{TI + TIA}$
		TIMEBASE/MULTIPLIER CONTROL									MODE CONTROL											
	FUNCT	2	4	13	19	16	17	18	14	15	1	3	5	6	7	8	9	10	11	12	20	21
	P	1	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	1	0	0	1	1
	U NO.	33				34					32							33				
	PIN	6	5	4	3	5	4	3	13	12	6	5	4	3	13	12	11	10	13	12	11	10

Table 5.11 - Period (P) Unit Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Signal detect FA ECL out	U6-2	A	Fig 5.18	Waveform #1
	100 MHz reference	U2-9	B	Fig 5.18	Waveform #2
	ECL counter input signal	U14-14	C	Fig 5.18	Waveform #3
	CLEAR	TP5	E	Fig 5.18	Waveform #5
	GATE	U17-9	F	Fig 5.18	Waveform #6
	Decade counter input (TTL)	U41-15	G	Fig 5.18	Waveform #7
	UPDATE	U43-12	H	Fig 5.18	Waveform #8
	Accumulator clock	U50-11	I	Fig 5.18	Waveform #9
	Accumulator data	U46-9	J	Fig 5.18	Waveform #10

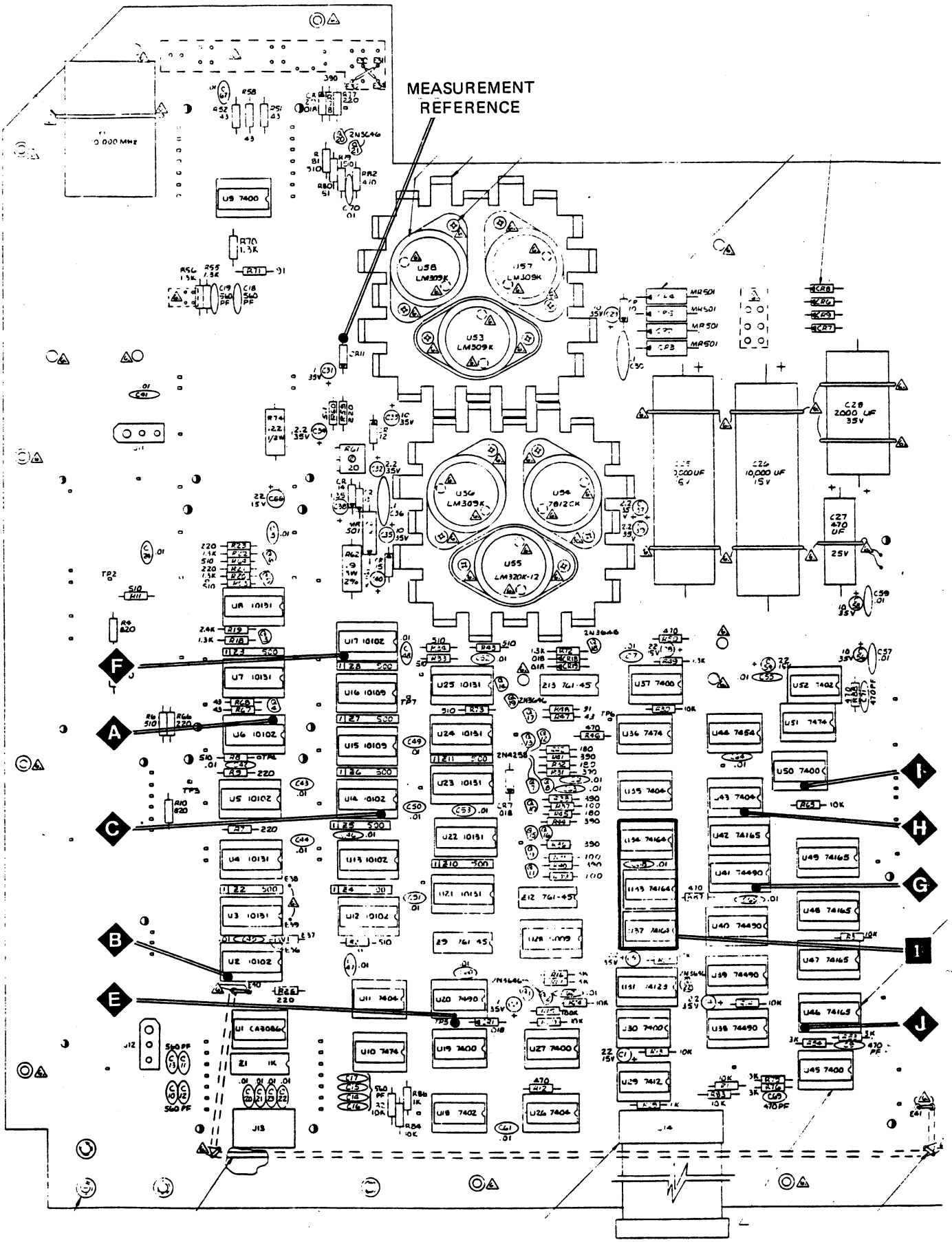
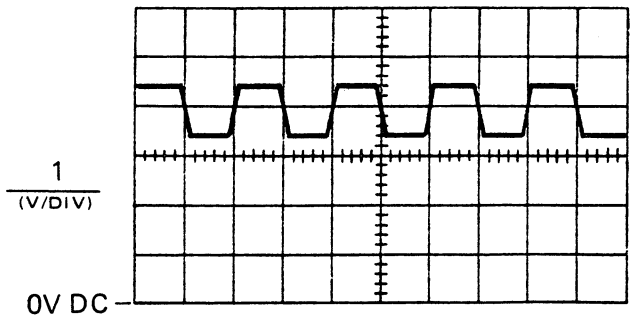


Figure 5.18 - Period (Main Logic) Unit Performance Test Points

WAVEFORMS FOR PERIOD (MAIN LOGIC)
UNIT PERFORMANCE TEST

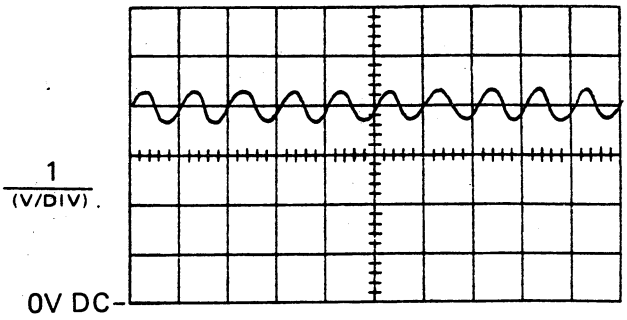
1 (NO.) U6-2
SIGNAL DETECT
FA ECL OUTPUT



.5 mSEC/DIV

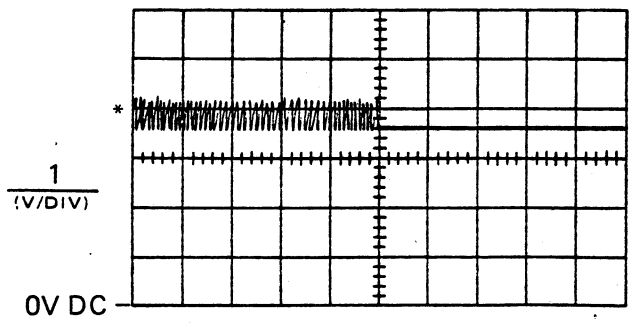
NOTE: USE INTERNAL TRIGGER

2 (NO.) U2-9
100 MHz REFERENCE



10 nSEC/DIV

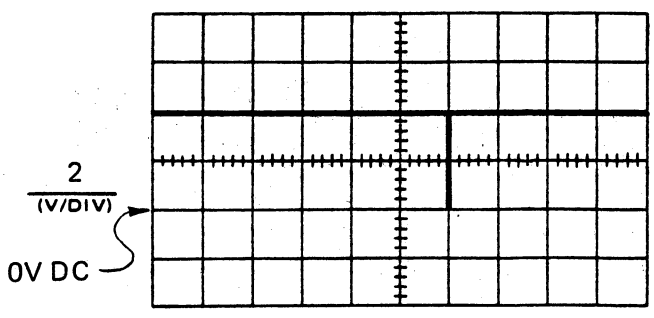
3 (NO.) U14-14
ECL COUNTER
INPUT SIGNAL



.2 mSEC/DIV

*NOTE: SIGNAL IS 100 MHz CLOCK

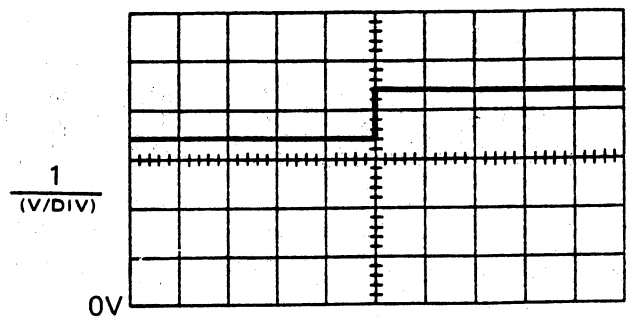
5 (NO.) TP5
$\overline{\text{CLEAR}}$



20 mSEC/DIV

TRIG ON TP7 "↑" EDGE

6 (NO.) U17-9
$\overline{\text{GATE}}$

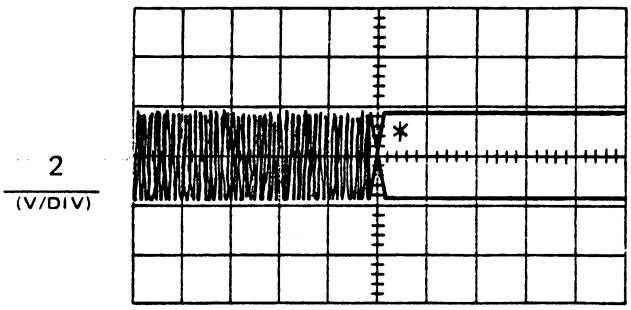


.2 mSEC/DIV

WAVEFORMS FOR PERIOD (MAIN LOGIC) UNIT PERFORMANCE TEST (Continued)

7 (NO.) U41-15

DECADE COUNTER INPUT (TTL)

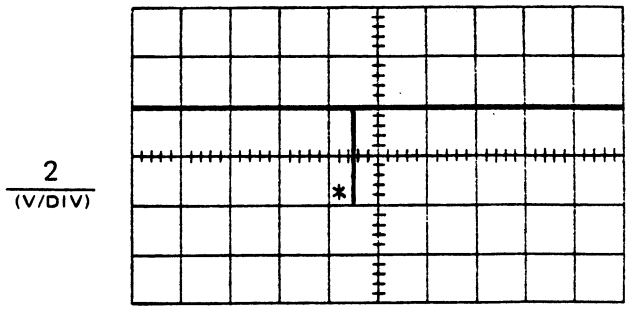


.2 mSEC/DIV

*NOTE:
SIGNAL MAY END IN EITHER HI OR LOW STATE

8 (NO.) U43-12

$\overline{\text{UPDATE}}$

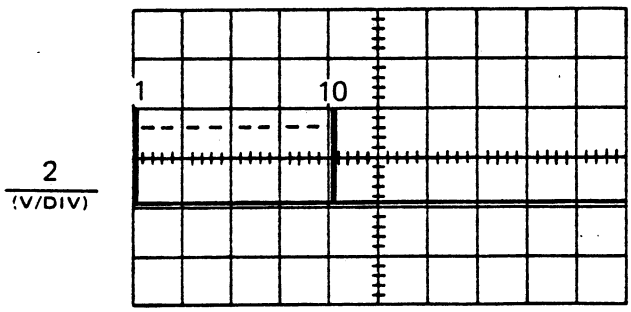


.5 mSEC/DIV

*NOTE:
APPROX PULSE POSITION WILL VARY 2 DIV

9 (NO.) U50-11

ACCUMULATOR CLOCK
(USE INTERNAL TRIG "↑" EDGE)

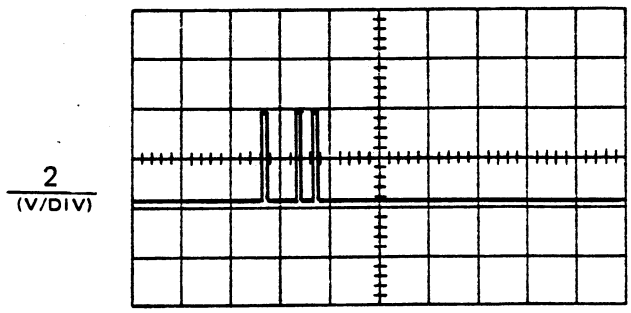


.5 MSEC/DIV

*NOTE:
SIGNAL IS 10 GROUPS OF 4 PULSES PER GROUP

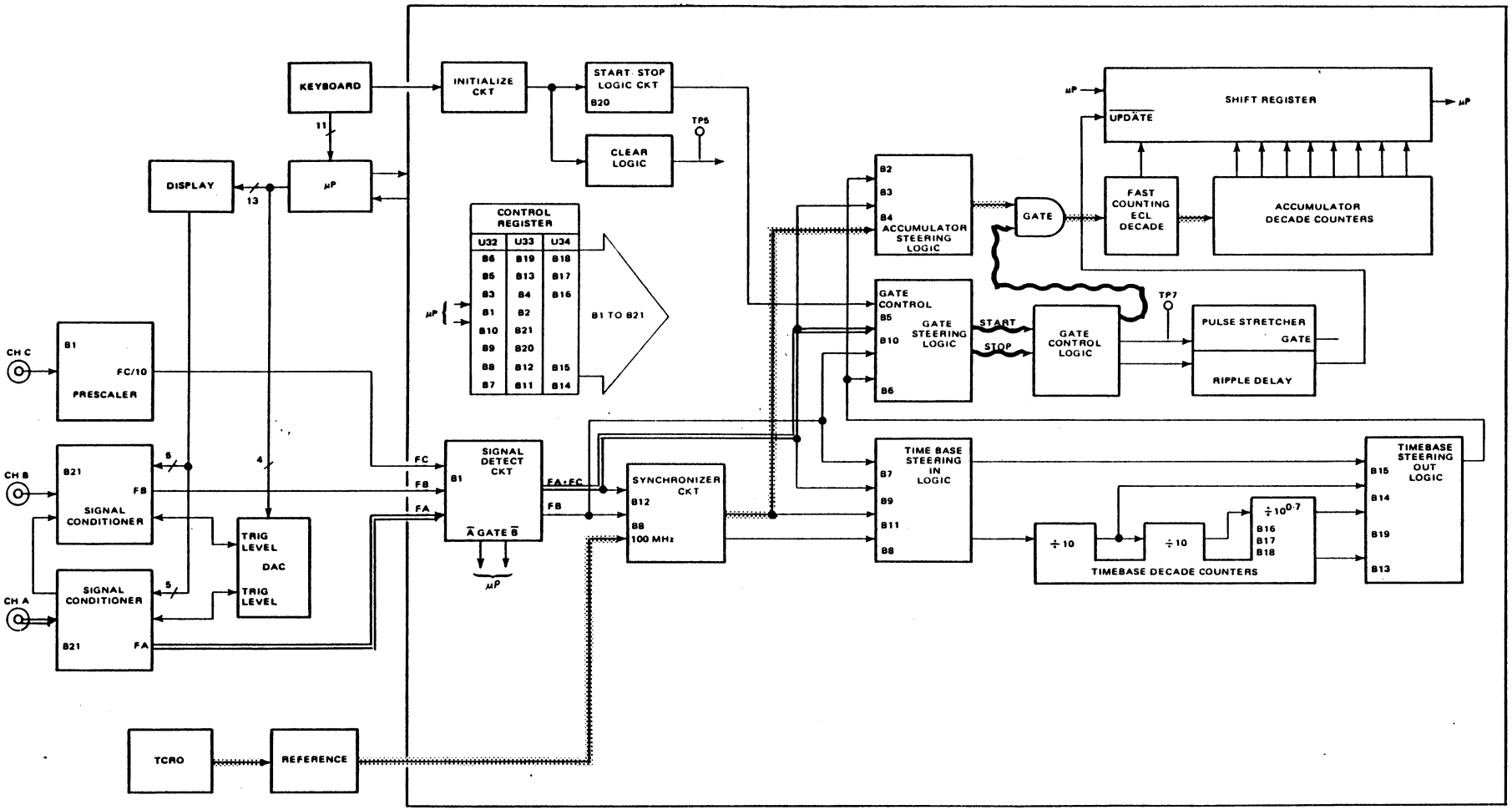
10 (NO.) U46-9

ACCUMULATOR DATA
(TRIG ON "↓" EDGE TP7)



1 mSEC/DIV

*NOTE:
APPROX WAVEFORM WILL VARY WITH INPUT SIGNAL



REFERENCE

FA

START/STOP, GATE

Figure 5.19 - Period (P) Single Thread Diagram

Table 5.12 - Time Interval (TI) Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
See preliminary unit performance test for main logic ECL supply voltage, reference PCB, and DAC PCB tests.					
See Frequency A (FA) unit performance test for Channel A signal conditioner tests.					
See Frequency A (FA) unit performance test for Channel B signal conditioning tests.					
Keyboard switches: Norm/Hold: Normal Sep/Test/Com: Com (Ch A) Slope: Coupling: DC (Ch B) Slope: Coupling: DC Keyboard: IT (initialize)					Note: Measurement reference for main logic PCB @ CR11 (Anode) Note: Scope trigger on plus edge of TP7 (Gate)
Apply A square wave input signal of 1V @ 1 KHz to Ch A (scope cal signal). Keyboard: (Ch A) TL, AU (Ch B) TL, AU					
	Main logic control register bits	U32, 33, 34 (see chart for pin locations)	1	Fig 5.20	Verify logic levels (TTL) 1 = ≥ +2.4 VDC 0 = ≤ +0.8 VDC

	TIMEBASE/MULTIPLIER CONTROL								
	(PI+TI) + 10 nSec	PA + TIA + (TI+P) 10 nSec	P + PA + TI	TIA	2^2	2^1	2^0	100 nSEC	10 nSec
HOME STATE									
FUNCT	2	4	13	19	16	17	18	14	15
TI	1	0	0	0	0	0	0	0	1
U NO.	33				34				
PIN	6	5	4	3	5	4	3	13	12

	MODE CONTROL											
	FC	P + TI + PA + TIA	$\overline{P}$	P + TI + TO	$\overline{A/B}$	$\overline{TIA}$	$\overline{PA + TO}$	$\overline{TI}$	PA + TIA + N_B + TO	FA + FC + TIA	$\overline{TO}$	$\overline{TI + TIA}$
FUNCT	1	3	5	6	7	8	9	10	11	12	20	21
TI	0	1	1	1	1	1	1	0	0	0	1	0
U NO.	32							33				
PIN	6	5	4	3	13	12	11	10	13	12	11	10

Table 5.12 - Time Interval (TI) Unit Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Signal detect FA ECL out	U6-2	A	Fig 5.20	Waveform #1
	Signal detect FB ECL out	U6-15	B	Fig 5.20	Waveform #2
	100 MHz reference	U2-9	C	Fig 5.20	Waveform #3
	ECL counter input signal	U14-14	D	Fig 5.20	Waveform #4
	$\overline{\text{CLEAR}}$	TP5	E	Fig 5.20	Waveform #5
	$\overline{\text{GATE}}$	U17-9	F	Fig 5.20	Waveform #6
	Decade counter input (TTL)	U41-15	G	Fig 5.20	Waveform #7
	$\overline{\text{UPDATE}}$	U43-12	H	Fig 5.20	Waveform #8
	Accumulator clock	U50-11	I	Fig 5.20	Waveform #9
	Accumulator data	U46-9	J	Fig 5.20	Waveform #10

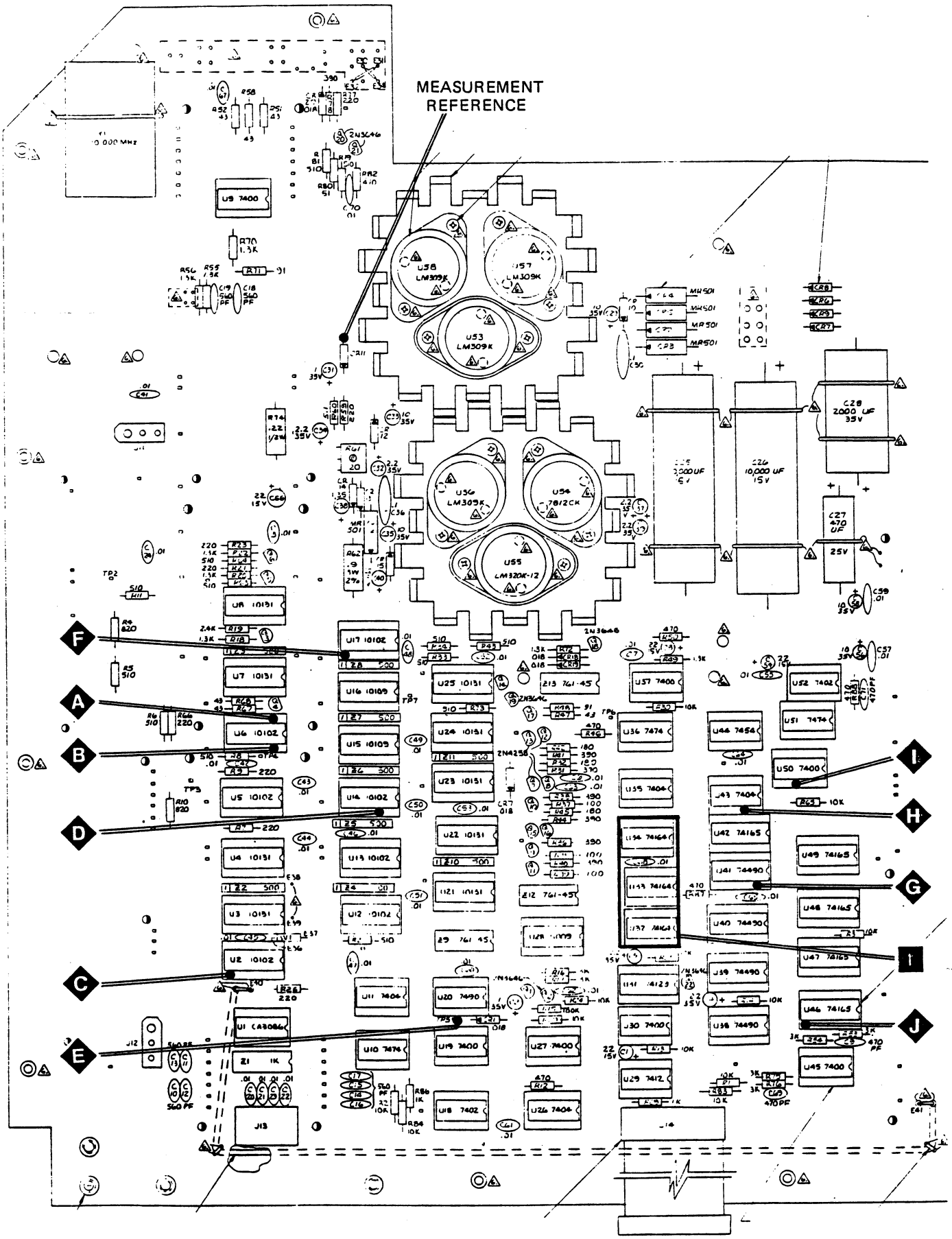
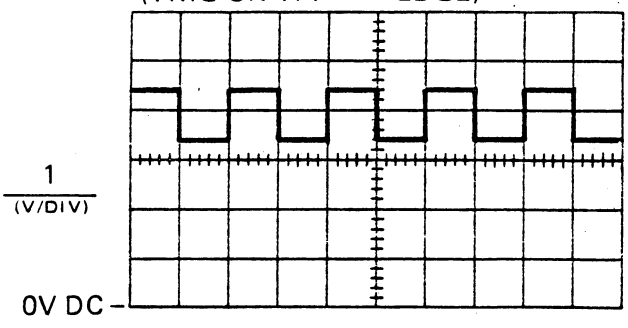


Figure 5.20 - Time Interval (Main Logic) Unit Performance Test Points

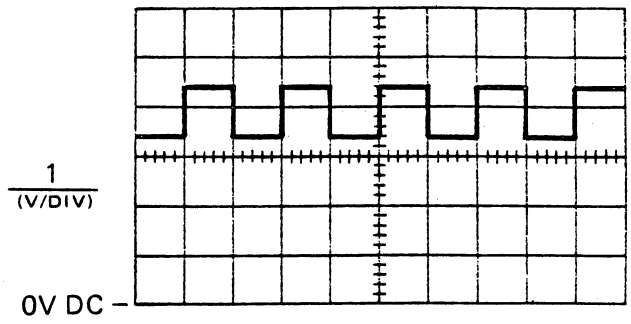
WAVEFORMS FOR TIME INTERVAL (MAIN LOGIC)
UNIT PERFORMANCE TEST

1 (NO.) U6-2
SIGNAL DETECT
FA ECL SIGNAL
(TRIG ON TP7 " " EDGE)



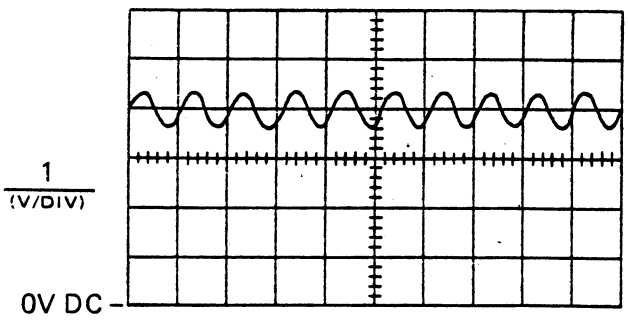
.5 mSEC/DIV

2 (NO.) U6-15
SIGNAL DETECT
FB ECL SIGNAL



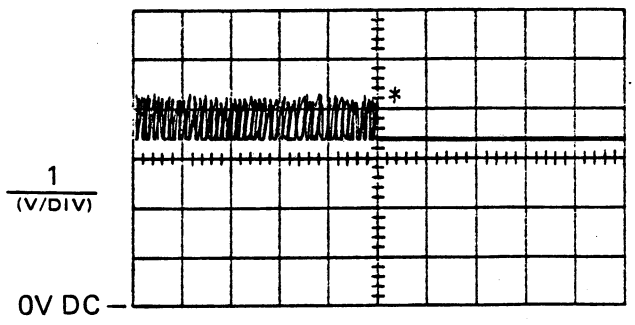
.5 mSEC/DIV

3 (NO.) U2-9
100 MHz REFERENCE



10 nSEC/DIV

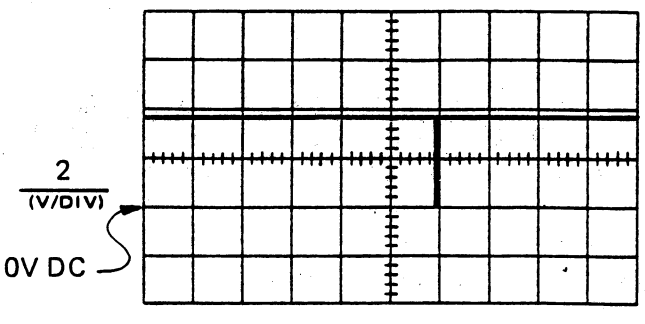
4 (NO.) U14-14
ECL COUNTER
INPUT SIGNAL



.1 mSEC/DIV

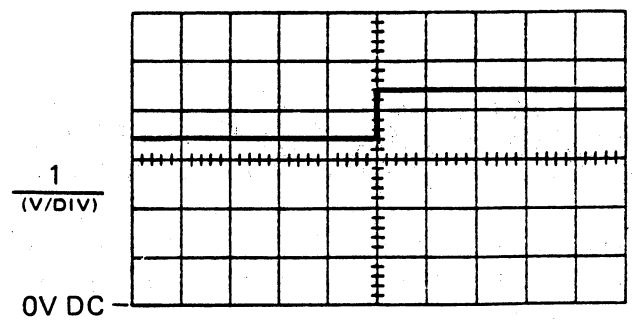
*NOTE: SIGNAL IS 100 MHz CLOCK

5 (NO.) TP5
$\overline{\text{CLEAR}}$



20 mSEC/DIV

6 (NO.) U17-9
$\overline{\text{GATE}}$

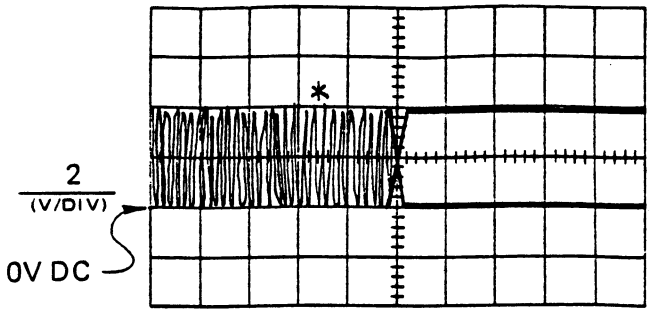


.1 mSEC/DIV

WAVEFORMS FOR TIME INTERVAL (MAIN LOGIC) UNIT PERFORMANCE TEST (Continued)

7 (NO.) U41-15

DECADE COUNTER INPUT (TTL)

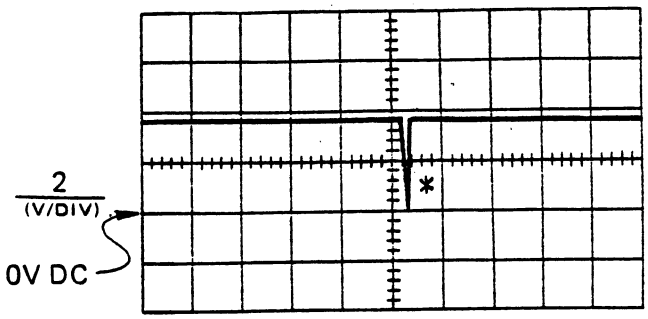


.1 mSEC/DIV

*NOTE:
100 MHz CLOCK, SIGNAL CAN END @ HI OR LOW STATE

8 (NO.) U43-12

$\overline{\text{UPDATE}}$

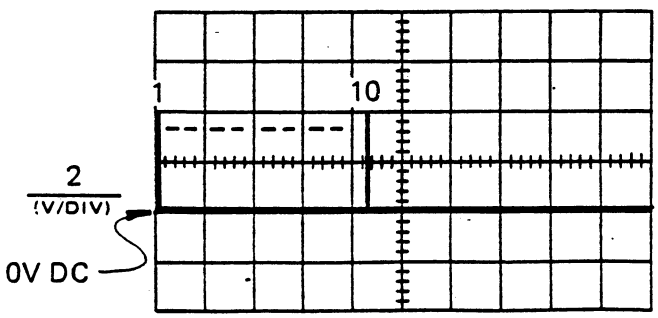


.2 mSEC/DIV

*NOTE:
PULSE POSITION WILL VARY ≈ 2 1/2 DIV

9 (NO.) U50-11

ACCUMULATOR CLOCK

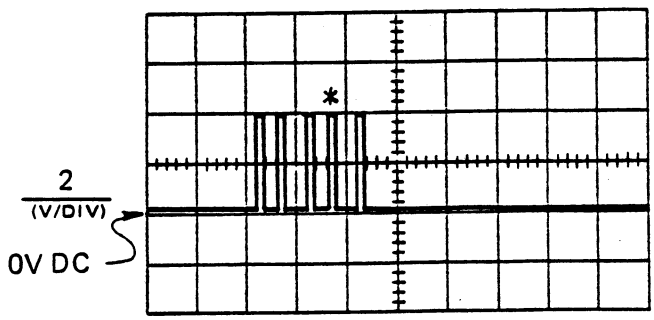


.5 mSEC/DIV

*SIGNAL IS 10 GROUPS OF 4 PULSES PER GROUP

10 (NO.) U46-9

ACCUMULATOR DATA
(TRIG ON "↓" EDGE OF TP7)



.5 mSEC/DIV

*NOTE:
APPROX SIGNAL WILL VARY WITH READING ON FRONT PANEL

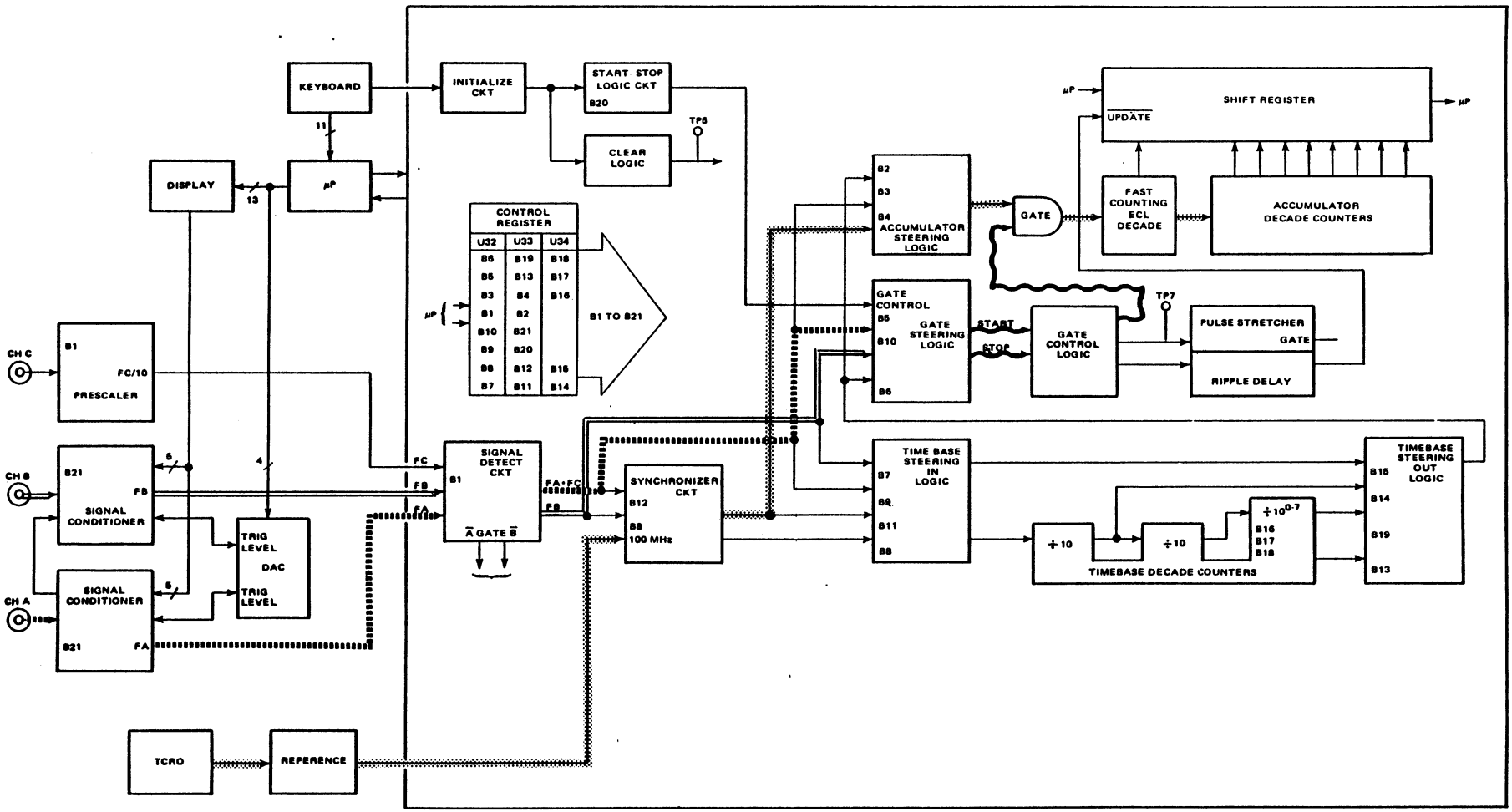


Figure 5.21 - Time Interval (TI) Single Thread Diagram

Table 5.13 - Period Average (PA) Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
See preliminary unit performance test for main logic ECL supply voltage, reference PCB, and DAC PCB tests.					
See Frequency A (FA) unit performance test for Channel A signal conditioning tests.					
Keyboard switches: Norm/Hold: Norm Sep/Test/Com: Sep (Ch A) Slope: Coupling: DC Keyboard: IT (initialize) P, AV					Note: Measurement reference for main logic PCB @ CR11 (cathode) Note: Scope trigger on plus edge of TP7 (gate)
Apply a square wave input signal of 1V @ 1 KHz to Ch A (scope cal signal). Keyboard: (Ch A) TL, AU					
	Main logic control register bits	U32, 33, 34 (see chart for pin locations)	1	Fig 5.22	Verify logic levels (TTL) 1 = ≥ +2.4 VDC 0 = ≤ +0.8 VDC

HOME STATE

	TIMEBASE/MULTIPLIER CONTROL									MODE CONTROL											
	(PI+TI) + 10 nSec	PA + TIA + (TI+P) 10 nSec	P + PA + TI	TIA	2^2	2^1	2^0	100 nSEC	10 nSec	FC	P + TI + PA + TIA	$\overline{P}$	P + TI + TO	$\overline{A/B}$	$\overline{TIA}$	$\overline{PA + TO}$	$\overline{TI}$	PA + TIA + N_β + TO	FA + FC + TIA	$\overline{TO}$	$\overline{TI + TIA}$
FUNCT	2	4	13	19	16	17	18	14	15	1	3	5	6	7	8	9	10	11	12	20	21
PA	1	0	0	0	0	0	0	1	0	0	1	1	0	1	1	0	1	1	0	1	1
U NO.	33				34					32							33				
PIN	6	5	4	3	5	4	3	13	12	6	5	4	3	13	12	11	10	13	12	11	10

Table 5.13 - Period Average (PA) Unit Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Signal detect FA ECL out	U6-2	A	Ref 5.22	Waveform #1
	100 MHz reference	U2-9	B	Ref 5.22	Waveform #2
	ECL counter input signal	U14-14	C	Ref 5.22	Waveform #3
	Time base steering out signal	U44-8	D	Ref 5.22	Waveform #4
	$\overline{\text{CLEAR}}$	TP5	E	Ref 5.22	Waveform #5
	$\overline{\text{GATE}}$	U17-9	F	Ref 5.22	Waveform #6
	Decade counter input (TTL)	U41-15	G	Ref 5.22	Waveform #7
	$\overline{\text{UPDATE}}$	U43-12	H	Ref 5.22	Waveform #8
	Accumulator clock	U50-11	I	Ref 5.22	Waveform #9
	Accumulator data	U46-9	J	Ref 5.22	Waveform #10

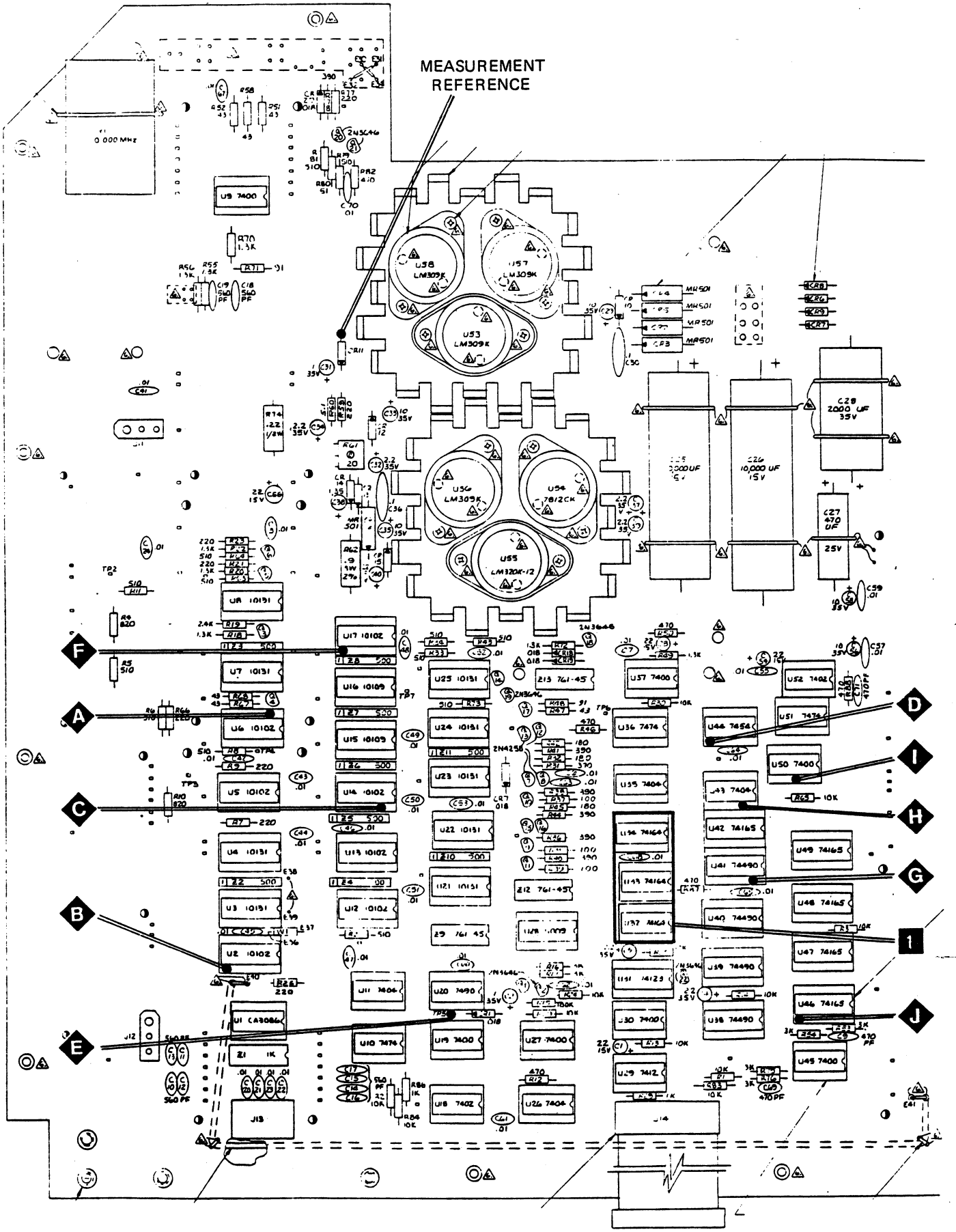
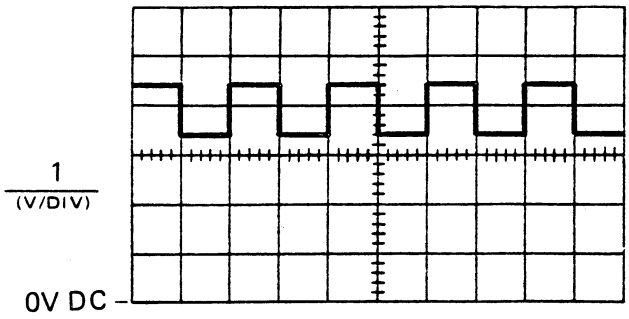


Figure 5.22 - Period Average (Main Logic) Unit Performance Test Points

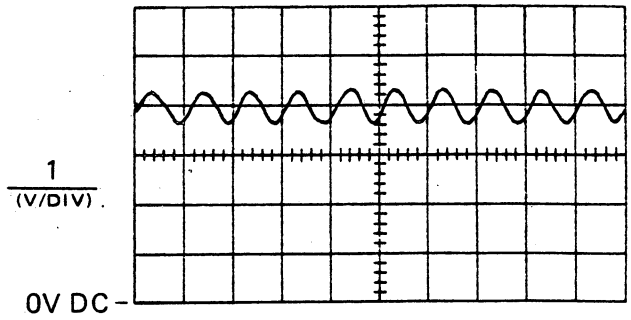
WAVEFORMS FOR PERIOD AVERAGE (MAIN LOGIC)
UNIT PERFORMANCE TEST

1 (NO.) U6-2
SIGNAL DETECT FA ECL OUT
(TRIG "↑" EDGE TP7)



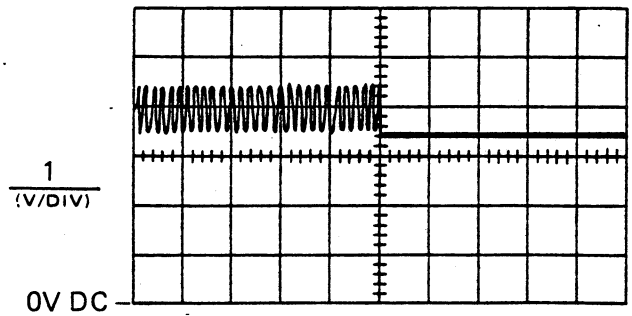
.5 mSEC/DIV

2 (NO.) U2-9
100 MHz REFERENCE



10 nSEC/DIV

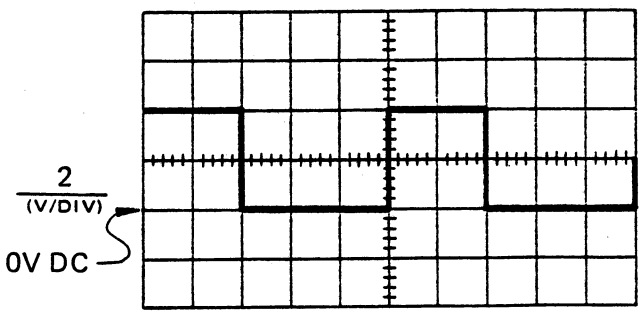
3 (NO.) U14-14
ECL COUNTER INPUT SIGNAL



2 mSEC/DIV

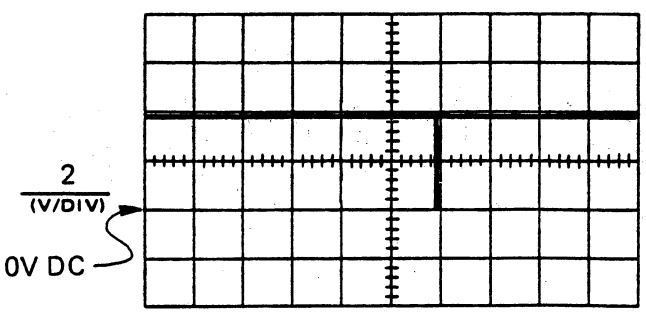
*NOTE: 100 MHz CLOCK SIGNAL

4 (NO.) U44-8
TIMEBASE STEERING OUT SIGNAL



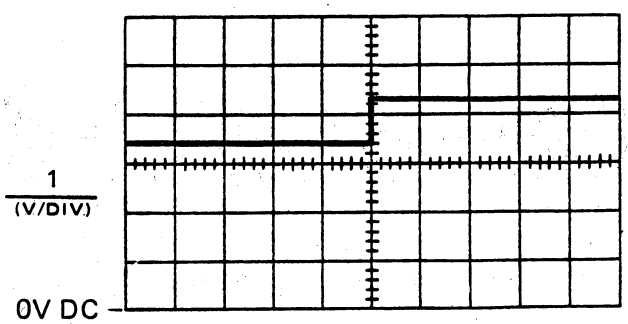
2 mSEC/DIV

5 (NO.) TP5
$\overline{\text{CLEAR}}$



20 mSEC/DIV

6 (NO.) U17-9
$\overline{\text{GATE}}$

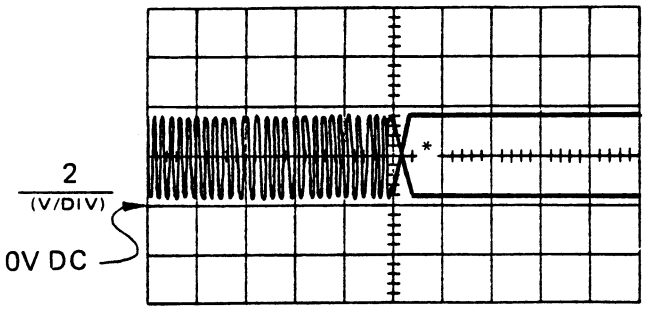


2 mSEC/DIV

WAVEFORMS FOR PERIOD AVERAGE (MAIN LOGIC) UNIT PERFORMANCE TEST (Continued)

7 (NO.) U41-15

DECADE COUNTER INPUT (TTL)

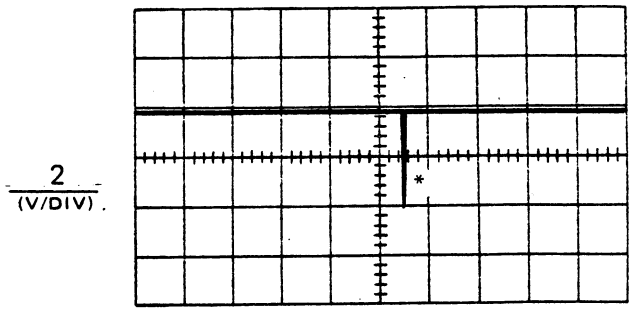


2 mSEC/DIV

*NOTE: SIGNAL MAY END IN HI OR LOW STATE

8 (NO.) U43-12

UPDATE



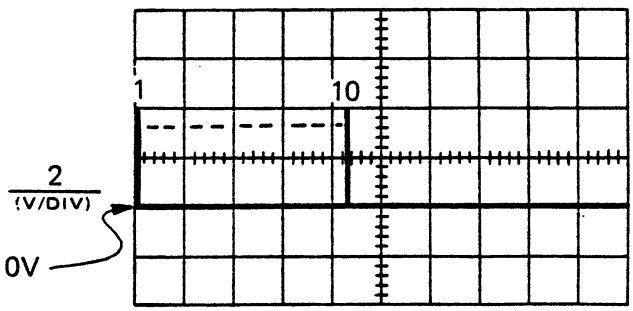
.2 mSEC/DIV

*NOTE: PULSE POSITION MAY VARY 3 DIV

9 (NO.) U50-11

ACCUMULATOR CLOCK

(USE "↑" EDGE OF INTERVAL TRIGGER)



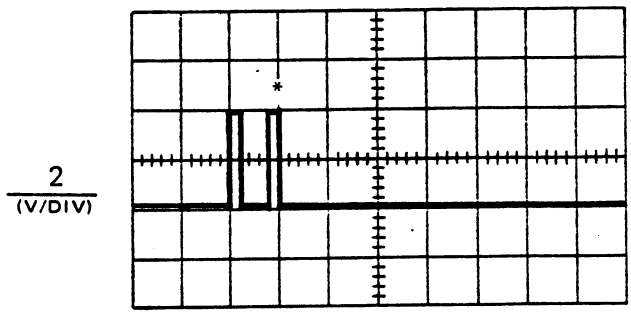
.5 mSEC/DIV

SIGNAL IS 10 GROUPS OF PULSES, 4 PULSES PER GROUP

10 (NO.) U46-9

ACCUMULATOR DATA

(TRIG ON "↑" EDGE TP7)



*NOTE: .5 mSEC/DIV

APPROX WAVEFORM SIGNAL WILL VARY WITH INPUT

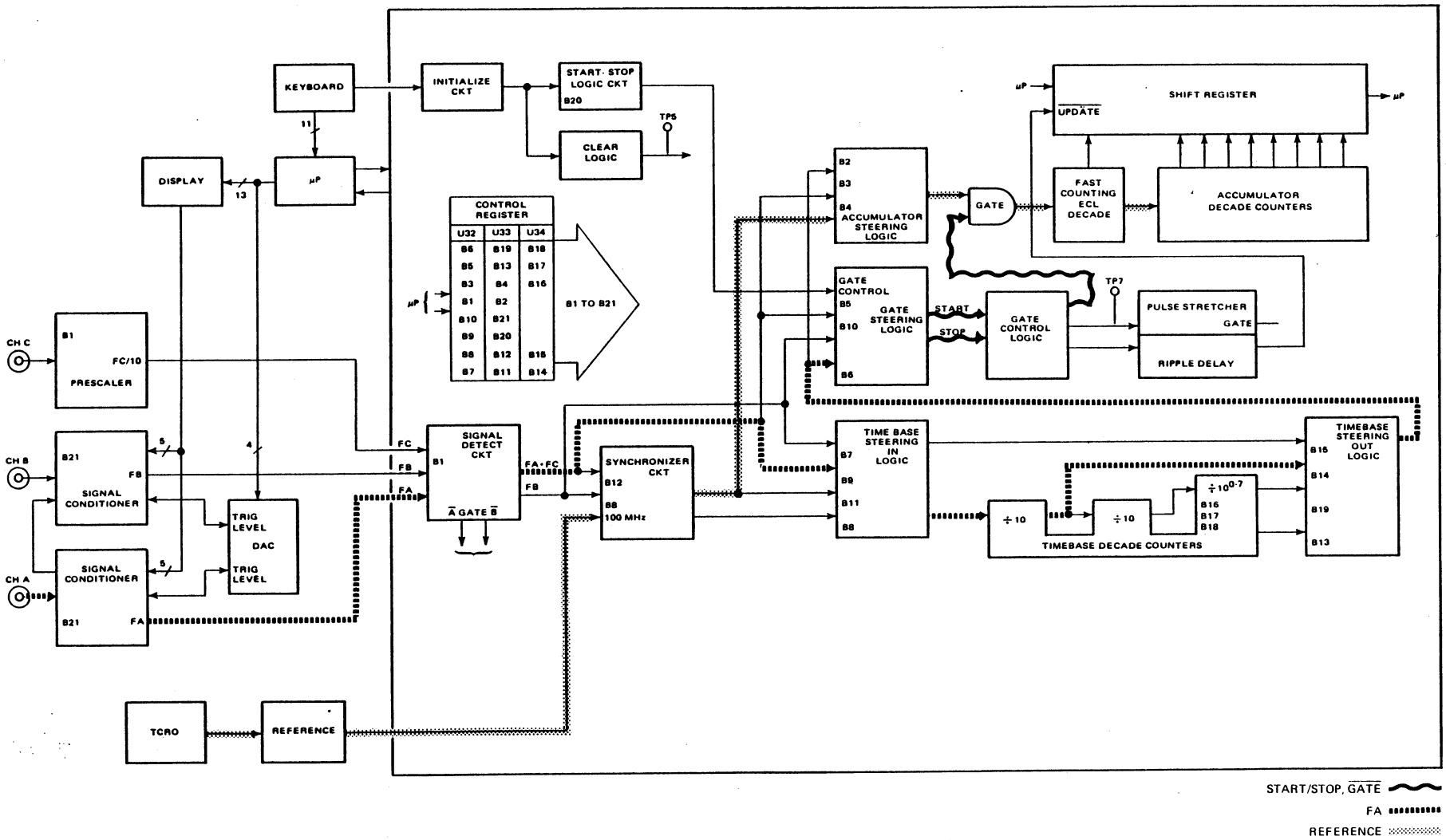


Figure 5.23 - Period Average (PA) Single Thread Diagram

Table 5.14 - Time Interval Average (TIA) Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
See preliminary unit performance test for main logic ECL supply voltage, reference PCB, and DAC PCB tests.					
See Frequency A (FA) unit performance test for Channel A and Channel B signal conditioning tests.					
Keyboard switches: Norm/Hold: Norm Sep/Test/Com: Com (Ch A) Slope: Coupling: DC (Ch B) Slope: Coupling: DC Keyboard: IT (initialize) AV					Note: Measurement reference for main logic PCB @ CR11 (Anode) Note: Scope trigger on plus edge of TP7 (Gate)
Apply a square wave input signal of 1V @ 1 KHz to Ch A (scope cal signal). Keyboard: (Ch A) TL, AU (Ch B) TL, AU					
	Main logic control register bits	U32, 33, 34 (see chart for pin locations)	1	Fig 5.24	Verify logic levels (TTL) 1 = ≥ +2.4 VDC 0 = ≤ +0.8 VDC

HOME STATE		TIMEBASE/MULTIPLIER CONTROL									MODE CONTROL											
		(PI+TI) + 10 nSec	PA + TIA + (TI+P) 10 nSec	P + PA + TI	TIA	2^2	2^1	2^0	100 nSEC	10 nSec	FC	P + TI + PA + TIA	$\overline{P}$	P + TI + TO	$\overline{A/B}$	$\overline{TIA}$	$\overline{PA + TO}$	$\overline{TI}$	PA + TIA + N_β + TO	FA + FC + TIA	$\overline{TO}$	$\overline{TI + TIA}$
	FUNCT	2	4	13	19	16	17	18	14	15	1	3	5	6	7	8	9	10	11	12	20	21
	TIA	1	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	1	1	1	1	0
	U NO.	33				34					32							33				
	PIN	6	5	4	3	5	4	3	13	12	6	5	4	3	13	12	11	10	13	12	11	10

Table 5.14 - Time Interval Average (TIA) Unit Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Signal detect FA ECL out	U6-2	A	Fig 5.24	Waveform #1
	Signal detect FB ECL out	U6-15	B	Fig 5.24	Waveform #2
	$\overline{\text{CLEAR}}$	TP5	C	Fig 5.24	Waveform #3
	Synchronizer output	U12-2	D	Fig 5.24	Waveform #4
	Timebase counter input	U15-3	E	Fig 5.24	Waveform #5
	Timebase steering out signal	U44-8	F	Fig 5.24	Waveform #6
	$\overline{\text{GATE}}$	U17-9	G	Fig 5.24	Waveform #7
	ECL counter input	U14-14	H	Fig 5.24	Waveform #8
	Decade counter input (TTL)	U41-15	I	Fig 5.24	Waveform #9
	$\overline{\text{UPDATE}}$	U43-12	J	Fig 5.24	Waveform #10
	Accumulator clock	U50-11	K	Fig 5.24	Waveform #11
	Accumulator data	U46-9	L	Fig 5.24	Waveform #12

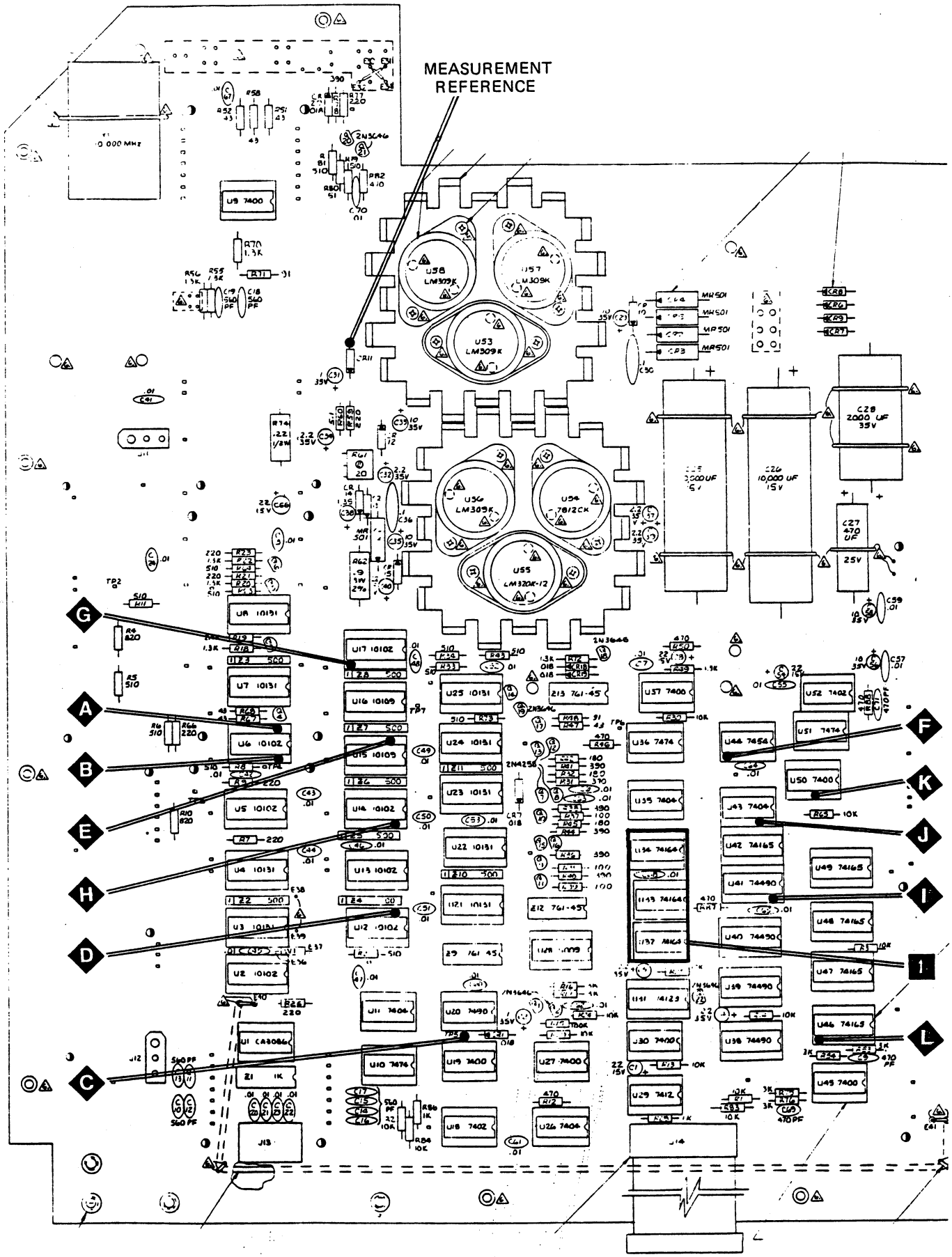
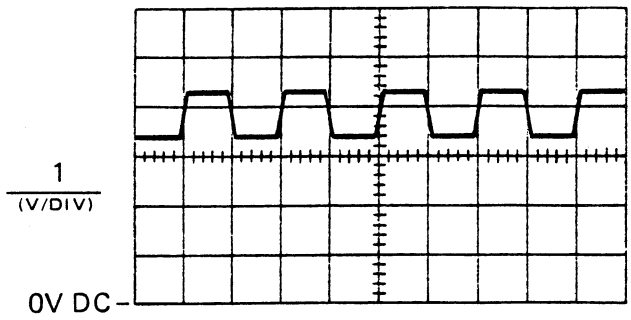


Figure 5.24 - Time Interval Average (Main Logic) Unit Performance Test Points

WAVEFORMS FOR TIME INTERVAL AVERAGE (MAIN LOGIC)
UNIT PERFORMANCE TEST

1 (NO.) U6-2

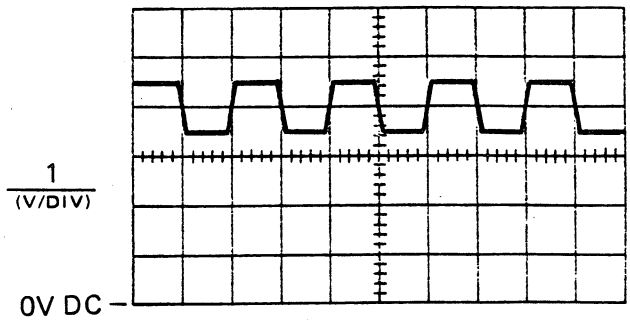
SIGNAL DETECT FA ECL OUT



.5 mSEC/DIV

2 (NO.) U6-15

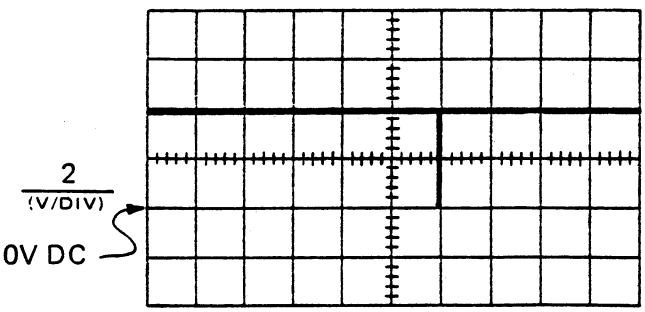
SIGNAL DETECT FB ECL OUT



.5 mSEC/DIV

3 (NO.) TP5

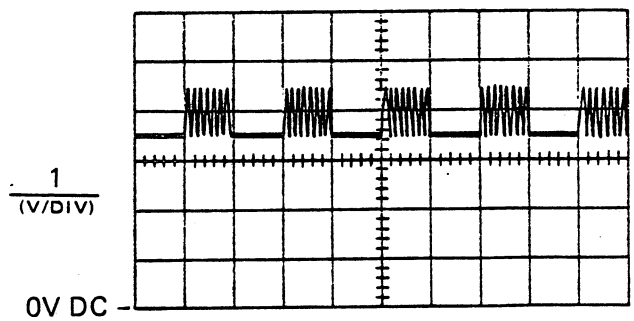
$\overline{\text{CLEAR}}$



50 mSEC/DIV

4 (NO.) U12-2

SYNCHRONIZER OUTPUT

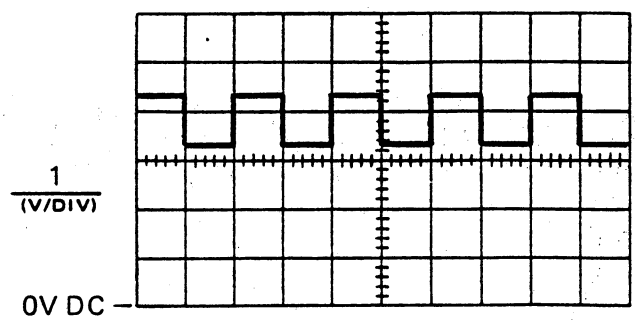


.5 mSEC/DIV

*NOTE: SIGNAL IS 100 MHz CLOCK

5 (NO.) U15-3

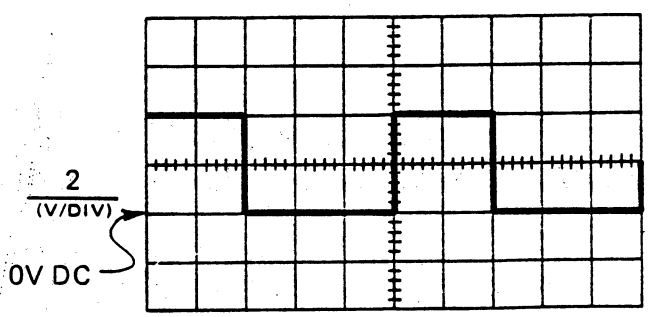
TIMEBASE COUNTER INPUT



.5 mSEC/DIV

6 (NO.) U44-8

TIMEBASE STEERING OUT SIGNAL

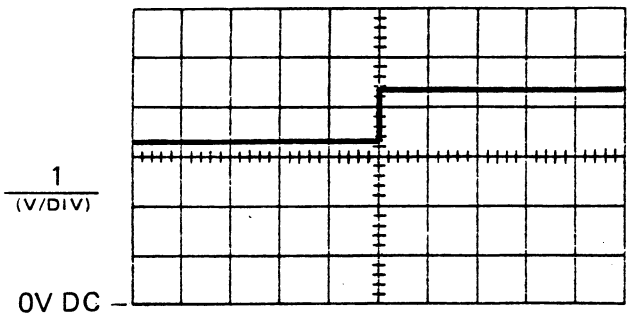


2 mSEC/DIV

WAVEFORMS FOR TIME INTERVAL AVERAGE (MAIN LOGIC) UNIT PERFORMANCE TEST (Continued)

7 (NO.) U17-9

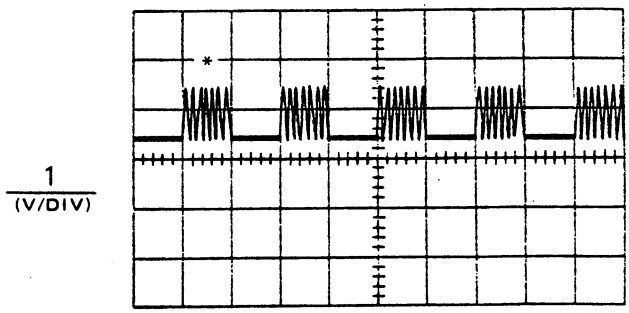
GATE



2 mSEC/DIV

8 (NO.) U14-14

ECL COUNTER INPUT

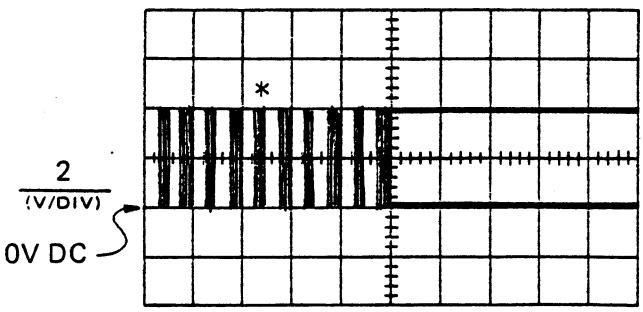


.5 mSEC/DIV

*NOTE: SIGNAL IS 100 MHz

9 (NO.) U41-15

DECADE COUNTER INPUT (TTL)

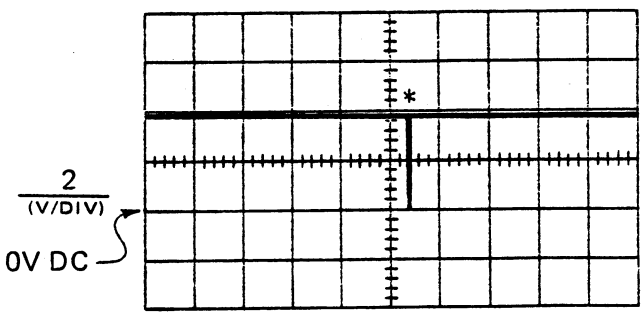


2 mSEC/DIV

*NOTE:
APPROX WAVEFORM SIGNAL WILL VARY WITH INPUT

10 (NO.) U43-12

$\overline{\text{UPDATE}}$

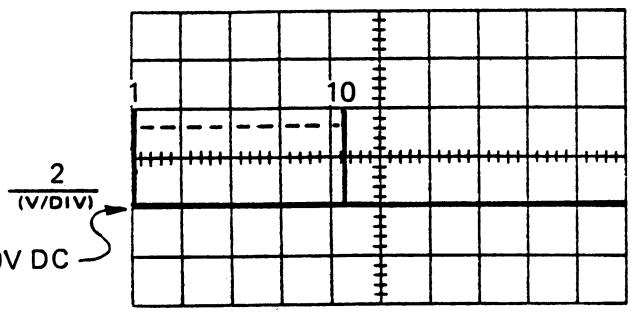


2 mSEC/DIV

*NOTE:
APPROX PULSE POSITION WILL VARY ≈ 1 DIV

11 (NO.) U50-11

ACCUMULATOR CLOCK
(TRIG ON "↑" EDGE INTERVAL TRIG)

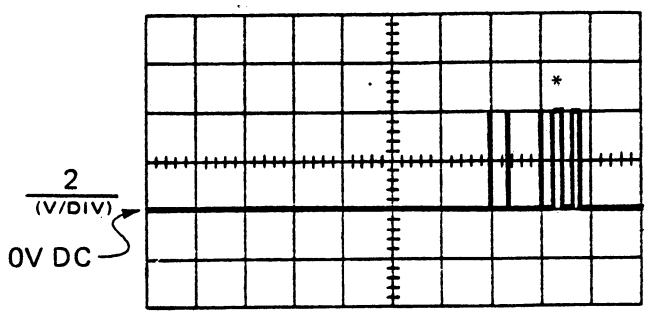


.5 mSEC/DIV

SIGNAL IS 10 GROUPS OF PULSES, 4 PULSES PER GROUP

12 (NO.) U46-9

ACCUMULATOR DATA



2 mSEC/DIV

*NOTE:
APPROX WAVEFORM SIGNAL WILL VARY WITH INPUT

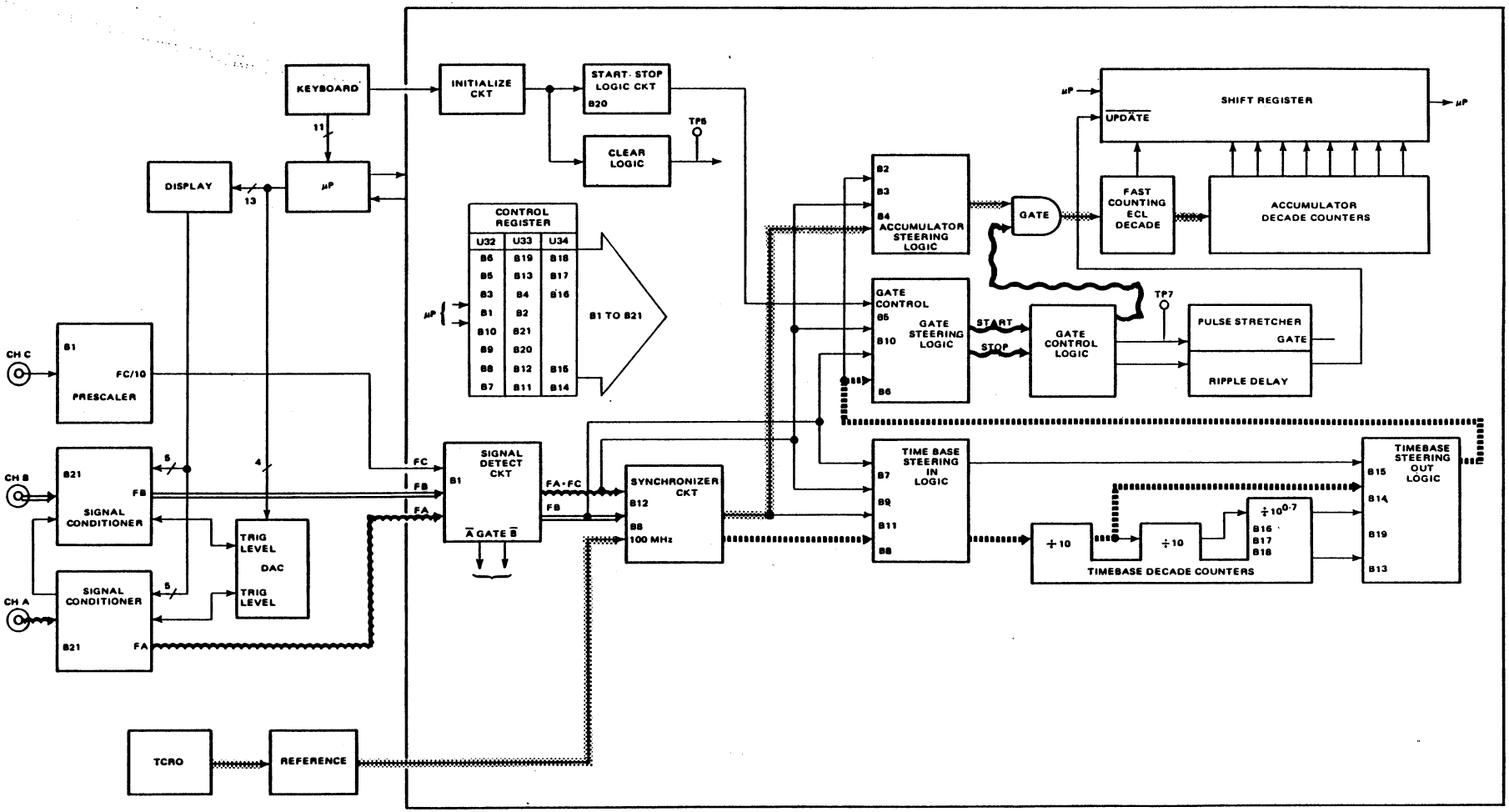


Figure 5.25 - Time Interval Average (TIA) Single Thread Diagram

Table 5.15 - Ratio (A/B) Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
See preliminary unit performance test for main logic ECL supply voltage, reference PCB, and DAC PCB tests.					
See Frequency A (FA) unit performance test for Channel A and Channel B signal conditioning tests.					
Keyboard switches: Norm/Hold: Norm Sep/Test/Com: Com (Ch A) Slope: or Coupling: DC (Ch B) Slope: or Coupling: DC Keyboard: IT (initialize) RA					Note: Measurement reference for main logic PCB @ CR11 (Anode) Note: Scope trigger on plus edge of TP7 (Gate)
Apply a square wave input signal of 1V @ 1 KHz to Ch A (scope cal signal) Keyboard: (Ch A) TL, AU (Ch B) TL, AU					
	Main logic control register bits	U32, 33, 34 (see chart for pin locations	1	Fig 5.26	Verify logic levels (TTL) 1 = ≥ +2.4 VDC 0 = ≤ +0.8 VDC

		TIMEBASE/MULTIPLIER CONTROL									MODE CONTROL												
		(P1+T1) + 10 nSec	PA + T1A + (T1+P) 10 nSec	P + PA + T1	T1A	2^2	2^1	2^0	100 nSEC	10 nSec	FC	P + T1 + PA + T1A	$\overline{P}$	P + T1 + TO	$\overline{A/B}$	$\overline{T1A}$	$\overline{PA + TO}$	$\overline{T1}$	PA + T1A + N_B + TO	FA + FC + T1A	$\overline{TO}$	$\overline{T1 + T1A}$
HOME STATE	FUNCT	2	4	13	19	16	17	18	14	15	1	3	5	6	7	8	9	10	11	12	20	21
	A/B	1	1	0	0	0	0	0	1	0	0	0	1	0	0	1	1	1	1	0	1	1
	U NO.	33				34					32							33				
	PIN	6	5	4	3	5	4	3	13	12	6	5	4	3	13	12	11	10	13	12	11	10

Table 5.15 - Ratio (A/B) Unit Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Signal detect FA ECL out	U6-2	A	Fig 5.26	Waveform #1
	Signal detect FB ECL out	U6-15	B	Fig 5.26	Waveform #2
	$\overline{\text{CLEAR}}$	TP5	C	Fig 5.26	Waveform #3
	Timebase steering out signal	U44-8	D	Fig 5.26	Waveform #4
	$\overline{\text{GATE}}$	U17-9	E	Fig 5.26	Waveform #5
	Decade counter input (TTL)	U41-15	F	Fig 5.26	Waveform #6
	$\overline{\text{UPDATE}}$	U43-12	G	Fig 5.26	Waveform #7
	Accumulator clock	U50-11	H	Fig 5.26	Waveform #8
	Accumulator data	U46-9	I	Fig 5.26	Waveform #9

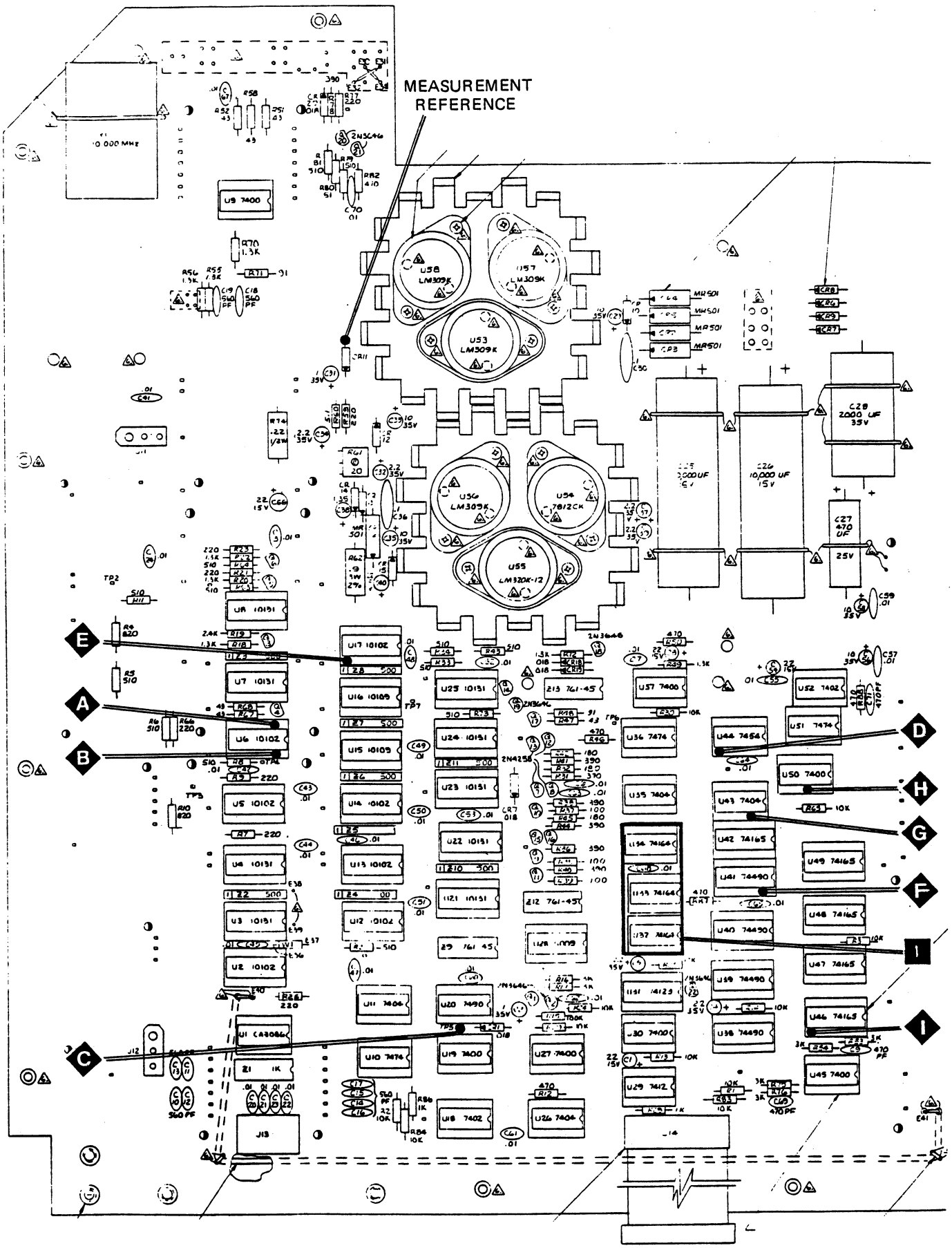
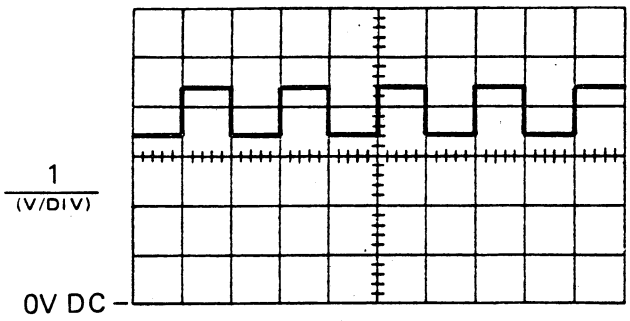


Figure 5.26 - Ratio (Main Logic) Unit Performance Test Points

WAVEFORMS FOR RATIO (MAIN LOGIC)
UNIT PERFORMANCE TEST

1 (NO.) U6-2

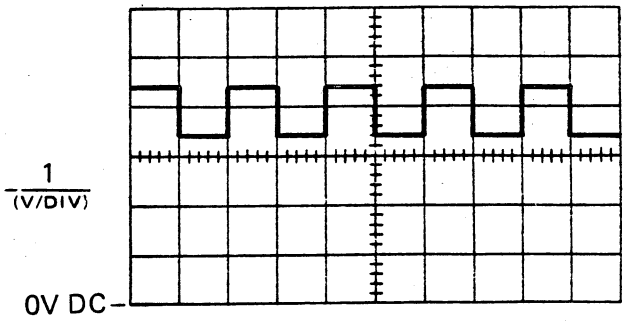
SIGNAL DETECT FA ECL OUT



.5 mSEC/DIV

2 (NO.) U6-15

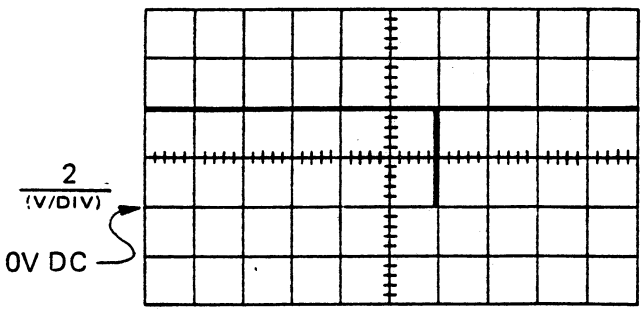
SIGNAL DETECT FB ECL OUT



.5 mSEC/DIV

3 (NO.) TP5

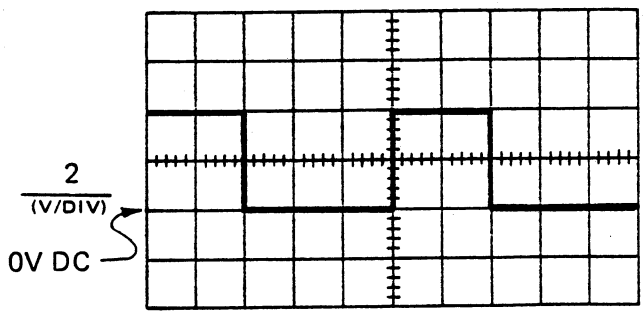
$\overline{\text{CLEAR}}$



50 mSEC/DIV

4 (NO.) U44-8

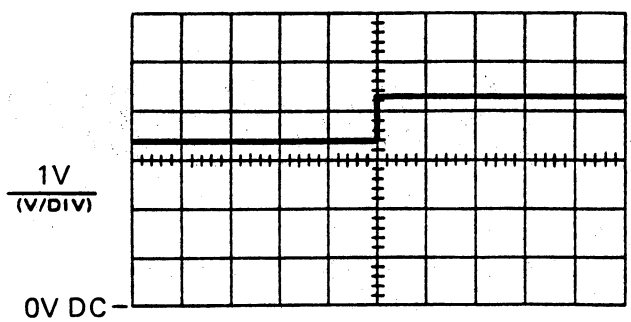
TIMEBASE STEERING OUT SIGNAL



2 mSEC/DIV

5 (NO.) U17-9

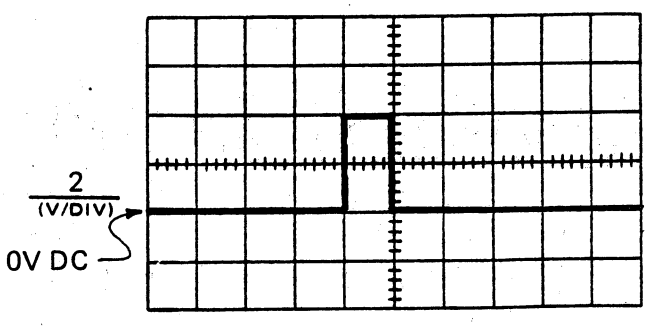
$\overline{\text{GATE}}$



2 mSEC/DIV

6 (NO.) U41-15

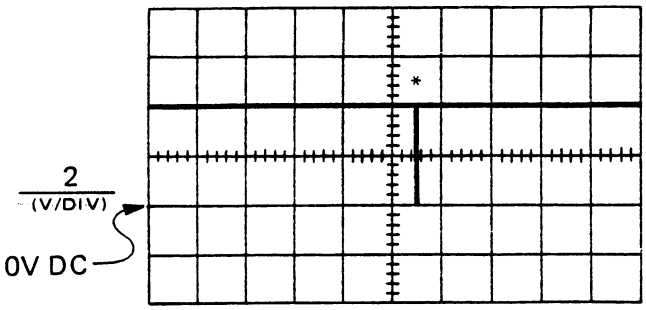
DECADE COUNTER INPUT (TTL)



2 mSEC

WAVEFORMS FOR RATIO (MAIN LOGIC) UNIT PERFORMANCE TEST (Continued)

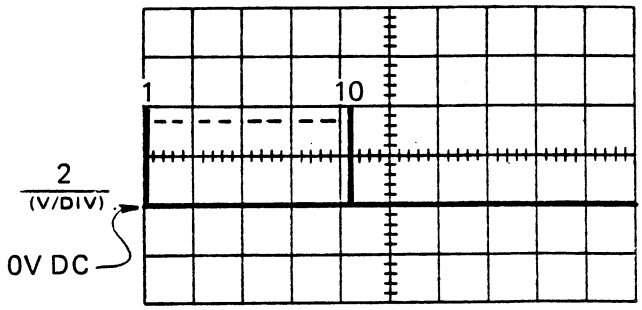
7 (NO.) U43-12 $\overline{\text{UPDATE}}$



2 mSEC/DIV

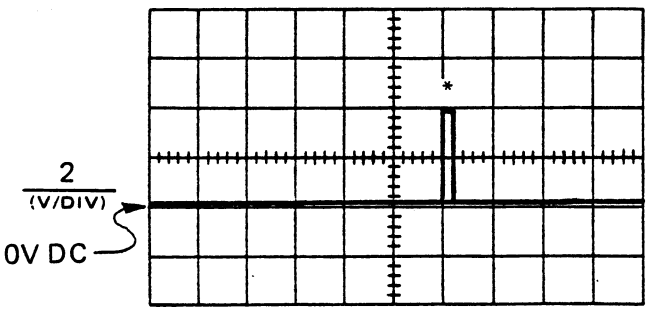
*NOTE: PULSE POSITION WILL VARY ≈ 1 DIV

8 (NO.) U50-11
ACCUMULATOR CLOCK
(TRIG ON INTERNAL)



.5 mSEC/DIV

9 (NO.) U46-9
ACCUMULATOR DATA



2 mSEC/DIV

*NOTE: PULSE POSITION WILL VARY ≈ 1 DIV

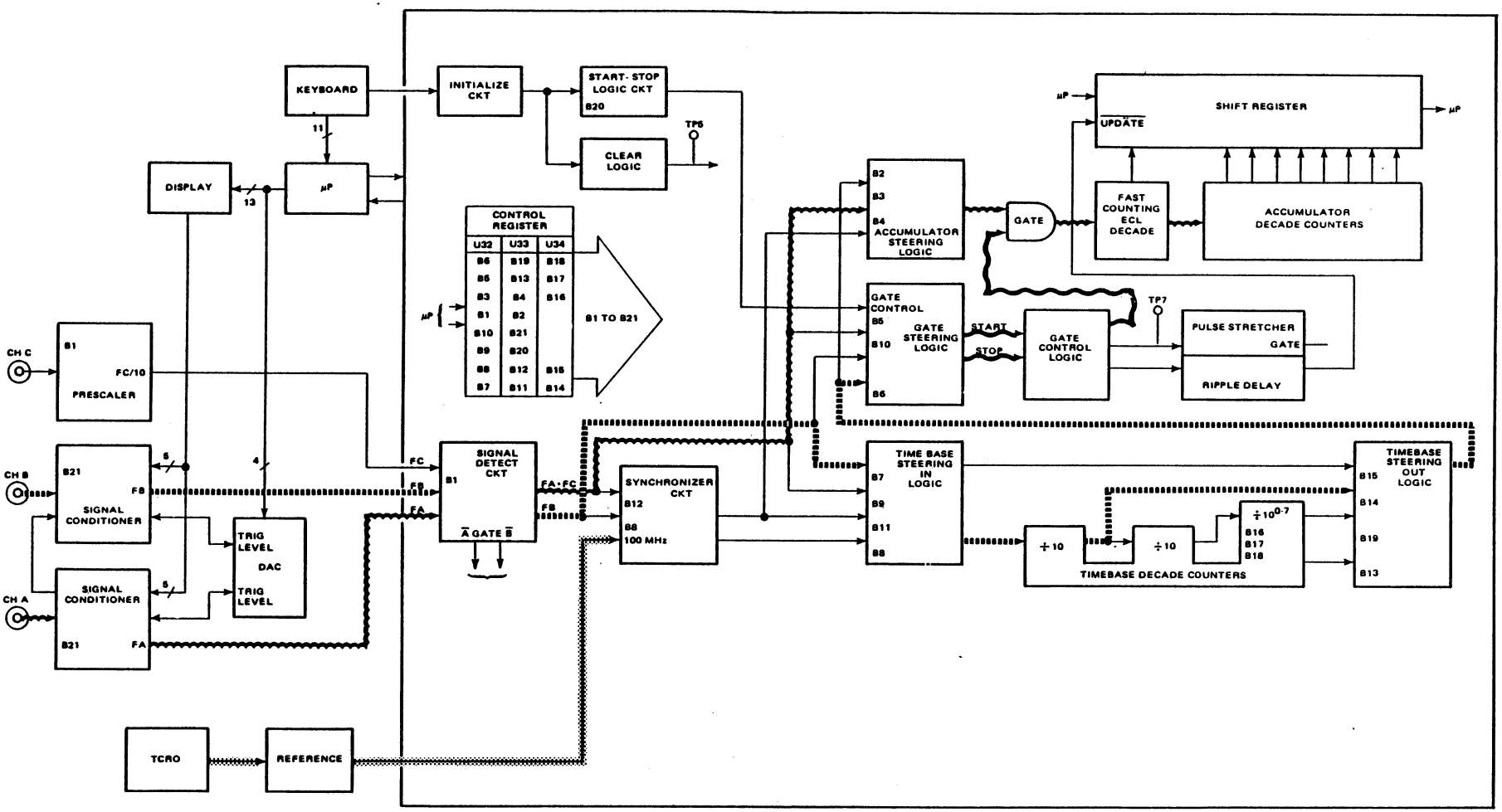


Figure 5.27 - Ratio (A/B) Single Thread Diagram

Table 5.16 - Totalize (TO) Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
See preliminary unit performance test for main logic ECL supply voltage, reference PCB, and DAC PCB tests.					
See Frequency A (FA) unit performance test for Channel A signal conditioning tests.					
Keyboard switches: Norm/Hold: Norm Sep/Test/Com: Sep (Ch A) Slope: ↑ Coupling: DC Keyboard: IT (initialize) TO					Note: Measurement reference for main logic PCB @ CR11 (Anode)
Apply a square wave input signal of 1V @ 1 KHz to Ch A (scope cal signal) Keyboard: (Ch A) TL, AU					
	Main logic control register bits	U32, 33, 34 (see chart for pin locations)	1	Fig 5.27	Verify logic levels (TTL) 1 = ≥ +2.4 VDC 0 = ≤ +0.8 VDC

HOME STATE		TIMEBASE/MULTIPLIER CONTROL									MODE CONTROL											
		(P1+T1) + 10 nSec	PA + T1A + (T1+P) 10 nSec	P + PA + T1	T1A	2^2	2^1	2^0	100 nSEC	10 nSec	FC	P + T1 + PA + T1A	$\overline{P}$	P + T1 + TO	$\overline{A/B}$	$\overline{T1A}$	$\overline{PA + TO}$	$\overline{T1}$	PA + T1A + N_B + TO	FA + FC + T1A	$\overline{TO}$	$\overline{T1 + T1A}$
	FUNCT	2	4	13	19	16	17	18	14	15	1	3	5	6	7	8	9	10	11	12	20	21
	TO	1	1	0	0	0	0	0	0	1	0	0	1	1	1	1	0	1	1	0	0	1
	U NO.	33				34					32							33				
	PIN	6	5	4	3	5	4	3	13	12	6	5	4	3	13	12	11	10	13	12	11	10

Table 5.16 - Totalize (TO) Unit Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Signal detect FA ECL out	U6-2	A	Fig 5.27	Waveform #1
	Time base counter input	U15-3	B	Fig 5.27	Waveform #2
	Time base steering out - scaled out	U9-6	C	Fig 5.27	Waveform #3
Keyboard: SS (Start Gate) SS (Stop Gate) Note: Each SS (keyboard) operation opens/closes the gate, admitting counts to the ECL and decade counters. Display accumulates total counts.	Gate control	U18-13	D	Fig 5.27	Waveform #4
	$\overline{\text{GATE}}$	U17-9	E	Fig 5.27	Waveform #5
	Decade counter input (TTL)	U41-15	F	Fig 5.27	Waveform #
	$\overline{\text{UPDATE}}$	U43-12	G	Fig 5.27	Waveform #
	Accumulator clock	U50-11	H	Fig 5.27	Waveform #
	Accumulator data	U46-9	I	Fig 5.27	Waveform #
Keyboard: RS (Reset) Note: Reset clears display of accumulated counts	$\overline{\text{CLEAR}}$	TP5	J	Fig 5.27	Waveform #

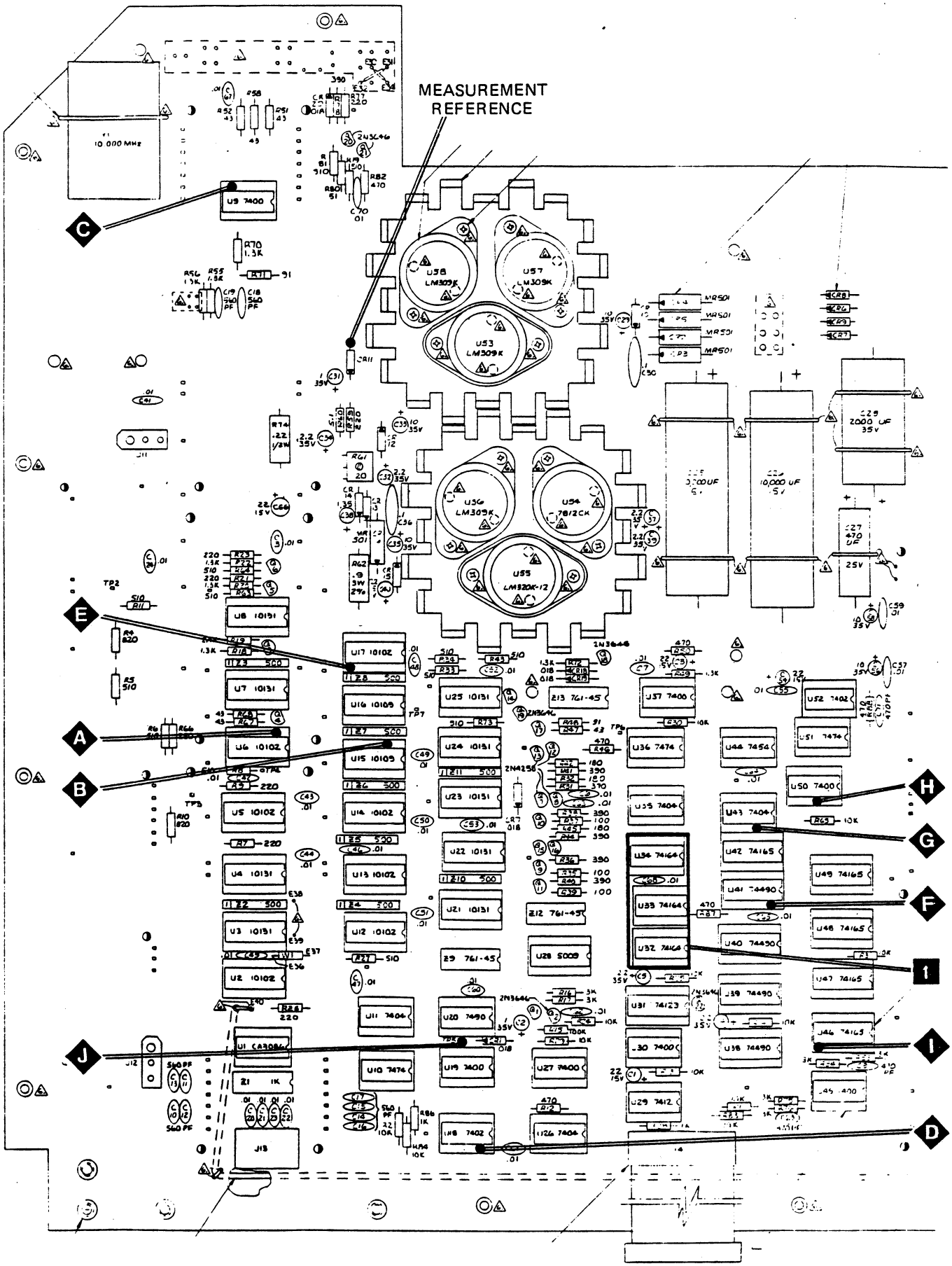
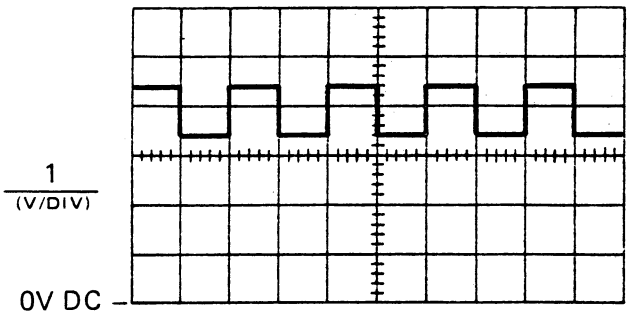


Figure 5.28 - Totalize (Main Logic) Unit Performance Test Points

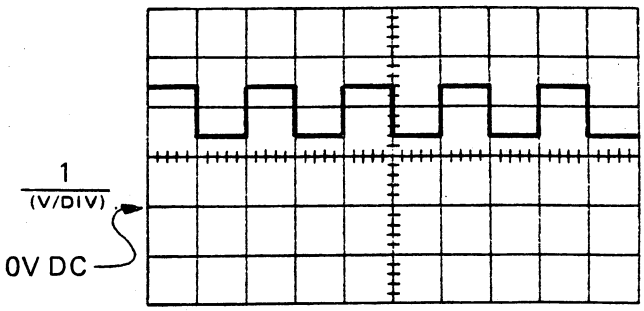
WAVEFORMS FOR TOTALIZE (MAIN LOGIC) UNIT PERFORMANCE TEST

1 (NO.) U6-2
SIGNAL DETECT FA ECL OUT
(USE INTERNAL TRIGGER)



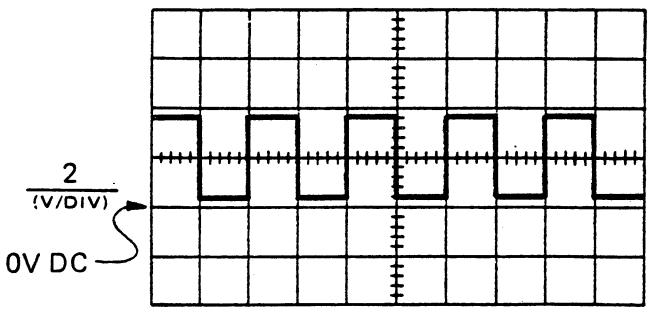
.5 mSEC/DIV

2 (NO.) U15-3
TIMEBASE COUNTER INPUT



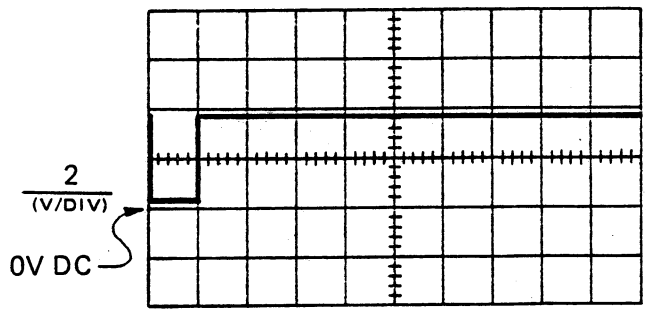
.5 mSEC/DIV

3 (NO.) U9-6
TIMEBASE STEERING OUT –
SCALED OUT



.5 mSEC/DIV

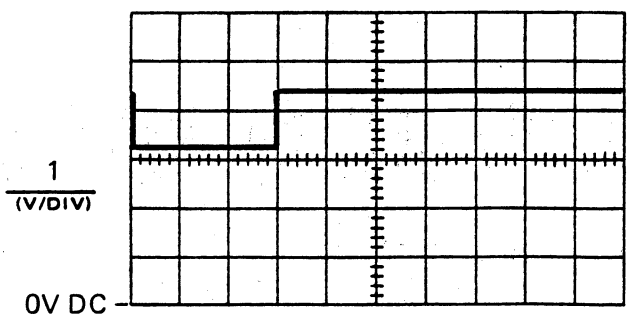
4 (NO.) U18-13 $\overline{\text{GATE CONTROL}}$
(TRIG ON "↓" EDGE USING DC
COUPLED INTERNAL TRIG)



20 mSEC/DIV

*NOTE:
SIGNAL IS GENERATED BY PRESSING S/S
MIN PULSE WIDTH 20 mSEC, TYP ≈ 80 mSEC

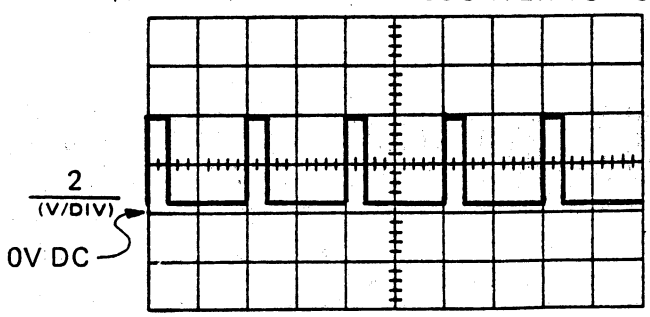
5 (NO.) U17-9 $\overline{\text{GATE}}$
(TRIG AS IN NO. 4)



100 mSEC/DIV

*NOTE:
PULSE WIDTH = TIME BETWEEN START → STOP

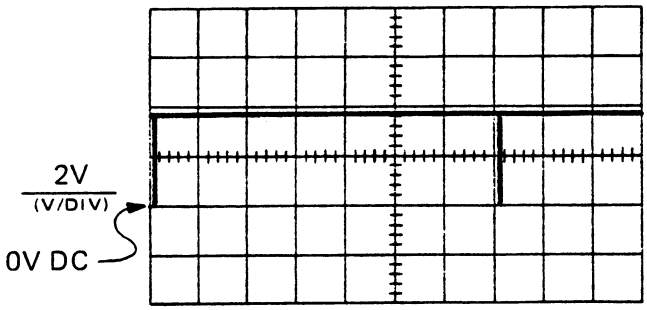
6 (NO.) U41-15 DECADE COUNTER INPUT
(TRIG ON "↑" EDGE INTERVAL)
(PRESS S/S ALLOWING COUNTER TO RUN)



5 mSEC/DIV

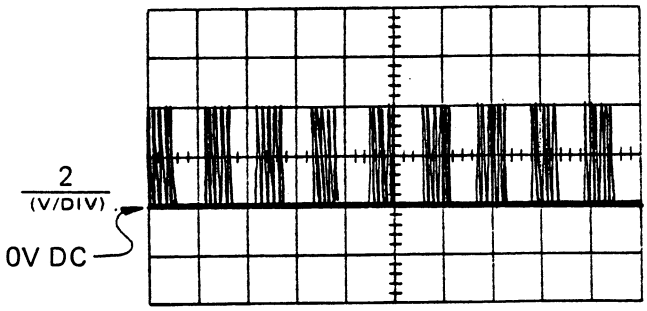
WAVEFORMS FOR TOTALIZE (MAIN LOGIC) UNIT PERFORMANCE TEST (Continued)

7 (NO.) U43-12
UPDATE
(TRIG ON "↓" EDGE INTERNAL)



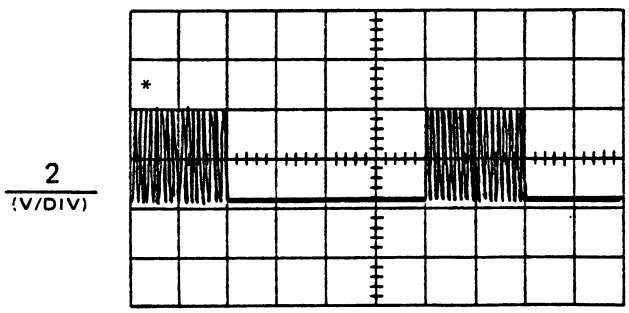
5 mSEC/DIV

8 (NO.) U50-11
ACCULULATOR CLOCK
(TRIG ON "↑" EDGE INTERNAL)



5 mSEC/DIV
(S/DIV)

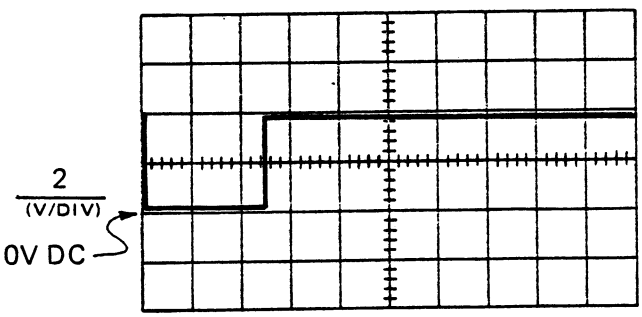
9 (NO.) U46-9
ACCUMULATOR DATA



.5 mSEC/DIV

*NUMBER OF PULSES IN GROUP WILL VARY WITH TOTAL COUNT

10 (NO.) TP5
CLEAR
(TRIG ON "↓" EDGE INTERNAL TRIG)



5 mSEC/DIV

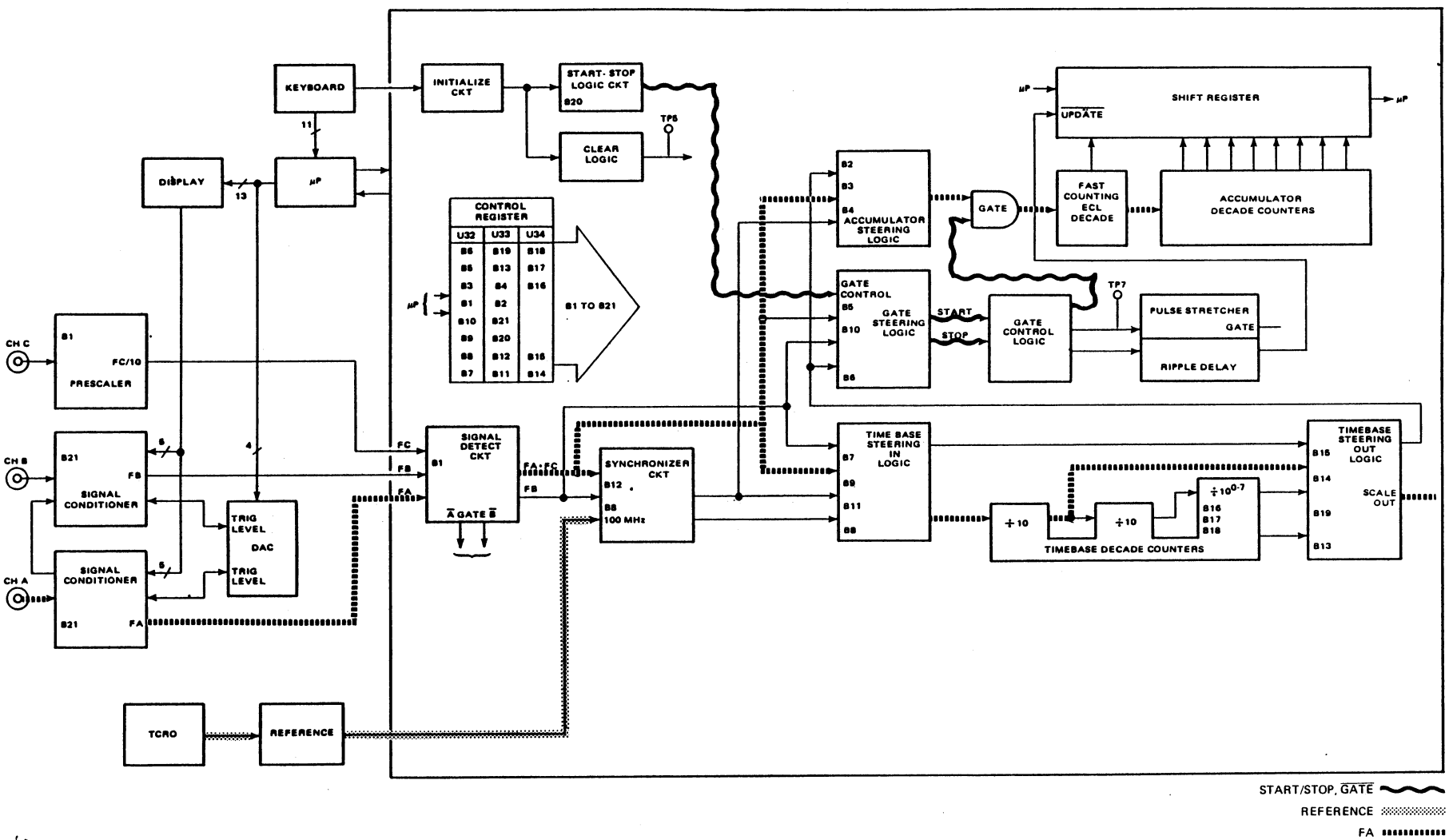


Figure 5.29 - Totalize (TO) Single Thread Diagram

5.11 SUBASSEMBLY PERFORMANCE TESTS.

5.11.1 Subassembly performance tests are designed to isolate a malfunction to a small group of components as a functional group of components. Once the trouble is narrowed down to a small area, the technician should resort to conventional troubleshooting techniques such as checking individual components (resistors, capacitors, semiconductors and IC's) and applications of heat and cold. Each of the subassembly performance tests is accompanied by performance standards for each step of the test. These performance standards are in the form of resistance measurement, DC (and AC) voltage measurements or oscilloscope waveforms.

5.11.2 In the case of the main logic PCB, the largest and most complex, several subassembly tests have been provided. These are segregated because the main logic PCB contains a number of separate functional circuits. Separate subassembly performance tests are provided for each of the remaining smaller PCB's.

5.11.3 The tolerance required for troubleshooting is looser than operating tolerances because the technician is generally looking for the presence of a signal or voltage, rather than an exact high tolerance standard. This allows the use of a much broader range of test equipment not subject to high accuracy calibration requirements. Troubleshooting, unlike calibration, may be done with any equipment that is accurate to $\pm$ 5%.

5.11.4 Note that the test points in the performance tables refer to the performance standard or waveforms in the test and to test point location on an assembly drawing that follows for each subassembly Performance Test. The presentation of assembly drawings in the troubleshooting section of the manual is redundant to the assembly drawings of Section 6, but it provides the necessary continuity and makes the technicians troubleshooting job easier.

WARNING

Removal of covers expose potentially lethal voltage. Avoid contact.

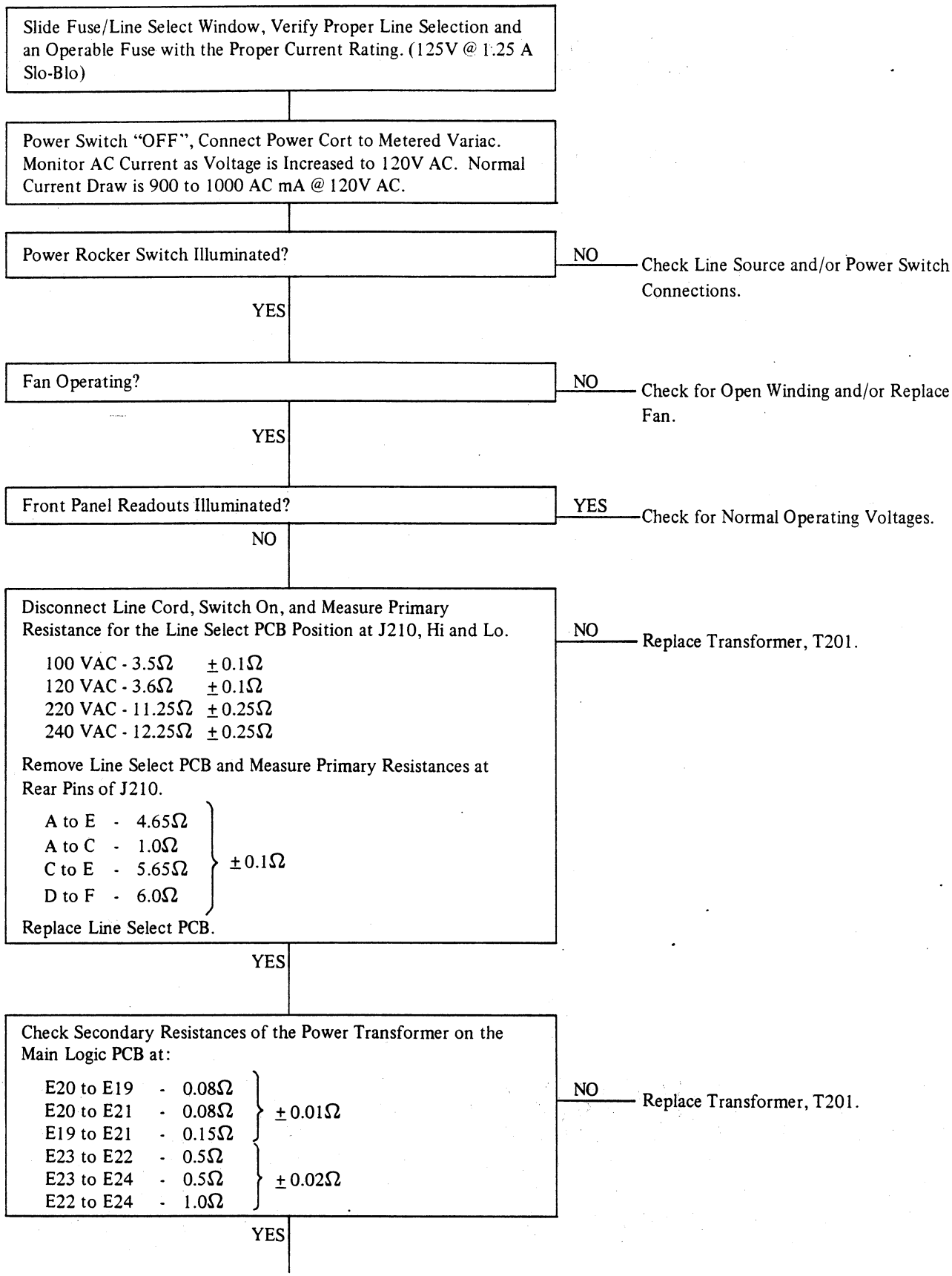


Figure 5.30 - Power Supply (Rear Panel & Main Logic) Subassembly Performance Test

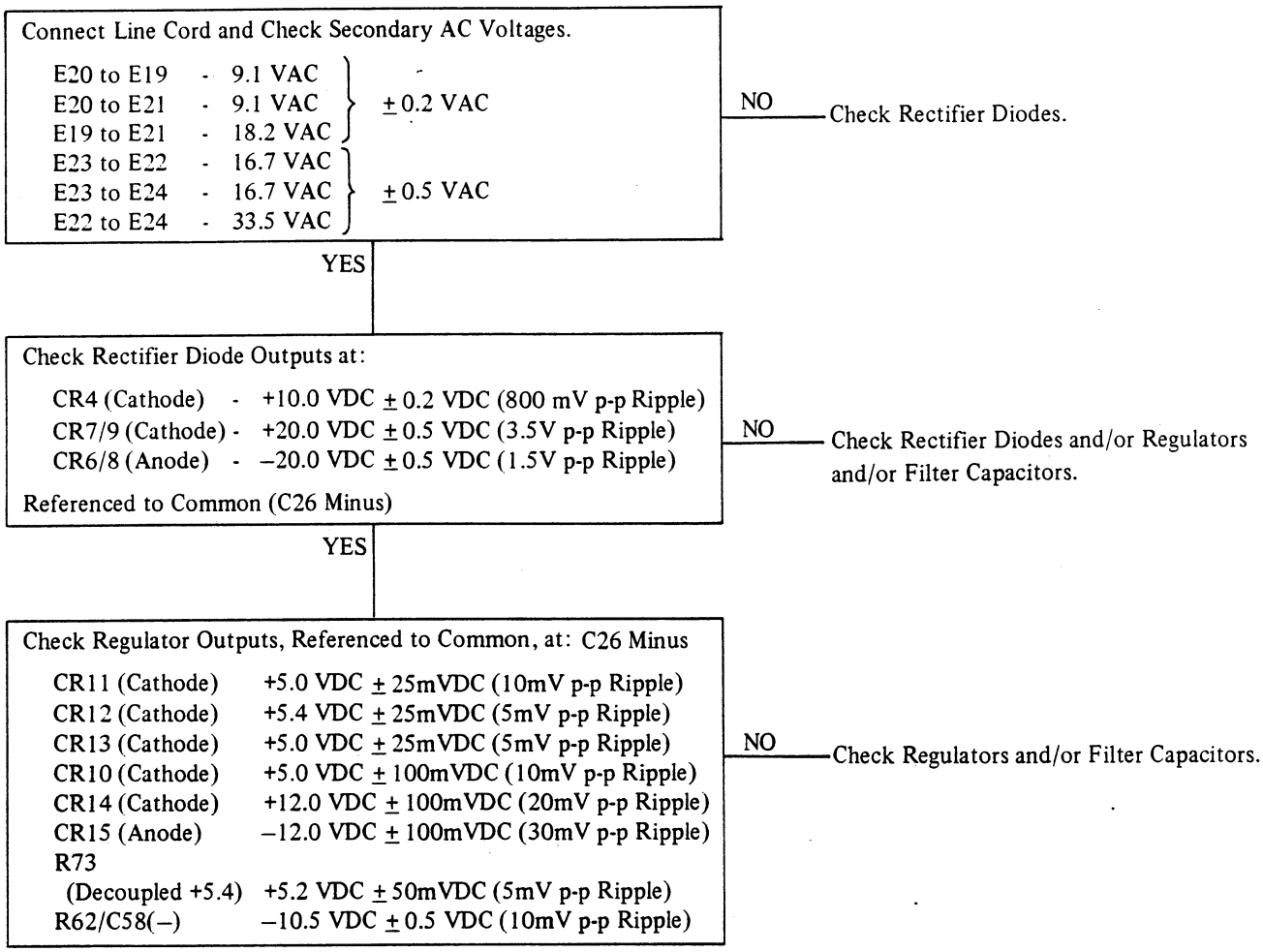


Figure 5.30 - Power Supply (Rear Panel & Main Logic) Subassembly Performance Test (continued)

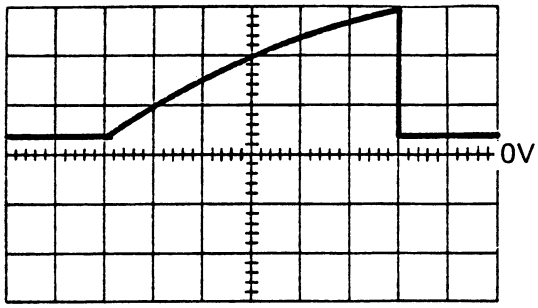
Table 5.18 - (Main Logic) Clear Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Test					Note: Measurement reference is CR11 (Anode).
Power Switch: On					
	Read Rate R/C	CR1 (Anode)	F	Fig 5.31	Waveform #1
	R/C Output	U26-13	G	Fig 5.31	Waveform #2
	$\overline{\text{MF ENABLE}}$	U26-3	H	Fig 5.31	Waveform #3
	Enable Drive	U27-8	I	Fig 5.31	Waveform #4
	R/S F/F Out	U19-3	J	Fig 5.31	Waveform #5
	DATA READY RESET	U26-6	K	Fig 5.31	Waveform #6
	$\overline{\text{CLEAR}}$	U18-1	L	Fig 5.31	Waveform #7
Norm/Hold: Hold Keyboard: RS	$\overline{\text{COMP MF CLEAR}}$	U27-4/5	M	Fig 5.31	Waveform #8

WAVEFORMS FOR CLEAR (MAIN LOGIC)
SUBASSEMBLY PERFORMANCE TEST

1 (NO.) CR1 (ANODE)

READ RATE R/C

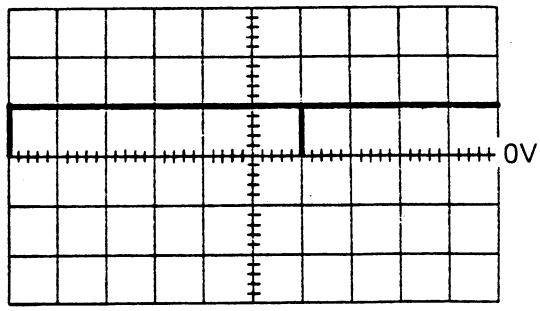


1 (V/DIV)

20mS (S/DIV)

2 (NO.) U26-13

R/C OUTPUT



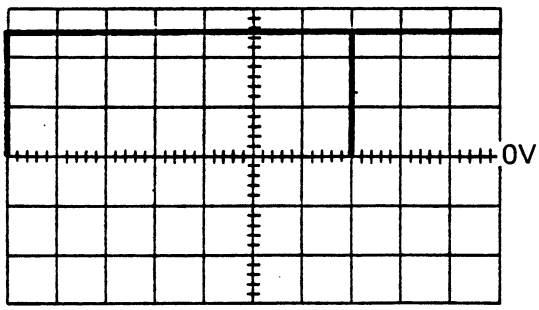
2 (V/DIV)

20mS (S/DIV)

PULSE WIDTH: 50 μSEC

3 (NO.) U26-3

$\overline{\text{MF ENABLE}}$



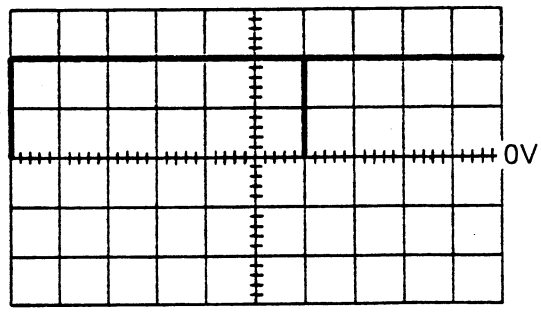
2 (V/DIV)

20mS (S/DIV)

PULSE WIDTH: ≈ 7 μSEC

4 (NO.) U27-8

ENABLE DRIVE



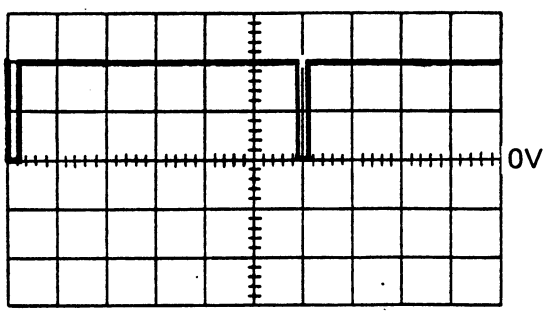
2 (V/DIV)

20mS (S/DIV)

PULSE WIDTH: ≈ 7 μSEC

5 (NO.) U19-3

R/S F/F OUT



2 (V/DIV)

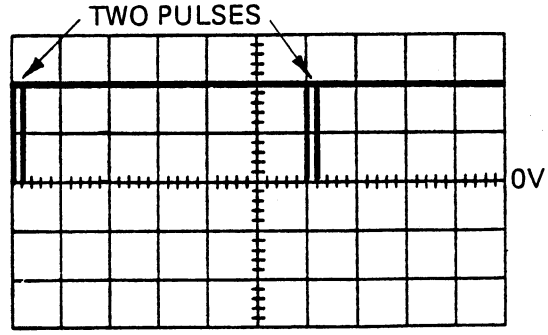
20mS (S/DIV)

PULSE WIDTH: ≈ 3.8mS

6 (NO.) U26-6

$\overline{\text{DATA READY RESET}}$

TWO PULSES



2 (V/DIV)

20mS (S/DIV)

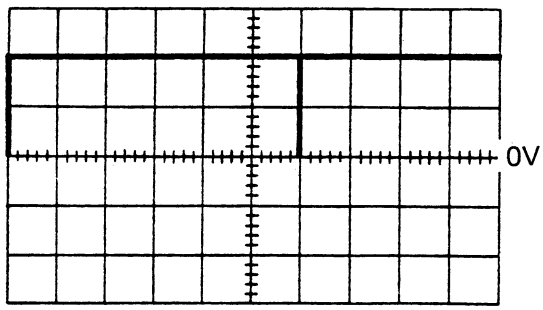
PULSE WIDTH: 7 μSEC

WAVEFORMS FOR CLEAR (MAIN LOGIC) SUBASSEMBLY PERFORMANCE TEST Continued

7 (NO.)

U18-1

$\overline{\text{CLEAR}}$



2 (V/DIV)

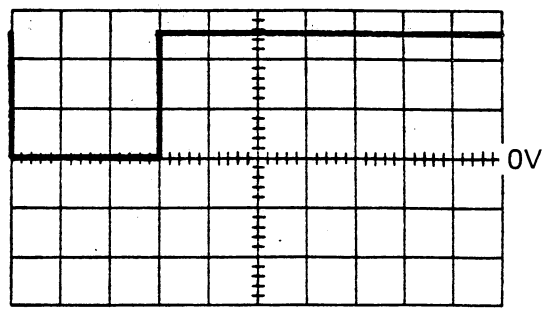
20mS (S/DIV)

PULSE WIDTH: ≈50 μS

8 (NO.)

U27-4/5

$\overline{\text{COMP MF CLEAR}}$



2 (V/DIV)

5 μSEC (S/DIV)

PULSE WIDTH: ≈15 μSEC

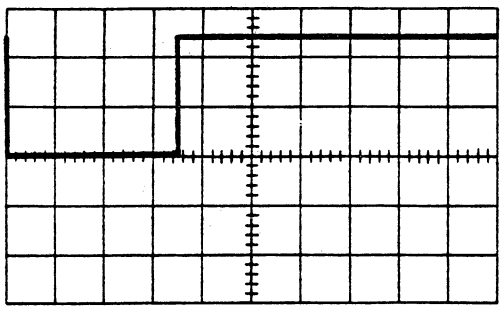
Table 5.19 - (Main Logic) Start/Stop Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Test (Ch. A) Slope: ↑ (Ch. A) Coupling: DC (Ch. B) Slope: ↓ (Ch. B) Coupling: DC					Note: Measurement reference is CR11 (anode).
Power Switch: On					
Keyboard: SS	One/Shot Output	U30-1	N	Fig 5.31	7mS Logic Low Pulse Waveform #1
Keyboard: TO,SS Display Counts	Start/Stop	U30-5	O	Fig 5.31	Waveform #2
Keyboard: SS Display Stops Count	R/S F/F Output	U30-3	P	Fig 5.31	Waveform #3
Keyboard: SS,SS Starts/Stops Count	$\overline{\text{GATE CONTROL}}$	U18-13	Q	Fig 5.31	Waveform #4

WAVEFORMS FOR START/STOP (MAIN LOGIC) SUBASSEMBLY PERFORMANCE TEST

1 (NO.) U30-1

ONE/SHOT OUTPUT

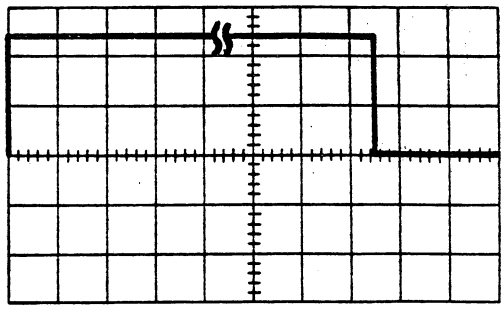


2 (V/DIV)

2mS (S/DIV)

2 (NO.) U30-5

S/S



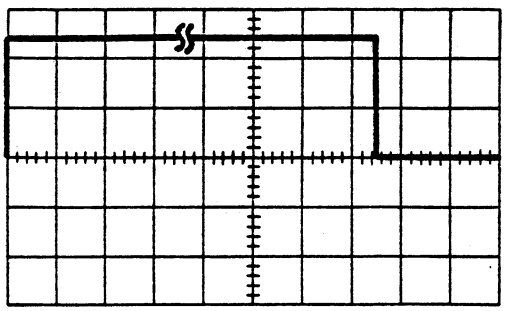
2 (V/DIV)

20mS (S/DIV)

SIGNAL STAYS HIGH
UNTIL "SS" SWITCH IS RELEASED

3 (NO.) U30-3

R/S F/F OUT

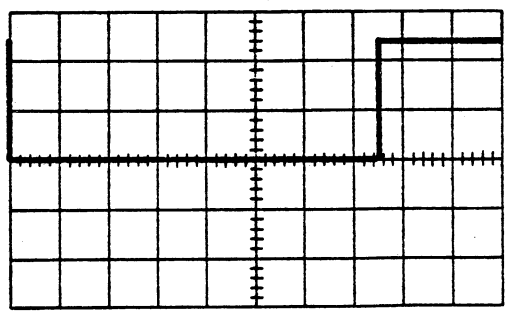


2 (V/DIV)

20mS (S/DIV)

SIGNAL STAYS HIGH
UNTIL "SS" SWITCH IS RELEASED

4 (NO.) 12-2



2 (V/DIV)

20mS (S/DIV)

SIGNAL STAYS LOW
UNTIL "SS" SWITCH IS RELEASED

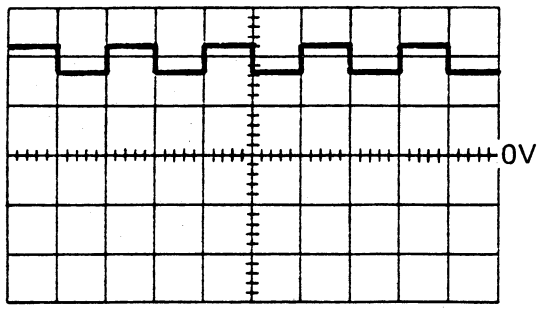
Table 5.20 - (Main Logic) Signal Detector Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Com (Ch. A) Slope: ↑ (Ch. A) Coupling: DC (Ch. B) Slope: ↓ (Ch. B) Coupling: DC					Note: Measurement reference is CR11 (anode).
					Note: Trigger scope on internal, plus.
Power Switch: On					
Apply a (scope cal) signal of 1V @ 1 KHz to the Ch. A input.					
	ECL FA	U8-6	R	Fig 5.31	Waveform #1
	ECL FB	U8-11	S	Fig 5.31	Waveform #2
Keyboard: (Ch. A): TL, AU	GATE A F/F Q	U8-2	T	Fig 5.31	Waveform #3
	GATE A F/F $\bar{Q}$	U8-3	U	Fig 5.31	Waveform #4
Keyboard: (Ch. B): TL, AU	GATE B F/F Q	U8-15	V	Fig 5.31	Waveform #5
	GATE B F/F $\bar{Q}$	U8-14	W	Fig 5.31	Waveform #6
Keyboard: (Ch. A): TL, AU	$\overline{\text{GATE A}}$	R21	X	Fig 5.31	Waveform #7
	$\overline{\text{GATE B}}$	R23	Y	Fig 5.31	Waveform #8
Keyboard: (Ch. B): TL, AU	$\overline{\text{GATE A}}$	R21	X	Fig 5.31	Waveform #9
	$\overline{\text{GATE B}}$	R23	Y	Fig 5.31	Waveform #10

WAVEFORMS FOR SIGNAL DETECTOR (MAIN LOGIC) SUBASSEMBLY PERFORMANCE TEST

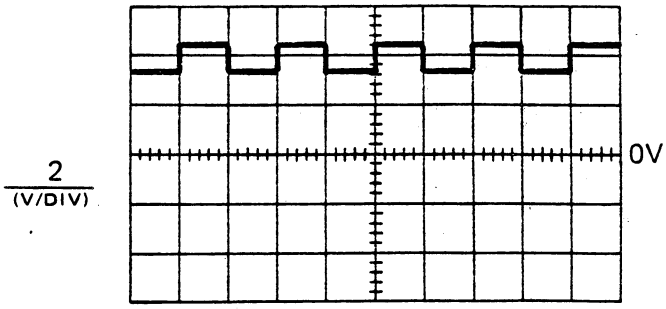
1 (NO.) U8-6

ECL FA



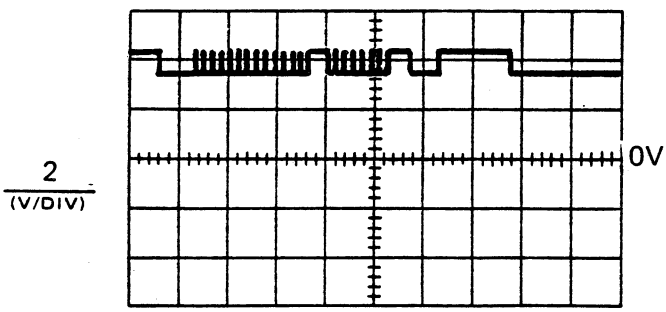
2 (NO.) U8-11

ECL FB



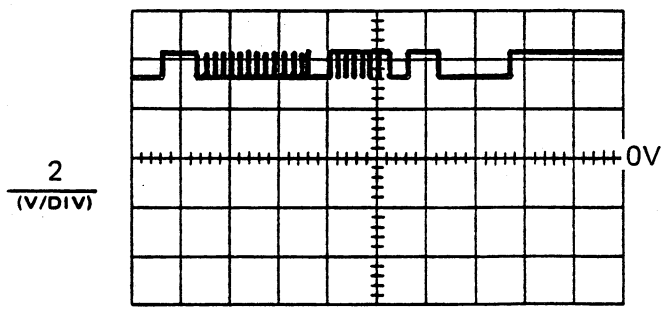
3 (NO.) U8-2

GATE A F/F Q



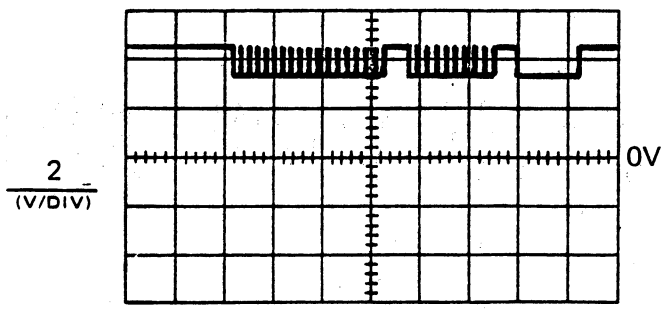
4 (NO.) U8-3

GATE A F/F $\bar{Q}$



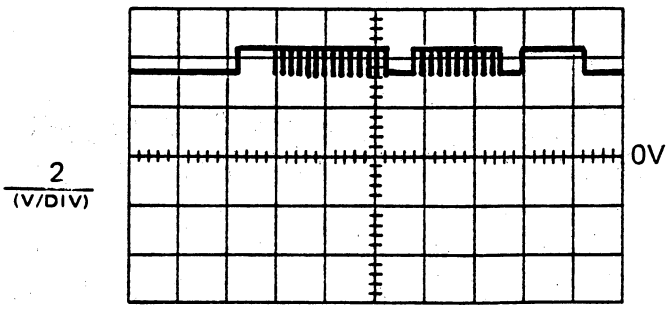
5 (NO.) U8-15

GATE B F/F Q



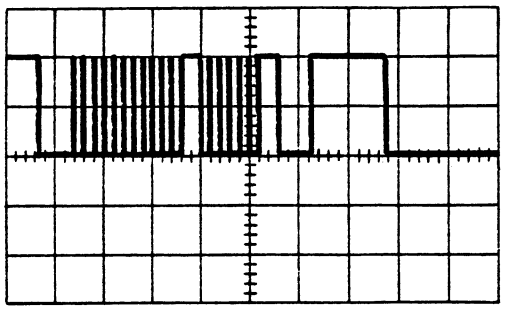
6 (NO.) U8-14

GATE B F/F $\bar{Q}$



WAVEFORMS FOR SIGNAL DETECTOR (MAIN LOGIC) SUBASSEMBLY PERFORMANCE TEST Continued

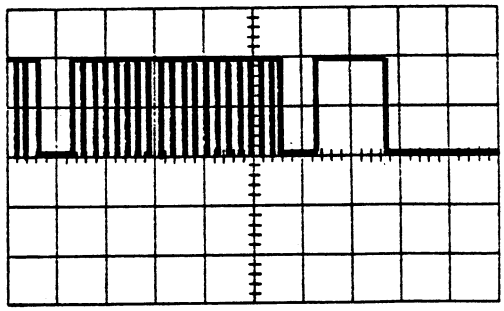
7 (NO.) R21 GATE A



2 (V/DIV)

20mS (S/DIV)

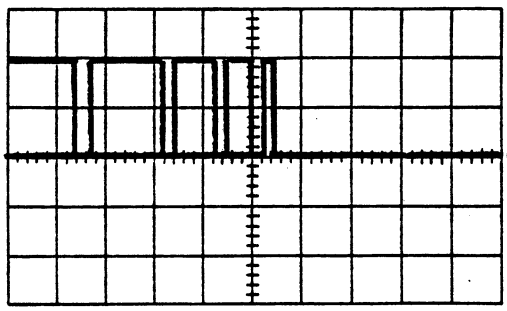
8 (NO.) R23 GATE B



2 (V/DIV)

20mS (S/DIV)

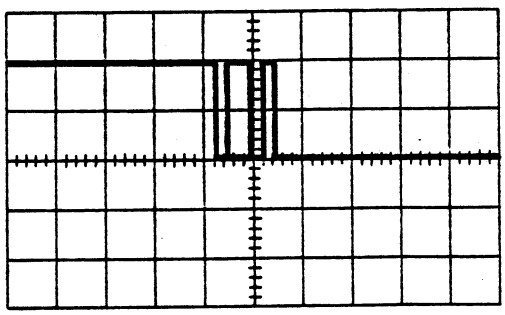
9 (NO.) R21 GATE A



2 (V/DIV)

.2S (S/DIV)

10 (NO.) R23 GATE B



2 (V/DIV)

.2S (S/DIV)

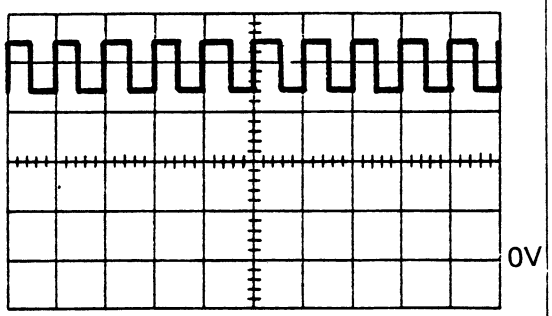
Table 5.21 - (Main Logic) Synchronizer Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Com (Ch. A) Slope: ↑ (Ch. A) Coupling: DC (Ch. B) Slope: ↓ (Ch. B) Coupling: DC					Note: Measurement reference is CR11 (anode).
Power Switch: On					
Apply a (scope cal) signal of 1V @ 1 KHz to the Ch. A input.					
Keyboard: AV (Ch. A): TL, AU (Ch. B): TL, AU					
	ECL FA (Start)	U4-6	Z	Fig 5.31	Waveform #1
	ECL FB (Stop)	U3-11	a	Fig 5.31	Waveform #2
	Measurement Start	U12-9	b	Fig 5.31	Waveform #3
	Intervals Averaged Measurement Period	U12-2	c	Fig 5.31	Waveform #4

WAVEFORMS FOR SYNCHRONIZER (MAIN LOGIC) SUBASSEMBLY PERFORMANCE TEST

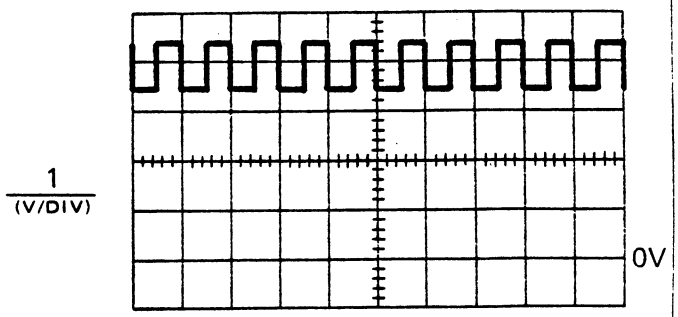
1 (NO.) U4-6

ECL FA (START)



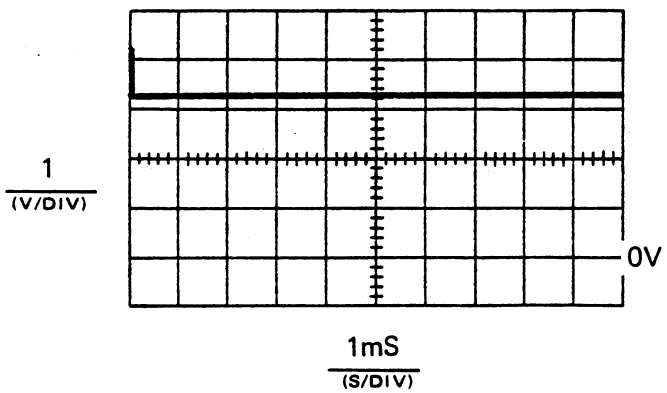
2 (NO.) U3-11

ECL FB (STOP)



3 (NO.) U12-9

MEASUREMENT START



4 (NO.)

INTERVALS AVERAGED (10)
(MEASUREMENT PERIOD)

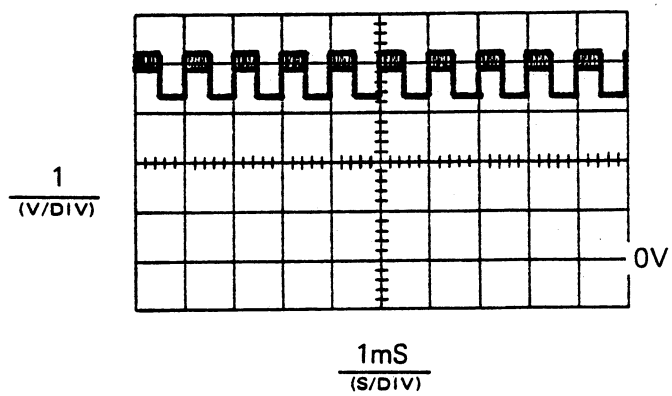


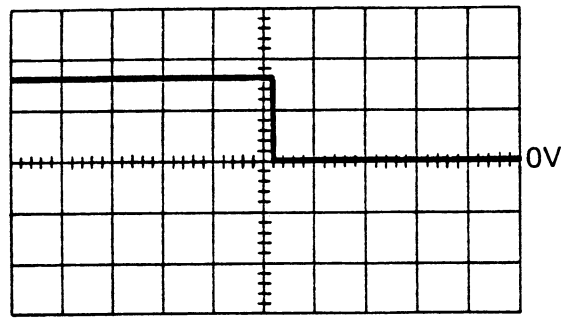
Table 5.22 - (Main Logic) Gate Control Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Com (Ch. A) Slope: (Ch. A) Coupling: DC (Ch. B) Slope: (Ch. B) Coupling: DC					Note: Measurement reference is CR11 (anode).
					Note: Externally trigger "–" on TP5 $\overline{\text{CLEAR}}$.
Power Switch: On					
Apply a (scope cal) signal of 1V @ 1 KHz to the Ch. A input.					
Keyboard: AV (Ch. A): TL, AU (Ch. B): TL, AU					
	Arm	U36-9	d	Fig 5.31	Waveform #1
	Start Sig	U25-6	e	Fig 5.31	Waveform #2
	Gate Enable F/F	U25-2	f	Fig 5.31	Waveform #3
	Stop Sig	U25-11	g	Fig 5.31	Waveform #4
	Gate Disable	U25-15	h	Fig 5.31	Waveform #5
	$\overline{\text{GATE}}$	U17-9	i	Fig 5.31	Waveform #6
	Ripple Delay Output	U10-11	j	Fig 5.31	Waveform #7
	$\overline{\text{DATA OUTPUT}}$	U10-8	k	Fig 5.31	Waveform #8
	$\overline{\text{GATE}}$	U43-6	l	Fig 5.31	Waveform #9
	$\overline{\text{UPDATE}}$	U43-12	m	Fig 5.31	Waveform #10

WAVEFORMS FOR GATE CONTROL (MAIN LOGIC) SUBASSEMBLY PERFORMANCE TEST

1 (NO.) U36-9

ARM

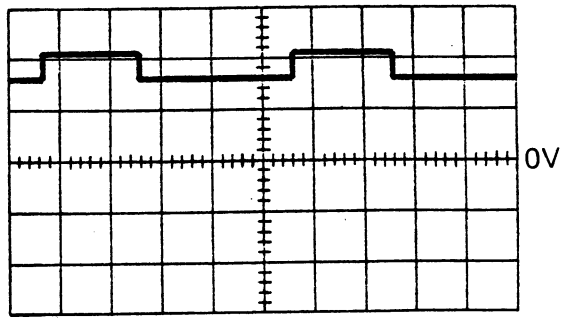


2 (V/DIV)

2mS (S/DIV)

2 (NO.) U25-6

START SIGNAL

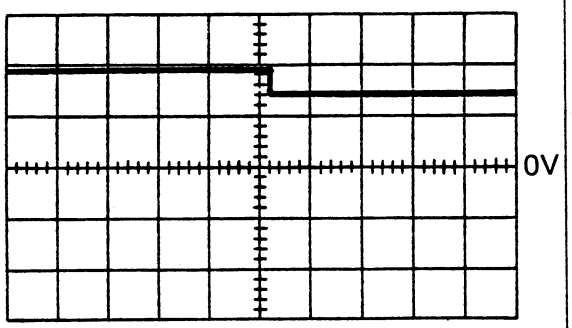


2 (V/DIV)

2mS (S/DIV)

3 (NO.) U25-2

GATE ENABLE F/F

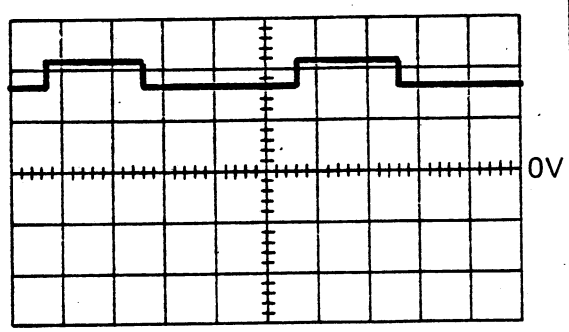


2 (V/DIV)

2mS (S/DIV)

4 (NO.) U25-11

STOP SIGNAL

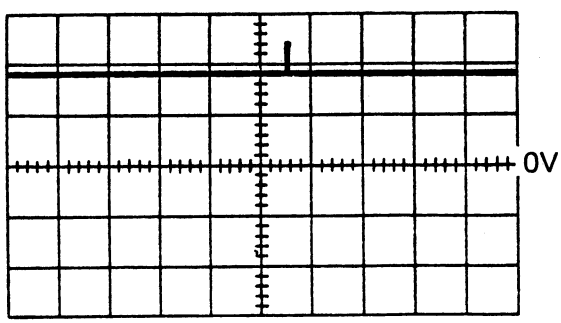


2 (V/DIV)

2mS (S/DIV)

5 (NO.) U25-15

GATE ENABLE

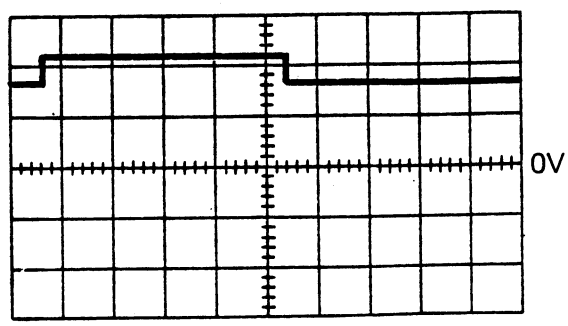


2 (V/DIV)

2mS (S/DIV)

6 (NO.) U17-9

GATE



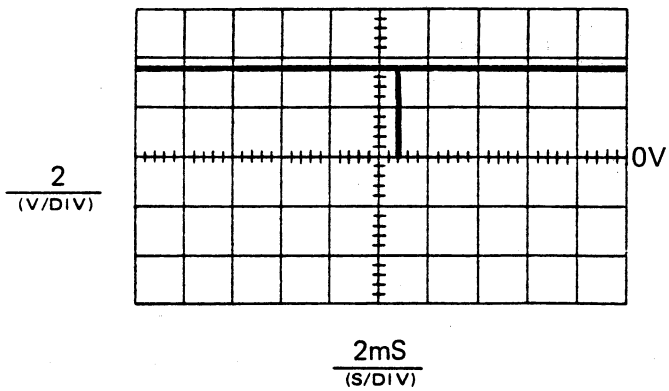
2 (V/DIV)

2mS (S/DIV)

WAVEFORMS FOR GATE CONTROL (MAIN LOGIC) SUBASSEMBLY PERFORMANCE TEST Continued

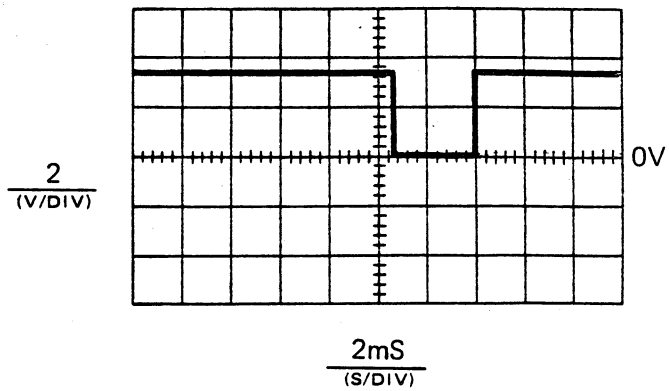
7 (NO.) U10-11

RIPPLE DELAY OUT



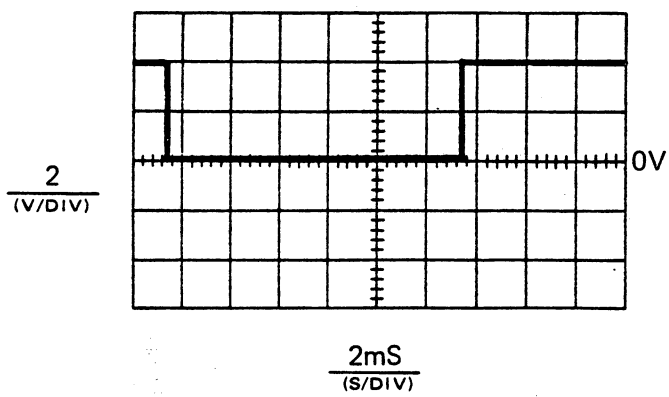
8 (NO.) U10-8

DATA OUTPUT



9 (NO.) U43-6

GATE



10 (NO.) U43-12

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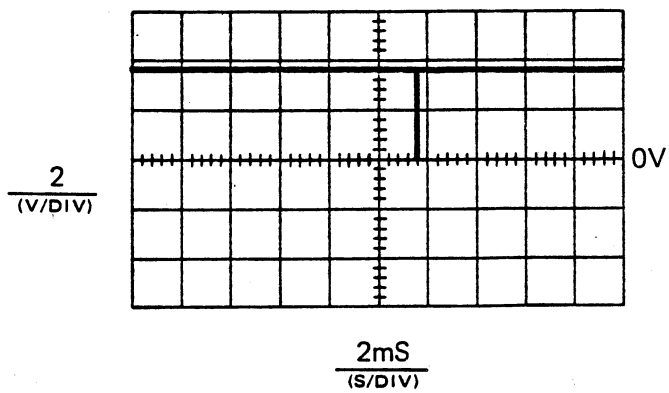


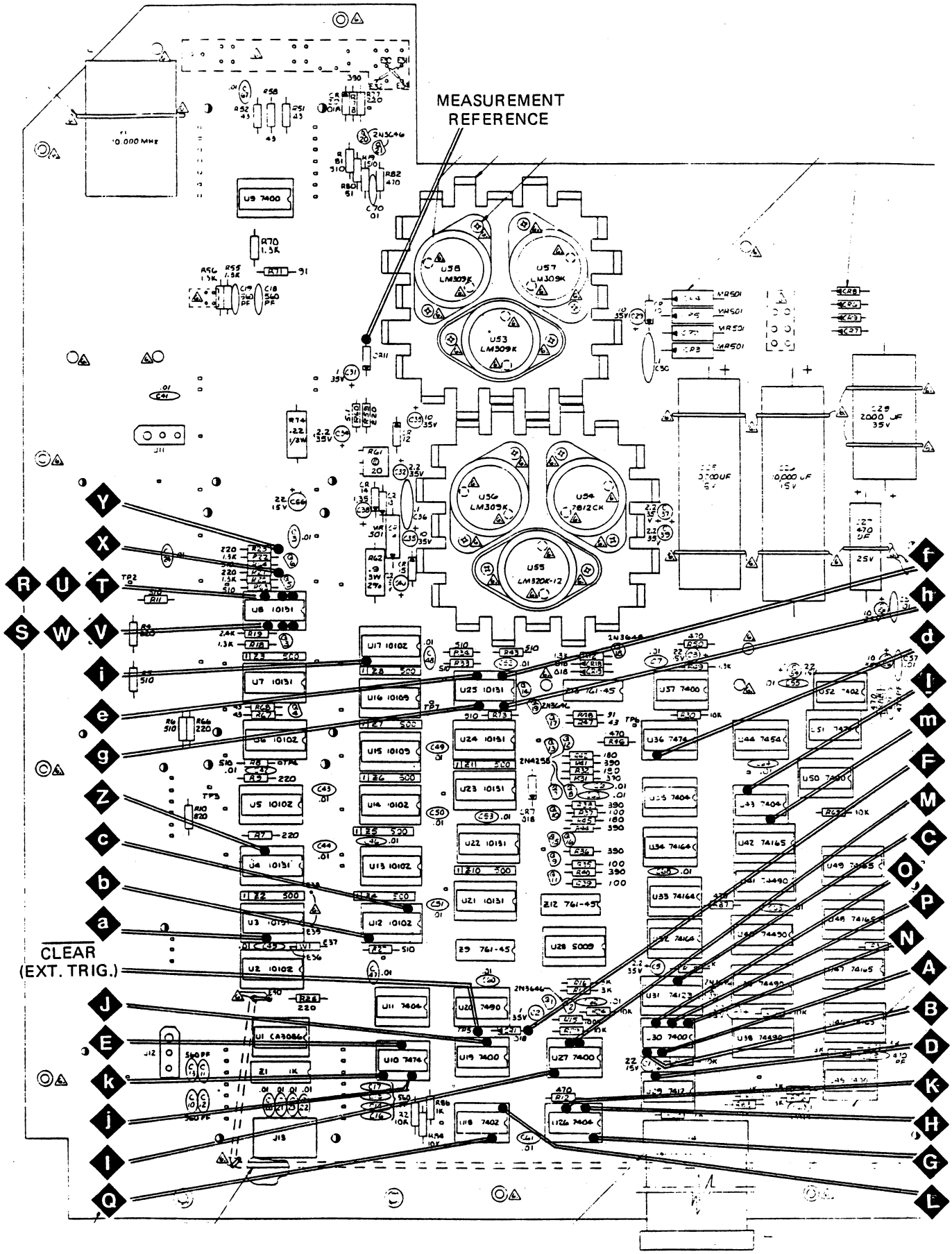


Figure 5.31 - Main Logic Subassembly Test Points

5.12 MAIN LOGIC SIG/REF CIRCUITS.

5.12.1 The Main Logic contains circuits that control the signal (or signals) and reference (100 MHz) frequencies that complete the organization for the function and timebase/ multiplier selection. The signal path for these circuits is largely controlled by the outputs of the Control Register (U32, 33, 34) "B" outputs.

5.12.2 The Accumulator Steering Logic enables a signal to be applied to the main gate and is outlined in Table 5.23.

5.12.3 The Gate Steering Logic enables a signal to the start and stop sequence for the Data Control Circuits, as outlined in Table 5.24.

5.12.4 The Timebase In Steering Logic enables a signal to be applied to the timebase counter as outlined in Table 5.25.

5.12.5 The Timebase Counter divides the output of the Timebase Steering Logic by decode factors to be applied to the Timebase Out Steering Logic to be used for measurement processing or for Scaled Output as outlined in Table 5.26. The Control Register logic codes for U28, the 10^{0-7} decode counter, are shown in Table 5.27.

Table 5.23 - Accumulator Steering Logic Signal Paths

Function	Signal Path	TB/Mult.	Freq.	Control Register Enable
FA	U5-15	All	Sig	B3
FC	U5-15	All	Sig	B3
P	U13-3	10^{-8}	Ref	B4
P	U18-10	10^{-7} to 10^{1}	Ref	B2
TI	U13-3	10^{-8}	Ref	B4
TI	U18-10	10^{-7} to 10^{1}	Ref	B2
PA	U13-3	All	Ref	B4
T1A	U13-3	All	Ref	B4
A/B	U5-15	All	Sig	B3
T0	U5-15	All	Sig	B3

Table 5.24 - Gate Steering Logic

Function	Signal Path	Signal	Control Register Enable
FA	U18-4	TB ST Out	B6
FC	U18-4	TB ST Out	B6
P	U17-3	FA	B5
TI	U17-2	FA	B10
TI	U5-14	FB	B10
PA	U18-4	TB ST Out	B6
T1A	U18-4	TB ST Out	B6
A/B	U18-4	TB ST Out	B6
TO	None	-	-

Table 5.25 - Timebase In Steering Logic

Function	Signal Path	Signal	Control Register Enable
FA	U13-2	Ref	B11
FC	U13-2	Ref	B11
P	U13-2	Ref	B11
TI	U13-2	Ref	B11
PA	U5-2	FA	B9
T1A	U13-14	Sync	B8
A/B	U5-3	FB	B7
T0	-	-	-

Table 5.26 - Timebase Counter

Function	÷ 10 Out 1	÷ 10 Out 2	÷ 10^0 to ÷ 10^{-7}	TB/Mult.	Input to T/B Steering Out	
					Input	Enable
FA	U20-1	U20-12	U43-2	10^{-6}	U44-13	B19
FA	U20-1	U20-12	U36-6	10^{-5} to 10^{1}	U44-10	B13
FC	U20-1	U20-12	U43-2	10^{-6}	U44-13	B19
FC	U20-1	U20-12	U43-6	10^{-5} to 10^{1}	U44-10	B13
P	U20-1	-	-	10^{-7}	U44-5	B14
P	U20-1	U20-12	-	10^{-6}	U44-13	B19
P	U20-1	U20-12	U43-6	$10^{-5}$to 10^{1}	U44-10	B13
T1	U20-1	-	-	10^{-7}	U44-5	B14
T1	U20-1	U20-12	U43-2	10^{-6}	U44-13	B19
T1	U20-1	U20-12	U36-6	10^{-5} to 10^{1}	U44-10	B13
PA	-	-	-	10	U44-3	B15
PA	U20-1	-	-	10^{1}	U44-5	B14
PA	U20-1	U20-12	U43-2	10^{2}	U44-13	B19
PA	U20-1	U20-12	U36-6	10^{3} to 10^{7}	U44-10	B13
T1A	-	-	-	10	U44-3	B15
T1A	U20-1	-	-	10^{1}	U44-5	B14
T1A	U20-1	U20-12	U43-2	10^{2} to 10^{7}	U44-13	B19
A/B	-	-	-	10	U44-3	B15
A/B	U20-1	-	-	10^{1}	U44-5	B14
A/B	U20-1	U20-12	U43-2	10^{2}	U44-13	B19
A/B	U20-1	U20-12	U36-6	10^{3} to 10^{8}	U44-10	B13
T0	-	-	-	10	U44-3	B15
T0	U20-1	-	-	10^{1}	U44-5	B14
T0	U20-1	U20-12	U43-2	10^{2}	U44-13	B19
T0	U20-1	U20-12	U36-6	10^{3} to 10^{9}	U44-10	B13

Table 5.27 - ÷ $10^{0 \text{ to } 7}$ Counter Decode For T/B Multiplier

B16	B17	B18	FA	FC	P	T1	PA	T1A	A/B	T0
1	1	1	+1	+1	+1	+1	-	-	-	+9
1	1	0	0	0	0	0	-	-	+8	+8
1	0	1	–1*	–1*	–1	–1	+7	+7	+7	+7
1	0	0	–2	–2	–2	–2	+6	+6	+6	+6
0	1	1	–3	–3	–3	–3	+5	+5	+5	+5
0	1	0	–4	–4	–4	–4	+4	+4	+4	+4
0	0	1	–5	–5	–5	–5	+3	+3	+3	+3
0	0	0	–6	–6	–6	–6	+2	+2	+2	+2

*Home State Where Applicable

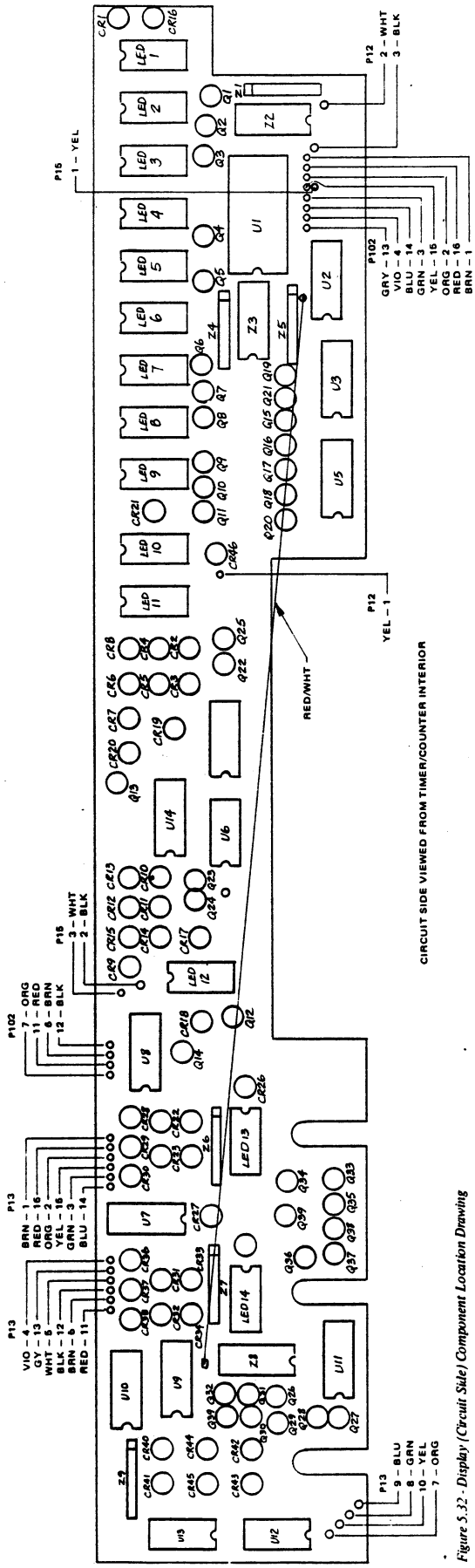
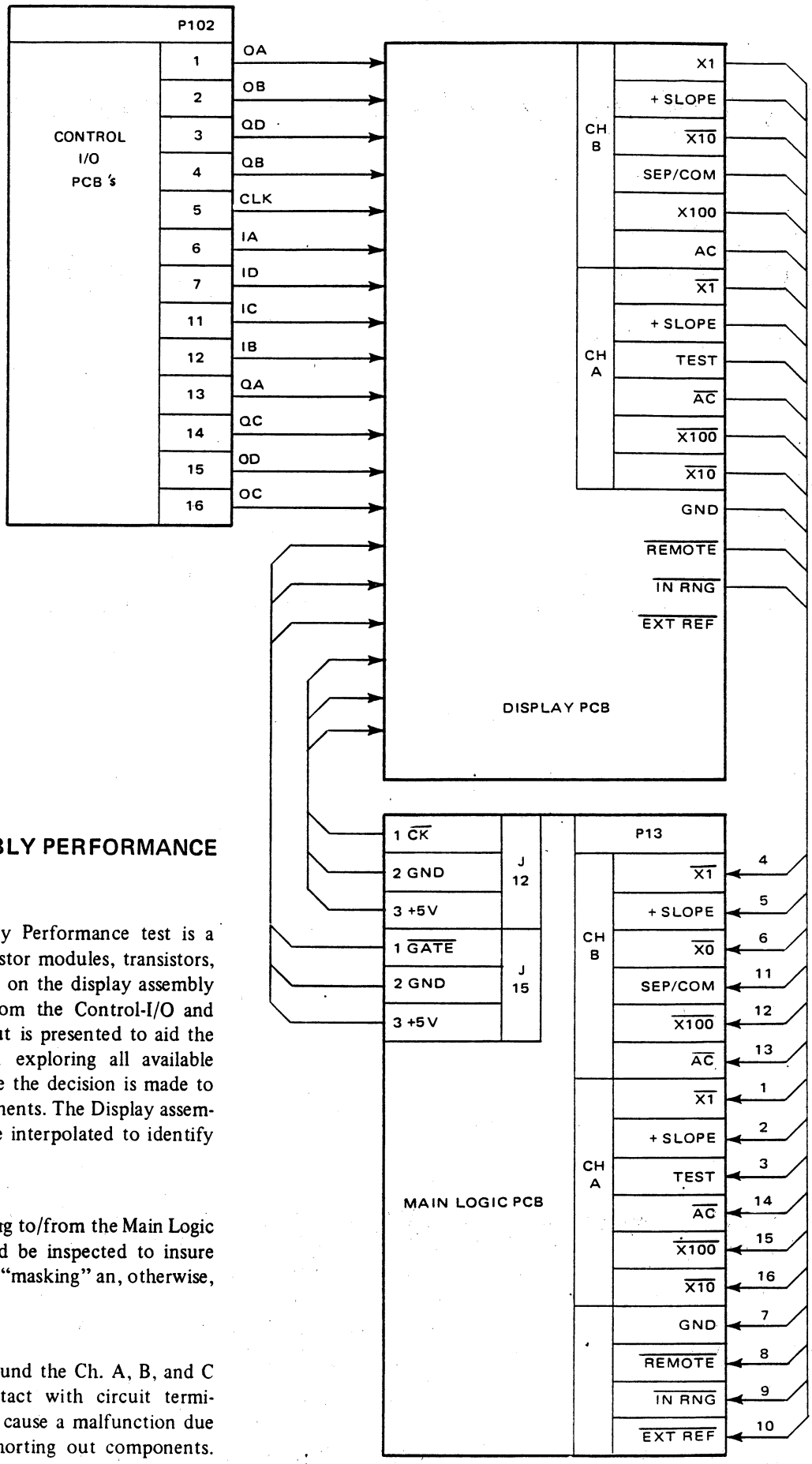


Figure 5.32 - Display (Circuit Side) Component Location Drawing



5.13 DISPLAY SUBASSEMBLY PERFORMANCE TEST.

5.13.1 The Display Subassembly Performance test is a circuit side layout of the IC, resistor modules, transistors, and LED components. The events on the display assembly are a result of output signals from the Control-I/O and Main Logic assemblies. The layout is presented to aid the maintenance/repair technician in exploring all available troubleshooting test points before the decision is made to disassemble and/or replace components. The Display assembly drawing in Section 6 must be interpolated to identify test points.

5.13.2 The interconnection wiring to/from the Main Logic and Control-I/O assemblies should be inspected to insure that broken or open leads are not "masking" an, otherwise, apparent malfunction.

5.13.3 The circuit side area around the Ch. A, B, and C input connectors can make contact with circuit terminations; which, if punctured, can cause a malfunction due to the cable shield (common) shorting out components.

Figure 5.33 - Display Input/Output Signals

Table 5.28 - **Signal Conditioner (Ch. A/Ch. B) Subassembly Performance Test**

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
The following tests are to be used to check the performance of both Ch. A and Ch. B signal conditioners. To extend the Ch. A PCB assembly, disconnect the input cables at J17/J18, remove the assembly, and remove the shields. Mount the assembly on the extender PCB, P/N 406851, and re-install at J4 on the main logic PCB assembly (check that all pins are straight, well seated, and do not interfere with assembly circuitry). Connect the Ch. A input cable to J18, instead of (normal) J17, due to cable length, and leave the cable from Ch. B open, but not to interfere with adjacent circuits or PCB's. Channel B signal conditioner should be extended in the same manner at J3, except the input cable for Ch. A should be used to provide a signal input at J19.					
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Sep (Ch. A) Slope: ↑ (Ch. A) Coupling: AC					Note: Measurements are referenced to J4-1 (Ch. A) or J3-1 (Ch. B).
Power: On No Input Signal Keyboard: (Ch. A) TL, AU					Front Panel Indication: Funct: T1, 10^{-8} Sec Status: AC, ↑ , ≈ 0.00
	+12 VDC	P3 (P4) - 13	1	Fig 5.34	+12V ±0.5 VDC
	+5.4 VDC	P3 (P4) - 10	2	Fig 5.34	+5.4V ±0.25 VDC
	–12 VDC	PC (P4) - 14	3	Fig 5.34	–12V ±0.5 VDC
	Decoupled +12V	L4	4	Fig 5.34	+12V ±0.5 VDC
	Decoupled +5V	L2	5	Fig 5.34	+5.4V ±0.25 VDC
	Decoupled –12V	L1	6	Fig 5.34	–12V ±0.5 VDC
	+ Clamp Voltage	CR8 (Cathode)	7	Fig 5.34	+3.3V ±0.25 VDC
	– Clamp Voltage	CR9 (Anode)	8	Fig 5.34	–3.3V ±0.25 VDC
	Trigger Level	P3 (P4) - 12	9	Fig 5.34	0V ±0.0125 VDC
Funct: T1 or T1 AV Funct: FA	$\overline{TI \cdot TIA}$ (B21)	P3 (P4) - 16	10	Fig 5.34	–0.4V ±0.025 VDC +2.5V ±0.05 VDC
Slope: Slope:	+ Slope	P3 (P4) - 7	11	Fig 5.34	+3.5V ±0.1 VDC +0.2V ±0.05 VDC
	Amp In (Sig)	Q1a (Gate)	12	Fig 5.34	0V ±0.001 VDC
	Amp In (Ref)	Q1b (Gate)	13	Fig 5.34	0V ±0.0125 VDC
The following voltage levels are made to U1, U2 and U3 (transistor arrays) without regard to signal nomenclature, but notations will be indicated as to Slope: ↑ , Slope: ↓ , T1 (AV), or FA.					

Table 5.28 - **Signal Conditioner (Ch. A/Ch. B) Subassembly Performance Test (continued)**

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
		U3-1	14	Fig 5.34	+3.5V ±0.025 VDC
		U3-2	15	Fig 5.34	–0.7V ±0.1 VDC
		U3-3	16	Fig 5.34	–0.9V ±0.1 VDC
		U3-4	17	Fig 5.34	+3.3V ±0.2 VDC
		U3-6	18	Fig 5.34	+3.3V ±0.2 VDC
		U3-7	19	Fig 5.34	+3.5V ±0.2 VDC
		U3-8	20	Fig 5.34	+0.2V ±0.025 VDC
		U3-9	21	Fig 5.34	–4.8V ±0.05 VDC
		U3-10	22	Fig 5.34	–4.0V ±0.05 VDC
		U3-11	23	Fig 5.34	+0.2V ±0.025 VDC
Slope: ↑ Slope: ↓		U2-1/5	24	Fig 5.34	+7.62V ±0.01 VDC +7.68V ±0.01 VDC
Slope: ↑ Slope: ↓	+ Slope Sig	U2-2	25	Fig 5.34	+5.12V ±0.02 VDC +1.17V ±0.02 VDC
Slope: ↑ Slope: ↓	ECL Trig Out	U2-3	26	Fig 5.34	+4.30V ±0.01 VDC +4.24V ±0.01 VDC
Slope: ↑ (Off) Slope: ↓ (On)	–Slope Sig	U2-4	27	Fig 5.34	+1.16V ±0.02 VDC +5.10V ±0.02 VDC
	Schmitt Trig Dr	U2-6(-)/9(+)	28	Fig 5.34	+4.3 to +5.3 VDC
	Schmitt Trig Out	U2-7(-)/10(+)	29	Fig 5.34	+3.6 to 4.5 VDC
		U2-8/11	30	Fig 5.34	+8.85V ±0.01 VDC
Slope: ↑ (On) Slope: ↓ (Off)	+ Slope Dr	U2-12	31	Fig 5.34	+0.04V ±0.01 VDC +0.82V ±0.01 VDC
Slope: ↑ (On) Slope: ↓ (Off)	+ Slope Out	U2-14	32	Fig 5.34	+5.0V ±0.5 VDC +0.1V ±0.02 VDC
Slope: ↑ (Off) Slope: ↓ (On)	Hysteresis Compensation Out (– Slope)	U1-1	33	Fig 5.34	+3.7V ±0.025 VDC +2.4V ±0.025 VDC
		U1-2	34	Fig 5.34	0V ±0.0005 VDC
		U1-3/14	35	Fig 5.34	–6.6V ±0.05 VDC

Table 5.28 - **Signal Conditioner (Ch. A/Ch. B) Subassembly Performance Test** (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Slope: ↑ (On) Slope: ↓ (Off)	Hysteresis Compensation DR (+ Slope)	U1-4	36	Fig 5.34	+1.4V ± 0.05 VDC −1.4V ± 0.05 VDC
Slope: ↑ (On) Slope: ↓ (Off)	Hysteresis Compensation Out (+ Slope)	U1-5	37	Fig 5.34	+2.4V ± 0.025 VDC +3.7V ± 0.025 VDC
Slope: ↑ (Off) Slope: ↓ (On)	− Slope Dr	U1-6	38	Fig 5.34	+0.82V ± 0.01 VDC +0.10V ± 0.01 VDC
Slope: ↑ (Off) Slope: ↓ (On)	− Slope Out	U1-8	39	Fig 5.34	+0.1V ± 0.02 VDC +4.5V ± 0.5 VDC
Funct: T1 (AV) Funct: FA	$\overline{TI \cdot TIA}$ Dr	U1-9	40	Fig 5.34	−6.67V ± 0.1 VDC −5.4V ± 0.1 VDC
		U1-10/13	41	Fig 5.34	−6.55V ± 0.05 VDC
		U1-12	42	Fig 5.34	−5.8V ± 0.05 VDC
Apply a 1Vp-p sinewave to Ch. A input.					Note: Externally trigger the oscilloscope "plus" to maintain the phase relationship through the signal conditioners.
Keyboard Sw: Slope: ↑ Coupling: AC					
Keyboard: T1 (or FA) TL, AU (Ch. A)					Note: Oscilloscope measurements are made with a X10 probe.
	Signal In	R1	A	Fig 5.34	Waveform #1
	Buffer Amp In	Q1a (Gate)	B	Fig 5.34	Waveform #2
	Sig Cond In	U3-8	C	Fig 5.34	Waveform #3
	1st Stage Sig Out	U3-7	D	Fig 5.34	Waveform #4
	1st Stage Ref Out	U3-6	E	Fig 5.34	Waveform #5
	2nd Stage Sig Out	U3-14	F	Fig 5.34	Waveform #6
	2nd Stage Ref Out	U3-13	G	Fig 5.34	Waveform #7
	Schmitt Trig Out (− Slope)	U2-7	H	Fig 5.34	Waveform #8
	Schmitt Trig Out (+ Slope)	U2-10	I	Fig 5.34	Waveform #9

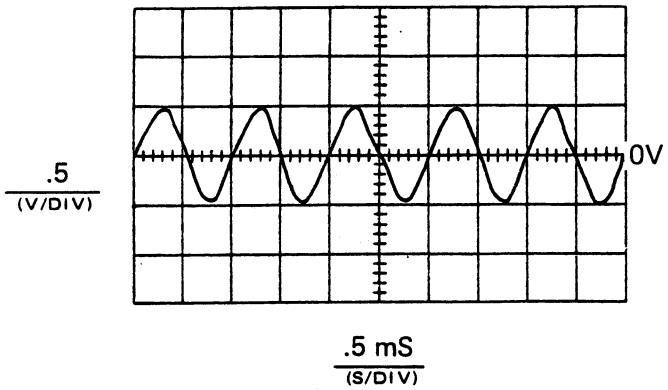
Table 5.28 - Signal Conditioner (Ch. A/Ch. B) Subassembly Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	+ Slope Output Drive Sig	U2-2	J	Fig 5.34	Waveform #10
	– Slope Output Drive Sig	U2-4	K	Fig 5.34	Waveform #11
	ECL Sig Out	U2-3	L	Fig 5.34	Waveform #12
Funct: FA Slope: ↑ (Ch. A)	Hysteresis Compensation	U1-1	M	Fig 5.34	Waveform #13
Funct: TI Slope: ↑ (Ch. A)					Waveform #14
Funct: TI Slope: ↓ (Ch. A)					Waveform #15
Funct: FA Slope: ↓ (Ch. A)	Hysteresis Compensation Output	U1-5	N	Fig 5.34	Waveform #16
Funct: T1 Slope: ↓ (Ch. A)					Waveform #17
Funct: T1 Slope: ↑					Waveform #18

WAVEFORMS FOR (CH A/CH B) SIGNAL CONDITIONER SUBASSEMBLY PERFORMANCE TEST

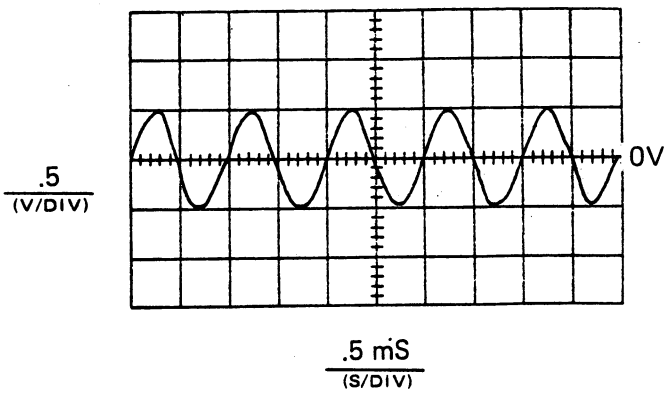
1 (NO.) R1

SIGNAL INPUT



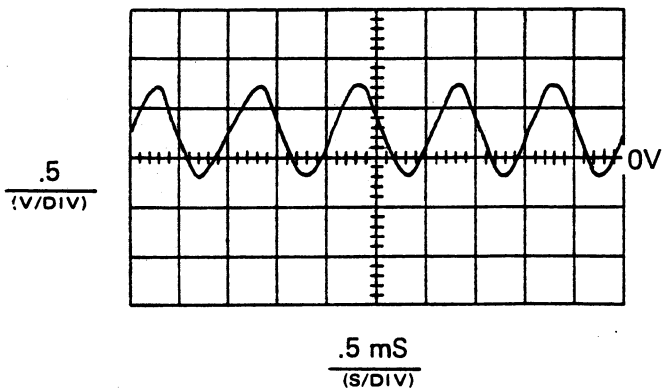
2 (NO.) Q1a (GATE)

AMP INPUT



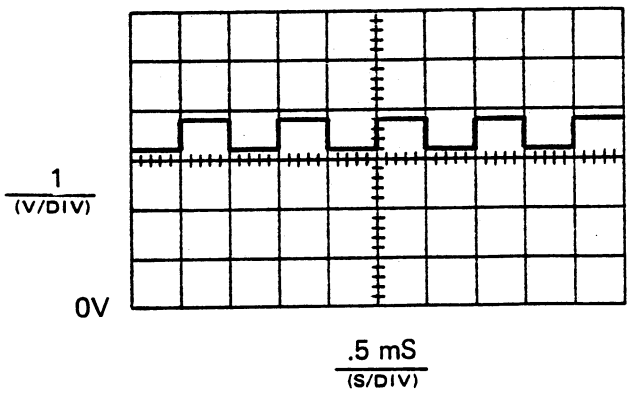
3 (NO.) U3-8

BUFFERED SIG COND INPUT



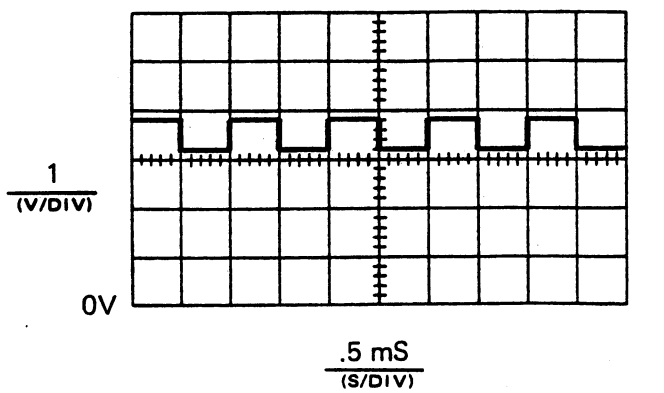
4 (NO.) U3-7

1ST STAG OUT (SIG)



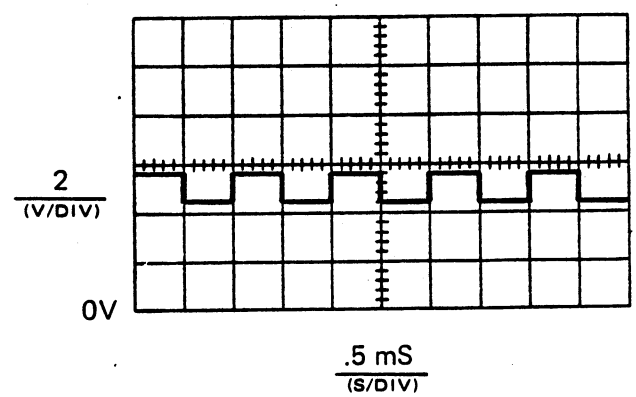
5 (NO.) U3-6

1ST STAGE OUT (REF)



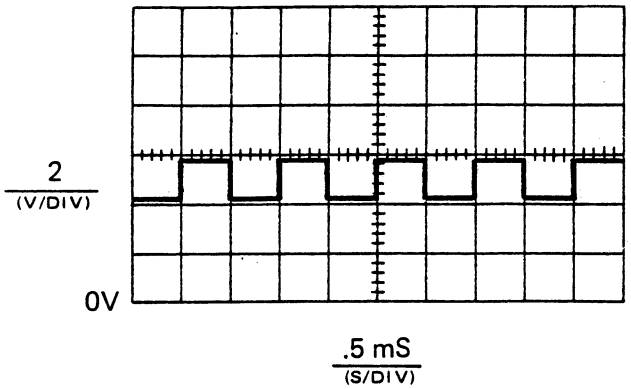
6 (NO.) U3-14

2ND STAGE OUT (SIG)



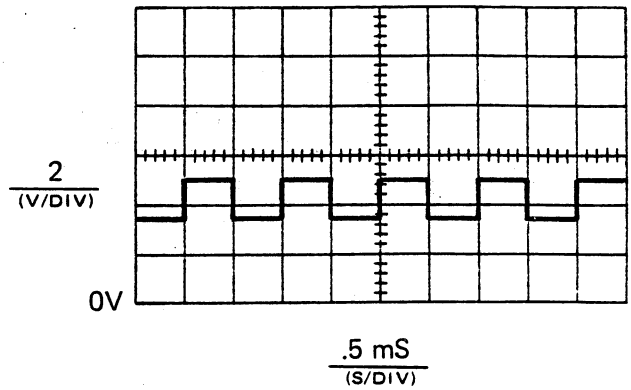
7 (NO.) U3-13

2ND STAGE OUT (REF)



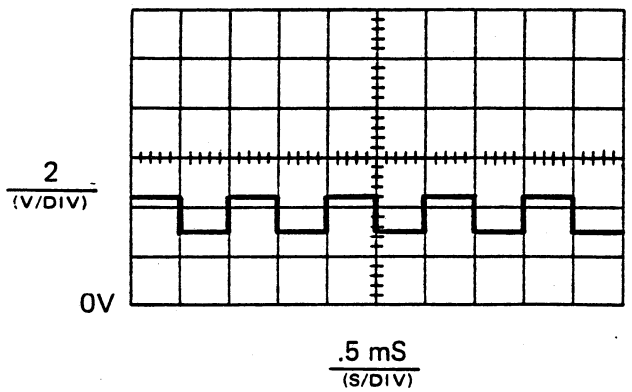
8 (NO.) U2-7

SCHMITT TRIG OUT (–)



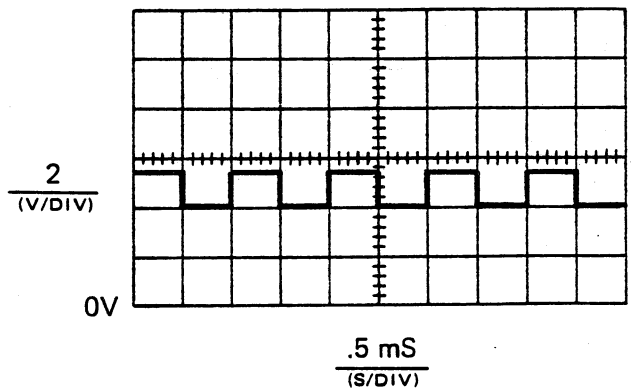
9 (NO.) U2-10

SCHMITT TRIG OUT (+)



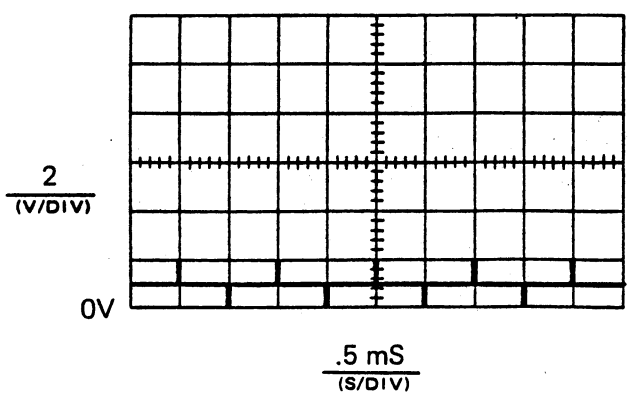
10 (NO.) U2-2

+ SCOPE SIG



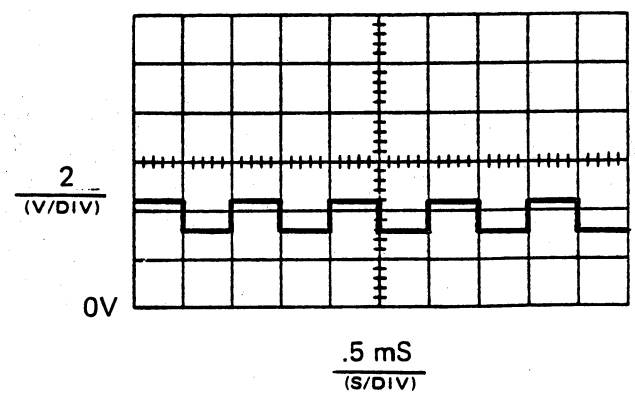
11 (NO.) U2-4

– SLOPE SIG



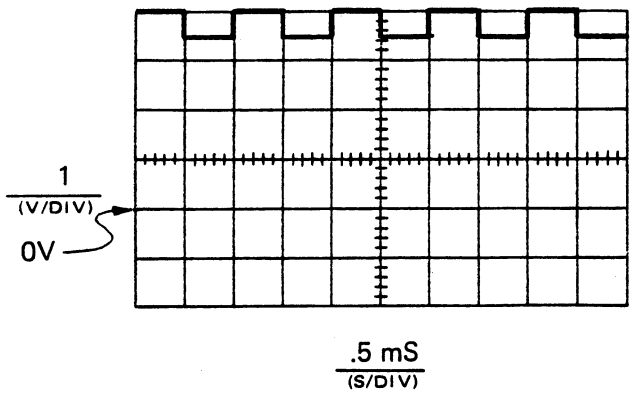
12 (NO.) U2-3

ECL SIG OUT



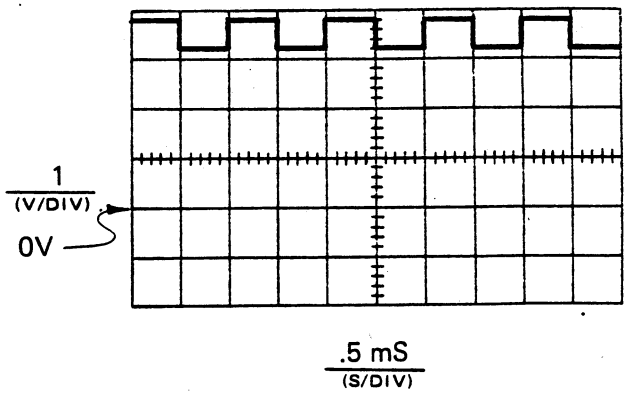
13 (NO.) U1-1

HYSTERESIS COMPENSATION OUTPUT (+ SLOPE)



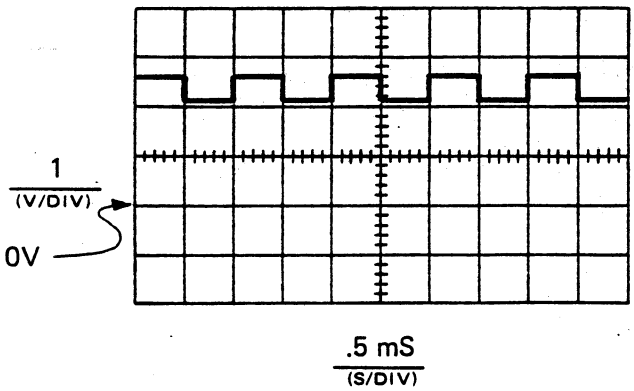
14 (NO.) U1-1

HYSTERESIS COMPENSATION OUTPUT (+ SLOPE)



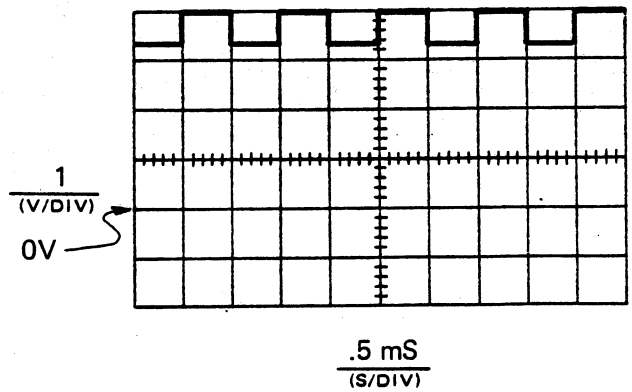
15 (NO.) U1-1

HYSTERESIS COMPENSATION OUTPUT (– SLOPE)



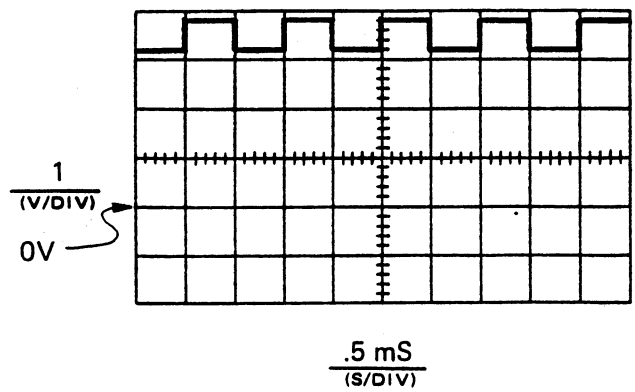
16 (NO.) U1-5

HYSTERESIS COMPENSATION OUTPUT (– SLOPE)



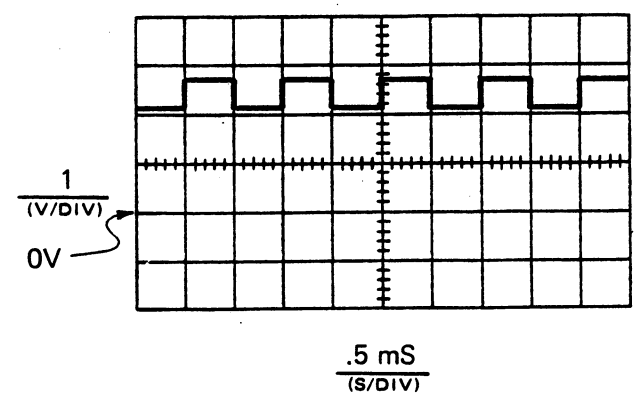
17 (NO.) U1-5

HYSTERESIS COMPENSATION OUTPUT (– SLOPE)



18 (NO.) U1-5

HYSTERESIS COMPENSATION OUTPUT (+ SLOPE)



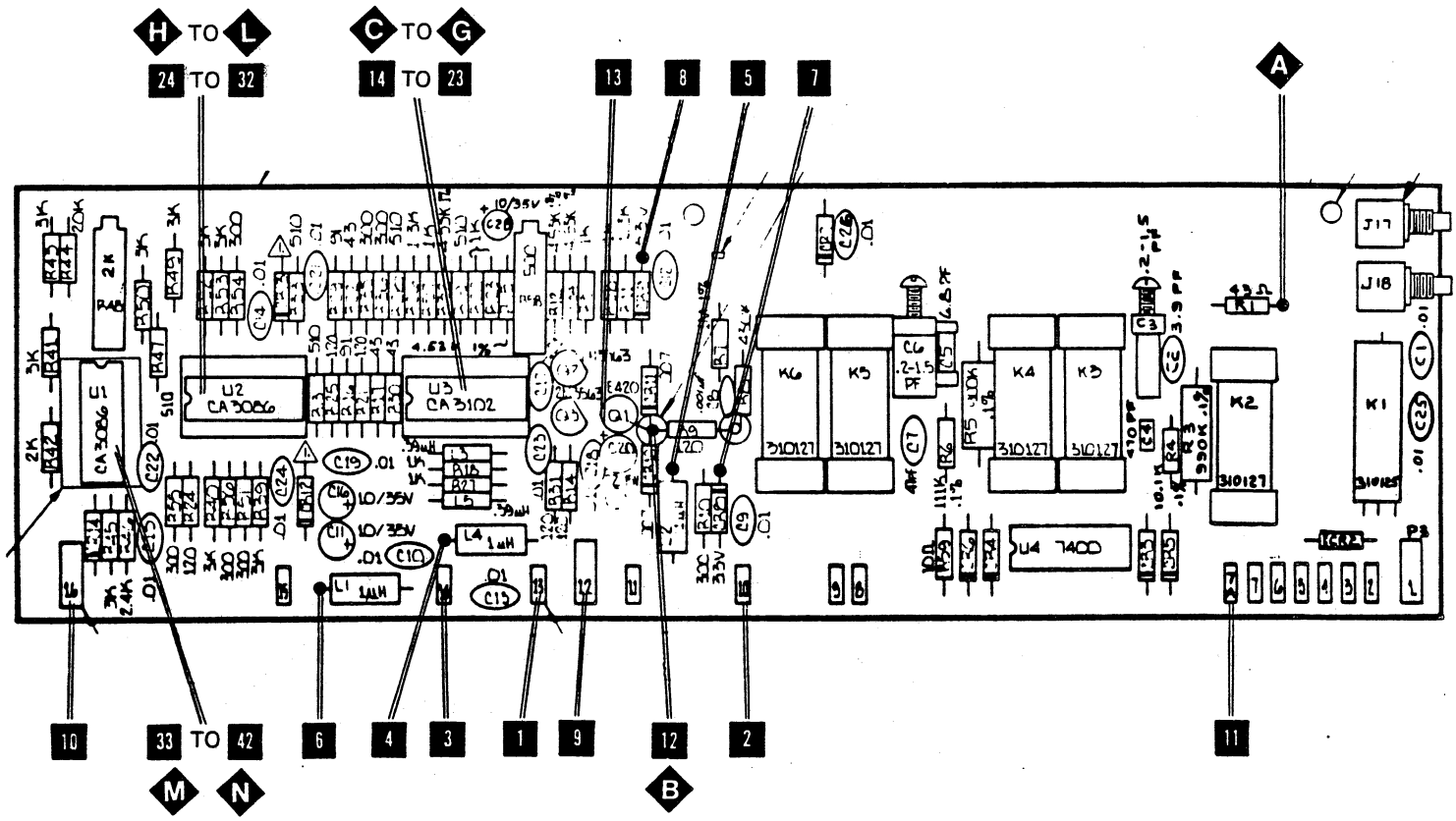


Figure 5.34 - Signal Conditioner (Ch A/Ch B) Subassembly Test Points

Table 5.29 - **Prescaler (FC) Subassembly Performance Test**

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
The prescaler assembly shield must be removed for test and installed on an extender PCB, P/N 406851. Check to insure that all pins are straight, well seated, and do not interfere assembly circuitry. Caution: When removing the assembly from its connector (J1), removing the shield, or reseating the assembly to the extender in the instrument; use extreme caution to avoid flexing or bending the PCB to prevent cracking the chip capacitors.					
Keyboard: FC Apply an input signal of 250 mV RMS, 100 to 500 MHz (Example used is 200 MHz)					Note: Measurements referenced to TP1.
					Note: Oscilloscope measurements must be made with a X10 input probe.
					Verify that the "in range" indicator is illuminated on the front panel.
	+12V Supply	P1-3	1	Fig 5.35	+11.9V ±0.1 VDC
	+5.4V Supply	P1-8	2	Fig 5.35	+5.35V ±0.025 VDC
	+5.2V Supply	P1-10	3	Fig 5.35	+5.2V ±0.05 VDC
	−12V Supply	P1-2	4	Fig 5.35	−11.7V ±0.1 VDC
Keyboard: TI Keyboard: FC	FC Enable (B1)	P1-6	5	Fig 5.35	+1.75V ±0.05 VDC +3.56V ±0.05 VDC
Signal: In Signal: Out	Attenuator Bias	R5	6	Fig 5.35	+6.6V ±0.05 VDC +7.5V ±0.05 VDC
Signal: In Signal: Out	Attenuator Bias	R7	7	Fig 5.35	+5.35V ±0.05 VDC +6.0V ±0.05 VDC
Signal: In Signal: Out	AGC Output	CR4 (Anode)	8	Fig 5.35	+5.1V ±0.05 VDC +8.0V ±0.05 VDC
Signal: In Signal: Out	Attenuator Bias	CR4 (Cathode)	9	Fig 5.35	+6.0V ±0.05 VDC +7.2V ±0.05 VDC
Signal: In Signal: Out	Pin Diode Bias	CR2,3,5 (Anodes)	10	Fig 5.35	+6.0V ±0.05 VDC +8.0V ±0.05 VDC
Signal: In Signal: Out	Voltage Level Trigger Input	Q3 (Base)	11	Fig 5.35	−.60V ±0.02 VDC +1.3V ±0.02 VDC

Table 5.29 - **Prescaler (FC) Subassembly Performance Test (continued)**

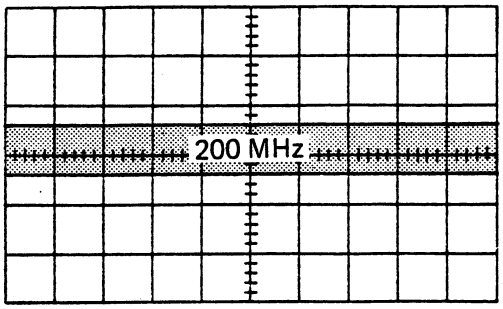
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Signal: In Signal: Out	Voltage Level Trigger Output	R29	12	Fig 5.35	+10.7V ± 0.05 VDC +1.1V ± 0.05 VDC
Keyboard: T1 Keyboard: FC	Voltage Level Trigger Enable	R23	13	Fig 5.35	+1.1V ± 0.05 VDC +0.60V ± 0.05 VDC
Keyboard: T1 Keyboard: FC	FC Enable Output	R23	14	Fig 5.35	+1.1V ± 0.05 VDC +0.03V ± 0.005 VDC
Signal: In Signal: Out	Voltage Level Output Drive	R25	15	Fig 5.35	+1.15V ± 0.01 VDC +0.12V ± 0.01 VDC
Signal: In Signal: Out	Voltage Level Trigger Output	R32	16	Fig 5.35	+2.3V ± 0.05 VDC +4.8V ± 0.05 VDC
Signal: In Signal: Out	ECL Output Enable	R35	17	Fig 5.35	+3.0V ± 0.05 VDC +4.5V ± 0.05 VDC
Signal: In Signal: Out	In Range Lite Drive	P1-7	18	Fig 5.35	+0.14V ± 0.01 VDC +3.7V ± 0.01 VDC
Signal: In Signal: Out	Diode Detector	TP2	19	Fig 5.35	+0.66V ± 0.01 VDC –0.27V ± 0.01 VDC
Signal: In Signal: Out	AGC Op Amp Input	R27	20	Fig 5.35	–0.001V ± 0.0002 VDC –0.9V ± 0.01 VDC
Signal: In Signal: Out	AGC Op Amp Output	R16	21	Fig 5.35	+4.2V ± 0.05 VDC +11.35V ± 0.05 VDC
Signal: In	Signal Input	F1/C2	A	Fig 5.35	Waveform #1
	1st RF Amp Out	U5-7	B	Fig 5.35	Waveform #2
	2nd RF Amp Out	U4-7	C	Fig 5.35	Waveform #3
	High Speed Divider Input	U2-10	D	Fig 5.35	Waveform #4
	High Speed Divider Output	U2-4	E	Fig 5.35	Waveform #5
	FC (ECL) Output	U3-15/P1-5	F	Fig 5.35	Waveform #6

WAVEFORMS FOR (FC) PRESCALER SUBASSEMBLY PERFORMANCE TEST

1 (NO.)

C2/F1

SIG IN



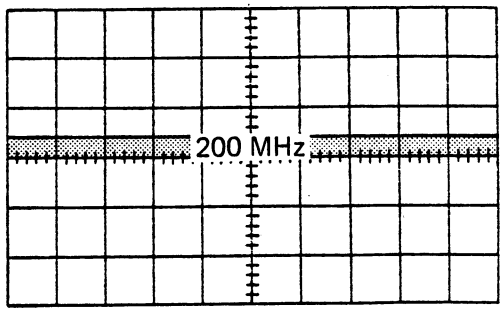
200mV (V/DIV)

.05 µS (S/DIV)

2 (NO.)

U5-7

1ST RF AMP OUT



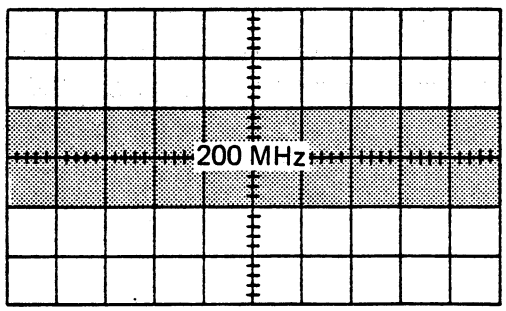
50mV (V/DIV)

.05 µS (S/DIV)

3 (NO.)

U4-7

2ND RF AMP OUT



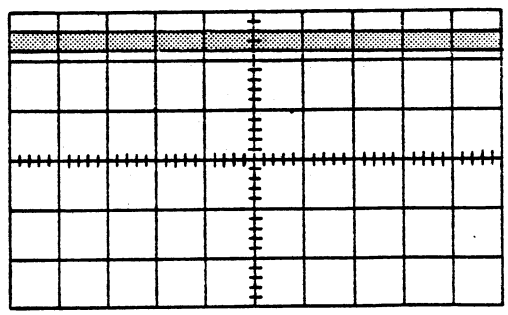
50mV (V/DIV)

.05 µS (S/DIV)

4 (NO.)

U2-10

HIGH SPEED ÷ 10 INPUT



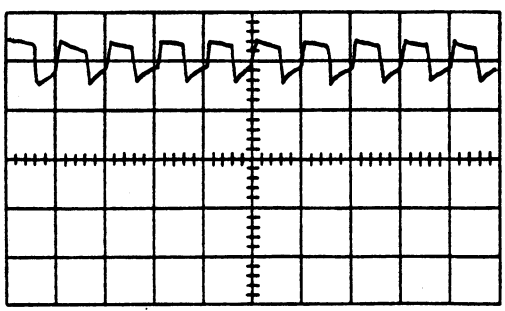
1V (V/DIV)

.05 µS (S/DIV)

5 (NO.)

U10-4

HIGH SPEED ÷ 10 OUTPUT (20 MHz)



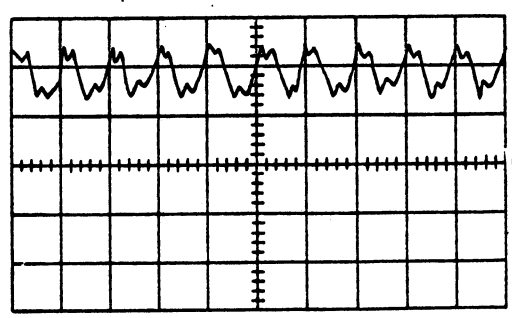
2V (V/DIV)

.05 µS (S/DIV)

6 (NO.)

U3-15

PRESCALER OUT (ECL) (20 MHz)



2V (V/DIV)

.05 µS (S/DIV)

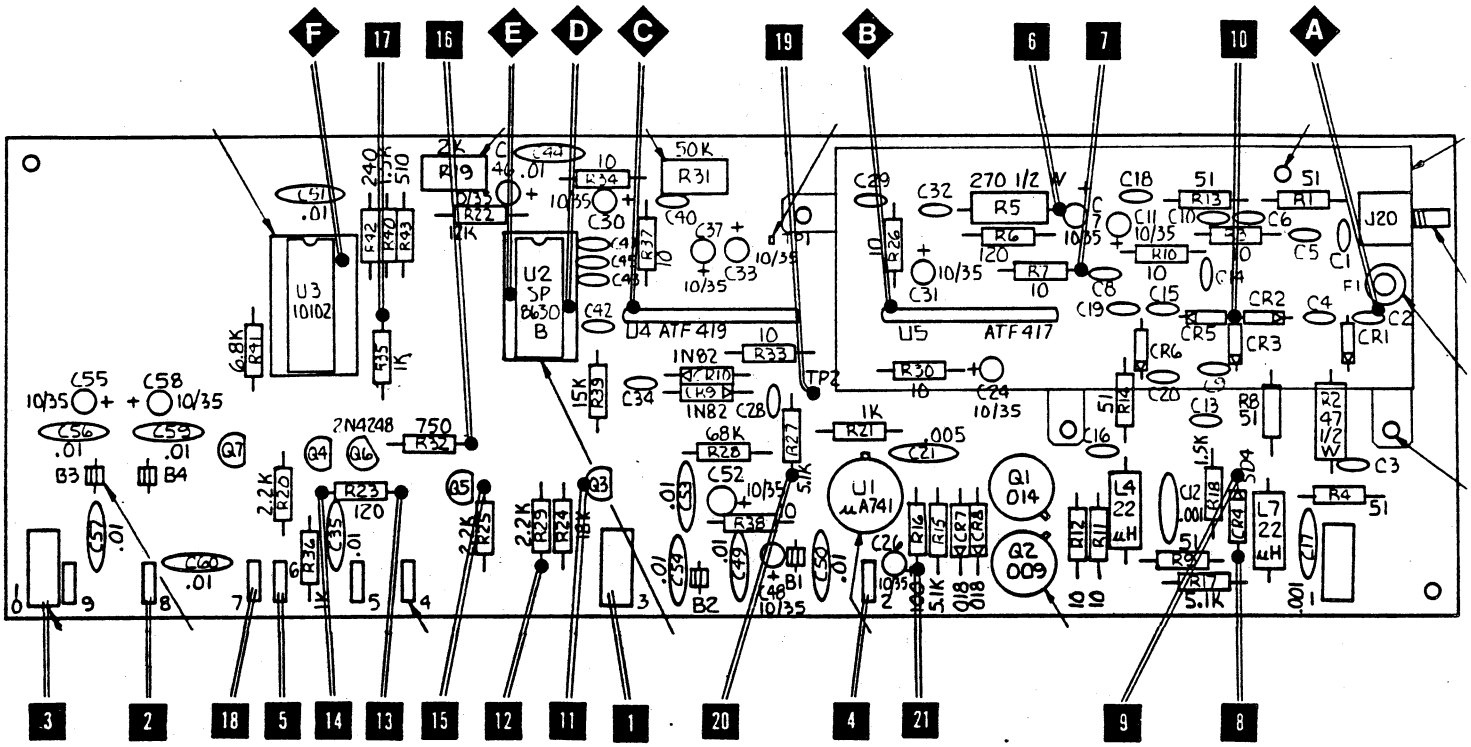


Figure 5.35 - Prescaler (FC) Subassembly Test Points

Table 5.30 - DAC Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Extend the DAC assembly with P/N 406852 extender PCB ass'y.					Note: Measurement reference is P2-5.
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Test (Ch. A) Slope: (Ch. A) Coupling: DC (Ch. B) Slope: (Ch. B) Coupling: DC					Note: Reference and temp compensation voltages are based on actual voltage measurements ± an allowable tolerance.
Power Switch: On					
Keyboard: (Ch. A) TL, 0, ., 0, 0, TL (Ch. B) TL, 0, ., 0, 0, TL					
	TTL Common	P2-3	1	Fig 5.36	–0.02V ± 0.005 VDC
	+12 VDC	P2-2	2	Fig 5.36	+11.9V ± 0.025 VDC
	+5.2 VDC	P2-6	3	Fig 5.36	+5.175V ± 0.025 VDC
	–12 VDC	P2-11	4	Fig 5.36	–11.7V ± 0.1 VDC
	Reference Voltage	U6-10, 12, 14	5	Fig 5.36	+0.7V ± 0.025 VDC
	Reference Voltage	U6-9, 11, 16	6	Fig 5.36	+1.4V ± 0.025 VDC
	Reference Voltage	U6-7, 8	7	Fig 5.36	+8.6V ± 0.05 VDC
	Reference Amp Out	U7-8, 9	8	Fig 5.36	+8.6V ± 0.05 VDC
	Voltage Divider	R19	9	Fig 5.36	+5.0V ± 0.05 VDC
	Voltage Divider	R20	10	Fig 5.36	+3.7V ± 0.05 VDC
	Divider Output	U7-1, 2	11	Fig 5.36	+3.7V ± 0.05 VDC
	Ch. A MSB Switch Drive	U1-1, 2	12	Fig 5.36	+3.75V ± 0.005 VDC
	Ch. A MSB Switch Base Bias	U6-2	13	Fig 5.36	+0.8V ± 0.025 VDC
	Ch. A MSB Switch Output Drive	U6-1	14	Fig 5.36	+0.07V ± 0.005 VDC
	Ch. A MSB Bias	R13	15	Fig 5.36	+3.7V ± 0.01 VDC

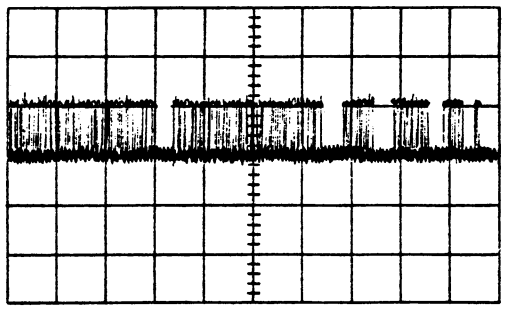
Table 5.30 - DAC Subassembly Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Ch. B MSB Switch Drive	U3-1, 2	16	Fig 5.36	+3.75V ± 0.005 VDC
	Ch. B MSB Switch Base Bias	U6-4	17	Fig 5.36	+0.8V ± 0.025 VDC
	Ch. B MSB Switch Output Drive	U6-5	18	Fig 5.36	+0.07V ± 0.005 VDC
	Ch. B MSB Bias	R18	19	Fig 5.36	+3.7V ± 0.01 VDC
	Ch. A DAC + Ref	U4-14	20	Fig 5.36	0V ± 0.0005 VDC
	Ch. A Summing Amp Minus Input	U7-13	21	Fig 5.36	0V ± 0.002 VDC
	Ch. A Summing Amp Plus Input	U7-12	22	Fig 5.36	0V ± 0.0005 VDC
	Ch. A Summing Amp Output	U7-14	23	Fig 5.36	+0.65 ± 0.01 VDC
	Ch. A Trigger Level Output	W-1	24	Fig 5.36	0V ± 0.005 VDC
	Ch. B DAC + Ref	U5-14	25	Fig 5.36	0V ± 0.0005 VDC
	Ch. B Summing Amp Minus Input	U7-6	26	Fig 5.36	0V ± 0.002 VDC
	Ch. B Summing Amp Plus Input	U7-5	27	Fig 5.36	0V ± 0.0005 VDC
	Ch. B Summing Amp Output	U7-7	28	Fig 5.36	+0.65V ± 0.01 VDC
	Ch. B Trigger Level Output	W-2	29	Fig 5.36	0V ± 0.005 VDC
	Trigger Level Output Drive Bias	R28	30	Fig 5.36	+4.9V ± 0.025 VDC
Keyboard: Ch. A: TL, AU	Ch. A Clock	P2-10	A	Fig 5.36	Waveform #1
	Ch. A Data	P2-9	B	Fig 5.36	Waveform #2
Keyboard: Ch. B: TL, AU	Ch. B Clock	P2-7	C	Fig 5.36	Waveform #3
	Ch. B Data	P2-8	D	Fig 5.36	Waveform #4
Check the Ch. A and Ch. B shift register outputs, as necessary to determine trigger level output capability at U1 and U3. See Table 5.31.					

WAVEFORMS FOR DAC SUBASSEMBLY PERFORMANCE TEST

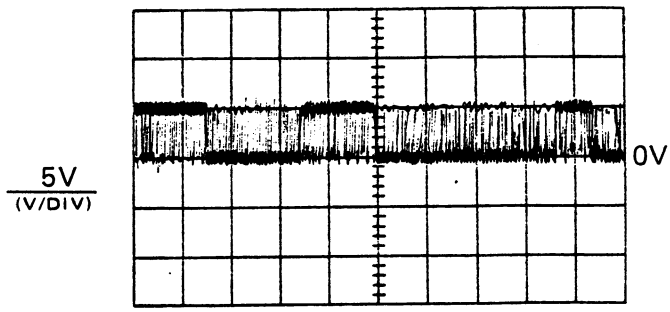
1 (NO.) P2-10

CH A CLOCK



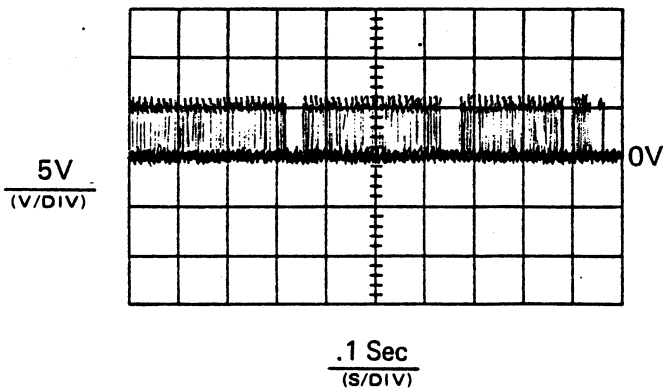
2 (NO.) P2-9

CH A DATA



3 (NO.) P2-7

CH B CLOCK



4 (NO.) P2-8

CH B DATA

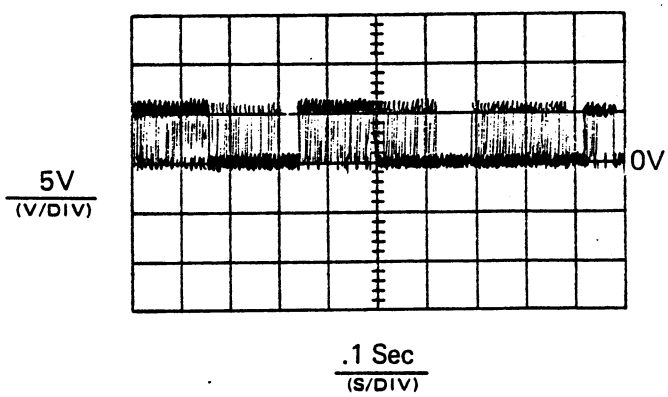


Table 5.31 - DAC Shift Register Logic Output Codes

	10	11	12	13	3	4	5	6	1/2
3.19	1	1	1	1	1	1	1	1	1
3.00	0	0	0	0	1	1	1	1	↓
2.00	↓	↓	↓	0	0	1	0	1	↓
1.00	↓	↓	↓	0	1	0	1	0	↓
0.90	↓	↓	↓	1	0	0	1	↓	↓
0.80	↓	↓	↓	0	0	0	1	↓	↓
0.70	↓	↓	↓	1	1	1	0	↓	↓
0.60	↓	↓	↓	0	1	1	0	↓	↓
0.50	↓	↓	↓	1	0	1	0	↓	↓
0.40	↓	↓	↓	0	0	1	0	↓	↓
0.30	↓	↓	↓	1	1	0	0	↓	↓
0.20	↓	↓	↓	0	1	0	0	↓	↓
0.10	↓	↓	↓	1	0	0	0	↓	↓
0.09	1	1	1	0	0	0	0	↓	↓
0.08	0	1	1	↓	↓	↓	↓	↓	↓
0.07	0	1	1	↓	↓	↓	↓	↓	↓
0.06	1	0	1	↓	↓	↓	↓	↓	↓
0.05	0	0	1	↓	↓	↓	↓	↓	↓
0.04	1	1	0	↓	↓	↓	↓	↓	↓
0.03	0	1	0	↓	↓	↓	↓	↓	↓
0.02	0	1	0	↓	↓	↓	↓	↓	↓
0.01	1	0	0	↓	↓	↓	↓	↓	↓
0.00	0	0	0	↓	↓	↓	↓	↓	↓
−0.01	1	1	1	1	1	1	1	1	0
−0.02	0	1	1	↓	↓	↓	↓	↓	↓
−0.03	0	1	1	↓	↓	↓	↓	↓	↓
−0.04	1	0	1	↓	↓	↓	↓	↓	↓
−0.05	0	0	1	↓	↓	↓	↓	↓	↓
−0.06	1	1	0	↓	↓	↓	↓	↓	↓
−0.07	0	1	0	↓	↓	↓	↓	↓	↓
−0.08	0	1	0	↓	↓	↓	↓	↓	↓
−0.09	1	0	0	↓	↓	↓	↓	↓	↓
−0.10	0	0	0	1	1	1	1	↓	↓
−0.20	↓	↓	↓	0	1	1	1	↓	↓
−0.30	↓	↓	↓	1	0	1	1	↓	↓
−0.40	↓	↓	↓	0	0	1	1	↓	↓
−0.50	↓	↓	↓	1	1	0	1	↓	↓
−0.60	↓	↓	↓	0	1	0	1	↓	↓
−0.70	↓	↓	↓	1	0	0	1	↓	↓
−0.80	↓	↓	↓	0	0	0	1	↓	↓
−0.90	↓	↓	↓	1	1	1	0	↓	↓
−1.00	↓	↓	↓	0	1	1	0	↓	↓
−2.00	↓	↓	↓	0	0	1	1	0	↓
−3.00	↓	↓	↓	0	1	0	0	0	↓
−3.20	↓	↓	↓	0	0	0	0	0	↓

U1 (U3) Ch. A (Ch. B)

1 = +4.5V ± 0.025 VDC

0 = +0.08V ± 0.005 VDC

Note: Output trigger level voltage is the same as Ch. A/Ch. B status reading ± 0.0125 VDC.

Note: Manual trigger level settings are entered by enabling the desired trigger level (Ch. A or Ch. B) keyboard switch, enabling the desired value, and enabling the same Ch. A or Ch. B "TL" switch again.

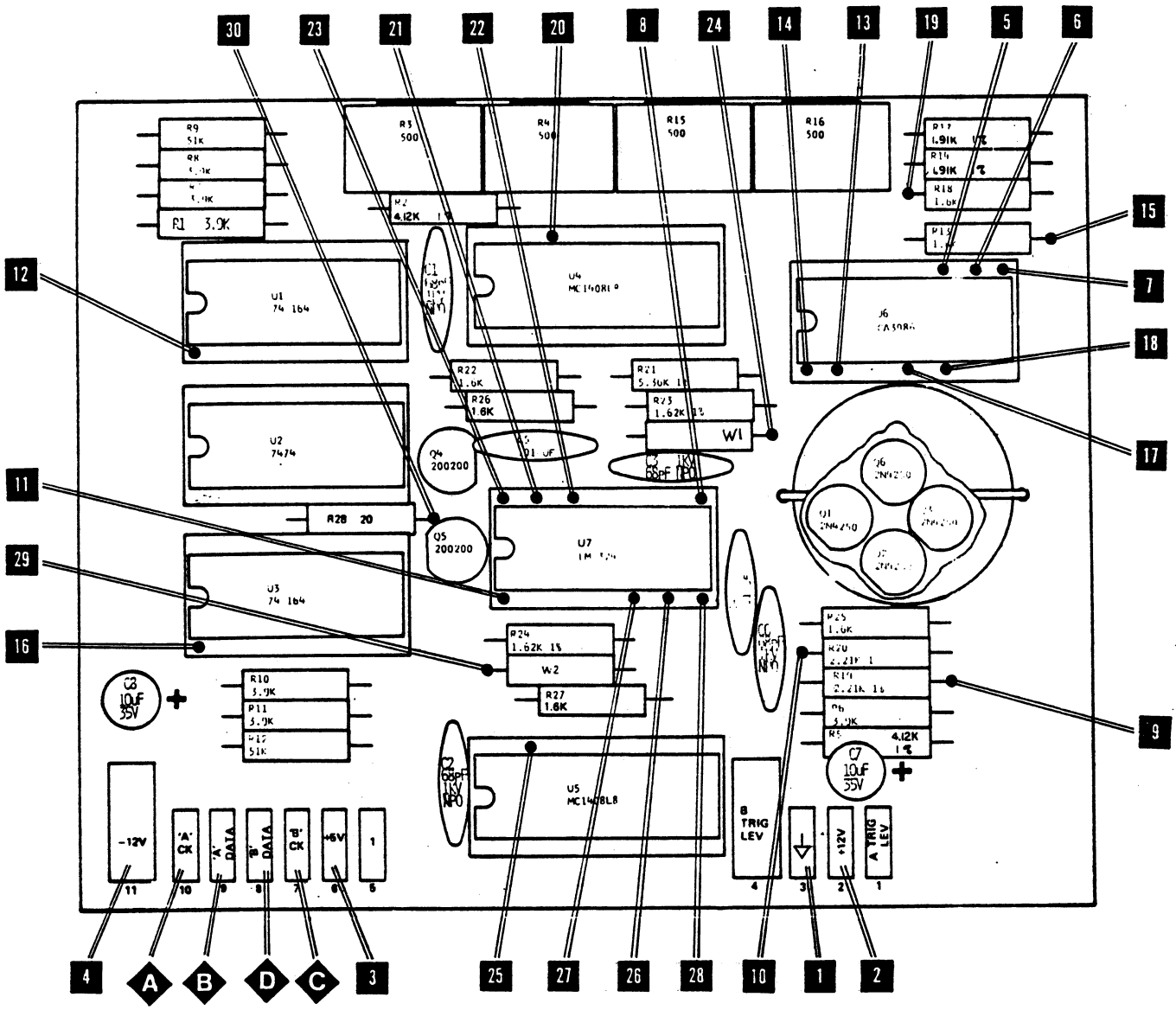


Figure 5.36 - DAC Subassembly Test Points

Table 5.32 - **Reference Subassembly Performance Test**

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Extend the reference assembly with P/N 406853 PCB extender assembly.					Note: Measurement reference is ECL ground @ TP1
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Test (Ch. A) Slope: ↑ Coupling: DC (Ch. B) Slope: ↓ Coupling: DC					
Power Switch: On					
Keyboard: Ch. A: TL,0,.,0,0,TL Ch. B: TL,0,.,0,0,TL					
	+12V Supply	P5-5	1	Fig 5.37	+11.9V ± 0.025 VDC
	+5.2V Supply	P5-3	2	Fig 5.37	+5.2V ± 0.025 VDC
	+5V Supply	P5-6	3	Fig 5.37	+5V ± 0.05 VDC
	–12V Supply	P5-10	4	Fig 5.37	–11.7V ± 0.025 VDC
	Signal Shaper Input (Lo)	U1-1	5	Fig 5.37	+1.35V ± 0.025 VDC
	Signal Shaper Output (Lo)	U1-8	6	Fig 5.37	+0.07V ± 0.005 VDC
	10 MHz Filter Input	R4	7	Fig 5.37	+0.9V ± 0.01 VDC
	10 MHz Filter DC Collector Bias	R7	8	Fig 5.37	+3.0V ± 0.05 VDC
	Filter Emitter Bias	R8	9	Fig 5.37	+0.17V ± 0.01 VDC
	Filter Bias	R12	10	Fig 5.37	–8.7V ± 0.05 VDC
	Filter Bias	R11	11	Fig 5.37	–0.35V ± 0.01 VDC
	Filter Bias	R13	12	Fig 5.37	–1.1V ± 0.025 VDC
	Filter Output	L1	13	Fig 5.37	+4.9V ± 0.05 VDC
	Signal Detector Input	CR2 (Cathode)	14	Fig 5.37	–0.19V ± 0.01 VDC
	Detector Bias	R19	15	Fig 5.37	–0.75V ± 0.01 VDC

Table 5.32 - Reference Subassembly Performance Test (continued)

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Detector Bias	CR5 (Anode)	16	Fig 5.37	+0.7V ± 0.01 VDC
	Detector Signal Output	CR5 (Cathode)	17	Fig 5.37	+4.9V ± 0.05 VDC
	Detector Logic Output (Lo)	U2-4/5	18	Fig 5.37	+0.18V ± 0.01 VDC
	Gate Output	U2-6	19	Fig 5.37	+3.9V ± 0.05 VDC
	Internal Ref Gate Out	U2-2	20	Fig 5.37	+1.1V ± 0.025 VDC
	X5 Multiplier Input	R20	21	Fig 5.37	0V ± 0.001 VDC
	Multiplier 1st Stage Output	L-2	22	Fig 5.37	+5.2V ± 0.05 VDC
	Multiplier Bias	R21	23	Fig 5.37	0V ± 0.005 VDC
	Multiplier Bias	R23	24	Fig 5.37	–0.56V ± 0.01 VDC
	Multiplier Output	TP2	25	Fig 5.37	+4.9V ± 0.025 VDC
	X2 Multiplier Input	R24	26	Fig 5.37	–4.0V ± 0.05 VDC
	Multiplier Bias	R24	27	Fig 5.37	–4.0V ± 0.05 VDC
	Multiplier Bias	R28	28	Fig 5.37	–4.7V ± 0.025 VDC
	Multiplier Bias	L3	29	Fig 5.37	–0.0005V ± 0.001 VDC
	Multiplier Bias	L5	30	Fig 5.37	–0.005V ± 0.001 VDC
	Multiplier Bias	R26	31	Fig 5.37	+0.45 ± 0.025 VDC
	Multiplier Bias	R29	32	Fig 5.37	–4.0V ± 0.05 VDC
	Multiplier Output	L4	33	Fig 5.37	+5.17V ± 0.005 VDC
	Buffer Input	R31	34	Fig 5.37	–0.1V ± 0.005 VDC
	Buffer Bias	R32	35	Fig 5.37	–0.5V ± 0.025 VDC
	Buffer Output	R33	36	Fig 5.37	+4.5V ± 0.025 VDC
	Driver Output	TP3	37	Fig 5.37	+3.8V ± 0.025 VDC

Table 5.32 - Reference Subassembly Performance Test (continued)

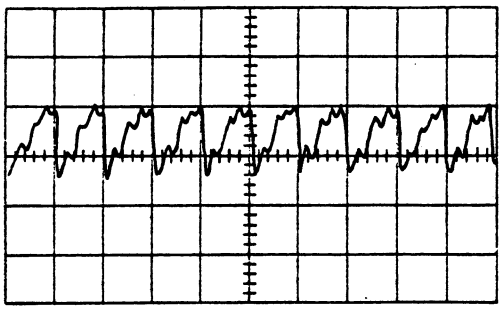
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Internal Ref. Input	U2-12	A	Fig 5.37	Waveform #1
	Internal Ref. Gate Output	U2-11	B	Fig 5.37	Waveform #2
	Detector Gate Output	U2-3	C	Fig 5.37	Waveform #3
	10 MHz Output	U2-8	D	Fig 5.37	Waveform #4
	X5 Freq Multiplier 1st Stage Output	L2	E	Fig 5.37	Waveform #5
	X5 Freq Multiplier Output	TP2	F	Fig 5.37	Waveform #6
	Buffer Input	R33	G	Fig 5.37	Waveform #7
	Driver Output	TP3	H	Fig 5.37	Waveform #8
Connect a 1V RMS 1 MHz (10 ppm) input on the rear panel @ J203. Verify the ext ref lite is annunciated on the front panel.	Signal Shaper Input	U1-1	I	Fig 5.37	Waveform #9
	Signal Shaper Output	U1-8	J	Fig 5.37	Waveform #10
	Detector Signal Output	CR5 (Cathode)	K	Fig 5.37	Waveform #11
	Detector Logic Output (Hi)	U2-4/5	18	Fig 5.37	+4.87V ± 0.025 VDC
	Gate Output	U2-6	19	Fig 5.37	+0.3V ± 0.025 VDC
	Internal Ref Gate Out	U2-2	20	Fig 5.37	+4.0V ± 0.05 VDC

WAVEFORMS FOR REFERENCE SUBASSEMBLY PERFORMANCE TEST

1 (NO.)

U2-12

10 MHz IN



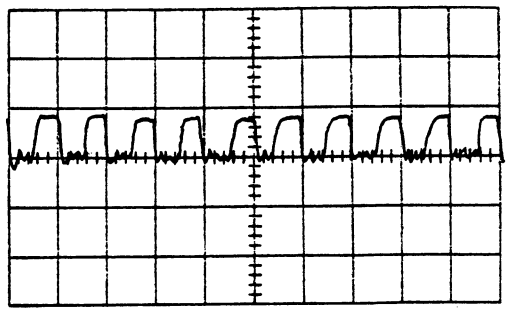
5V (V/DIV)

.1 μS (S/DIV)

2 (NO.)

U2-11

INTERNAL REF GATE OUT



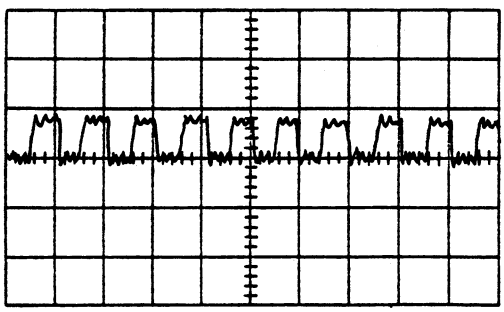
5 (V/DIV)

.1 μS (S/DIV)

3 (NO.)

U2-3

DETECTOR GATE OUTPUT



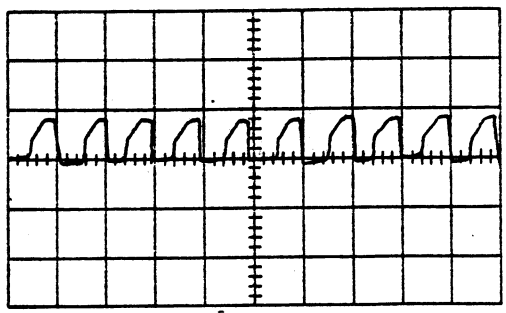
5 (V/DIV)

.1 μS (S/DIV)

4 (NO.)

U2-8

10 MHz OUTPUT



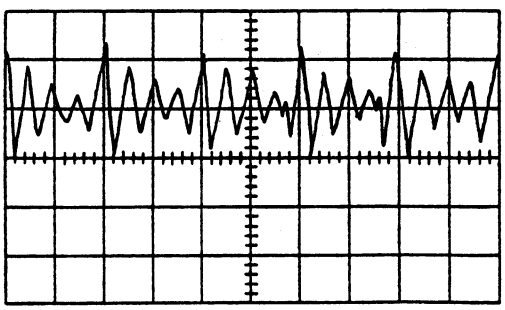
5 (V/DIV)

.1 μS (S/DIV)

5 (NO.)

L2

X5 FREQ MULT 1ST STAGE OUTPUT



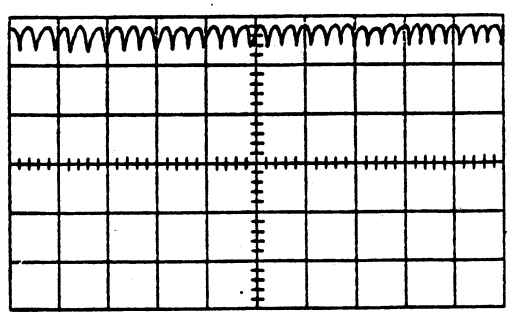
5 (V/DIV)

.05 μS (S/DIV)

6 (NO.)

TP2

X5 FREQ MULT OUTPUT (50 MHz)

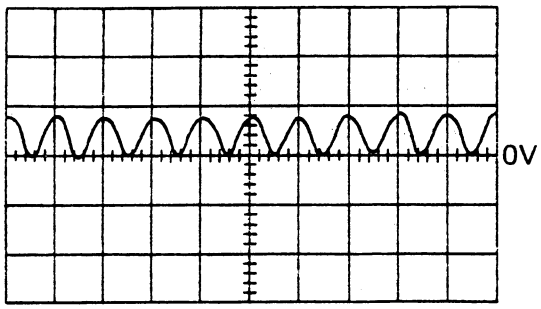


2 (V/DIV)

.05 μS (S/DIV)

7 (NO.) R31

BUFFER INPUT (100 MHz)



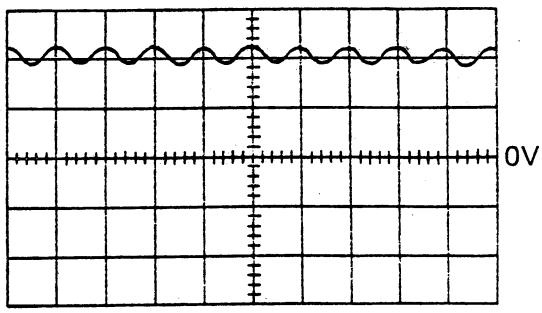
1 (V/DIV)

.1 μS (S/DIV)

USE HORIZ X10 SWEEP

8 (NO.) TP3

DRIVER OUTPUT (100 MHz)



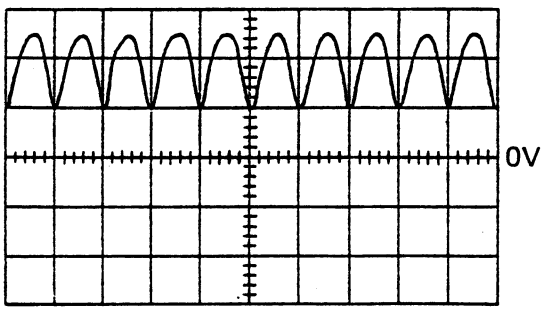
2 (V/DIV)

.1 μS (S/DIV)

USE HORIZ X10 SWEEP

9 (NO.) U1-1

(EXT REF IN) SIGNAL SHAPER INPUT

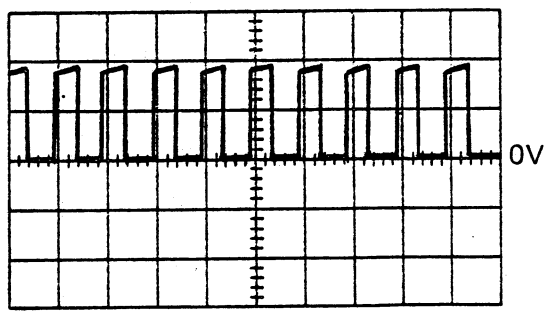


1 (V/DIV)

1 μS (S/DIV)

10 (NO.) U1-8

SIGNAL SHAPER OUTPUT

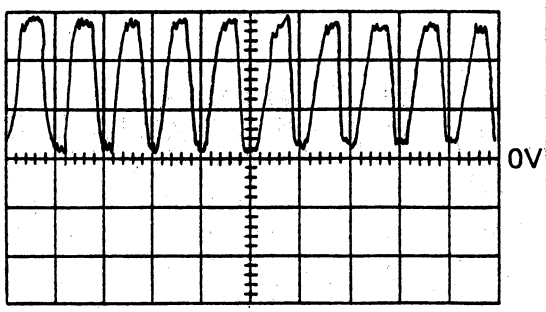


2 (V/DIV)

1 μS (S/DIV)

11 (NO.) CR5 (CATHODE)

DETECTOR SIGNAL OUTPUT



2 (V/DIV)

1 μS (S/DIV)

USE HORIZ X10 SWEEP

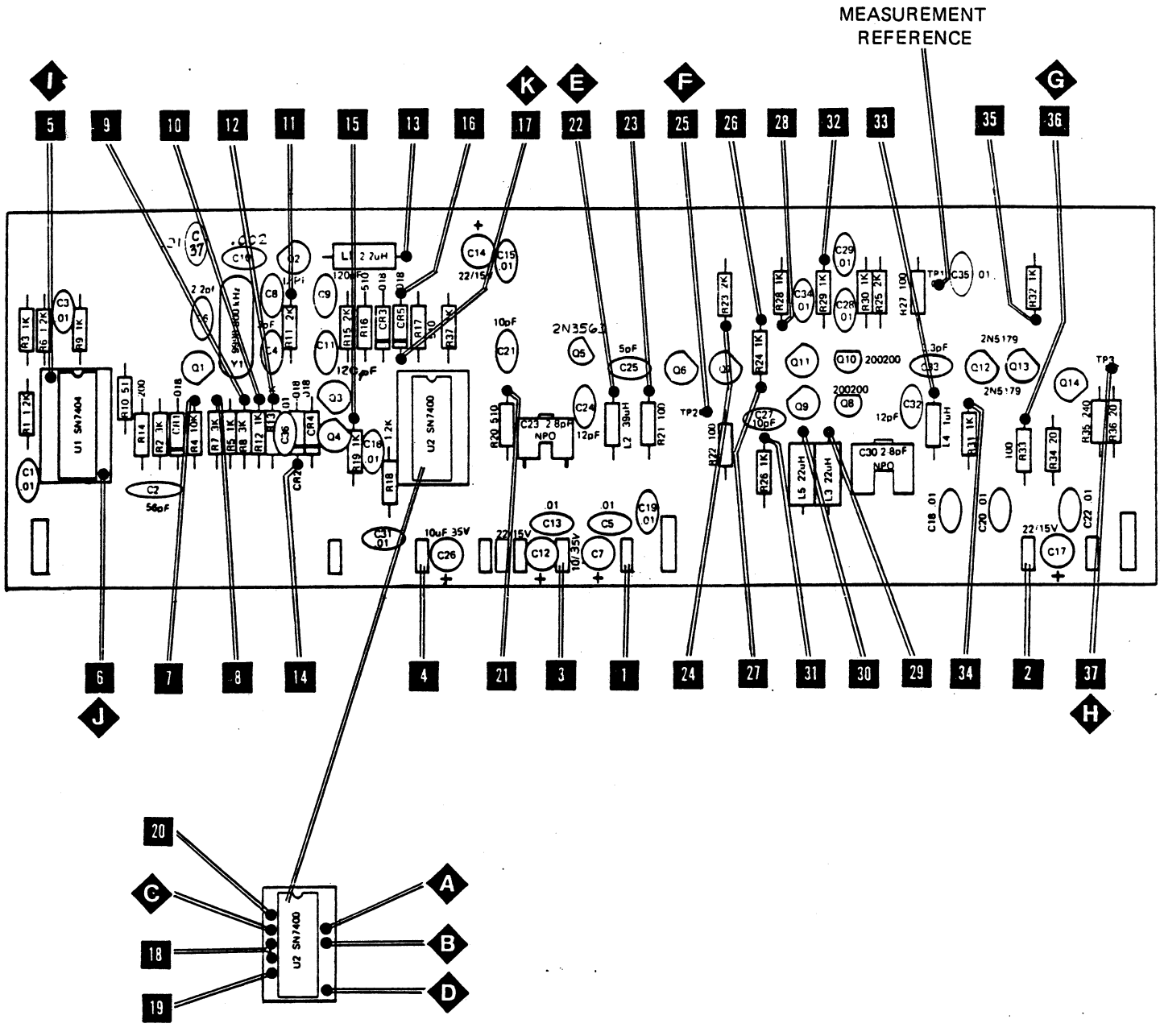


Figure 5.37 - Reference Subassembly Test Points

Table 5.33 - Option (22/24) Oscillator Power Supply (Regulator) Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
When the instrument is connected to line voltage, the power supply (regulator) produces +28 VDC to allow the Reference Oscillator (Option 22 or 24) the necessary voltage to provide an output of 10 MHz, whether or not the 9000A main power switch is on or off, to minimize oscillator stability when the 9000A is "in use". Note: The unit can be extended for test on P/N 406852, DAC/Opt OSC extender PCB. The input cable at P21 does not have the required service loop to provide input power when the unit is extended. This must be done with clip lead jumpers. Because of the transformer weight, extra support may be necessary. Warning: The AC power cord must be disconnected from the 9000A when handling this assembly to avoid harmful electrical shock. Note: DC voltage are referenced to J10-1.					
Remove AC Line Cord and Assembly	Primary Resistance (120V)	P21 Pins 1&3	1	Fig 5.38	63Ω ± 5Ω
	Primary Resistance (230V)	P21 Pins 1&3	1	Fig 5.38	255Ω ± 20Ω
	Secondary Resistance	T2 Pins 5&6	2	Fig 5.38	9Ω ± 1Ω
Complete Installation Apply Line Power	Secondary AC V (115 VAC)	T2 Pins 5&6	2	Fig 5.38	35.5 VAC ± 2 VAC
	Rectified Output	C1 (Plus)	3	Fig 5.38	+45.0V ± 1.0 VDC (100mVp-p Ripple)
	Regulated Output	J10-2	4	Fig 5.38	+28.0V ± 0.05 VDC (15mVp-p Ripple)

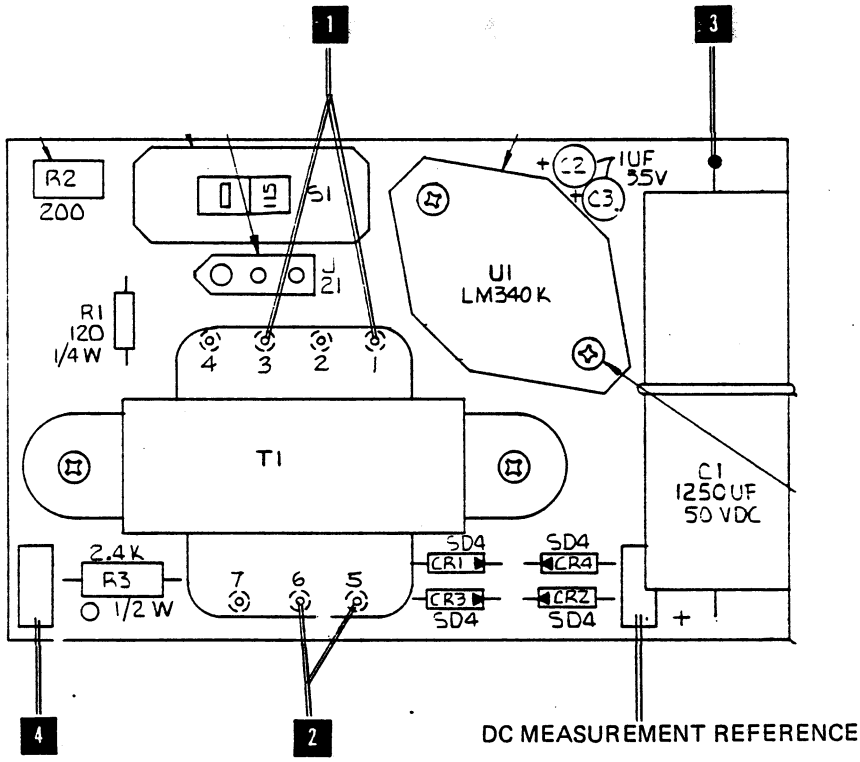


Figure 5.38 - Option (22/24) Power Supply (Regulator) Test Points

Table 5.34 - Control Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
The control assembly can only be tested to the point where certain "Knowns" can be verified. If the proper waveforms are not observed, a factory tested assembly or CPU, RAM, and specially "Masked" ROM must be retained as replacement spares.					
Extend the assembly with P/N 406855 card assembly.					Note: Measurement reference is made at CR11 Anode on the main logic board.
Control assembly necessitates insuring that the circuit side does not come in contact with the 9000A frame (common).					
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Test Ch. A Slope: ↑ Ch. A Coupling: DC Ch. B Slope: ↓ Ch. B Coupling: DC					
Power Switch: On		Test Points Shown On Figure 5.39			
	+5V Supply	P8-1	1		+5V ± 0.25 Vdc
	−12V Supply	P8-47	2		−12V ± 0.5 Vdc
	10 MHz Clock	P8-49	A		Waveform No. 1
Use internal trig. on the scope.	μP Clk	U3-39	B		Waveform No. 2
	VMA 02	U2-6	C		Waveform No. 3
	$\overline{R/W}$	U6-2	D		Waveform No. 4
	BVMA	U13-17	E		Waveform No. 5
	B $R/\overline{W}$	U13-11	F		Waveform No. 6
	B02	U13-5	G		Waveform No. 7
	BA0	U13-15	H		See Note Below
	BA1	U13-7	I		" "
	BA2	U13-13	J		" "
	BA3	U13-9	K		" "

Table 5.34 - Control Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Address Bus	U3 - Pins 13 to 20 and 22 to 25	L		See Note Below
	Data Bus	U12 - Pins 12 to 19	M		See Note Below

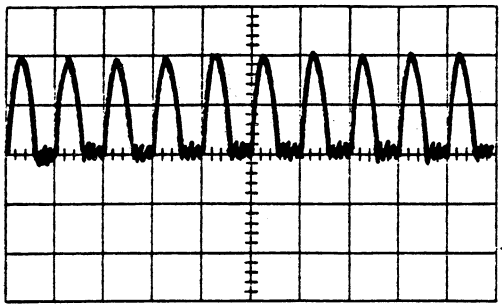
Note: These waveforms are asynchronous TTL signals. If the signals are always High or Low at these points, it is an indication of a Fault.

WAVEFORMS FOR CONTROL SUBASSEMBLY PERFORMANCE TEST

1 (NO.)

P8-49

10 MHz CLOCK



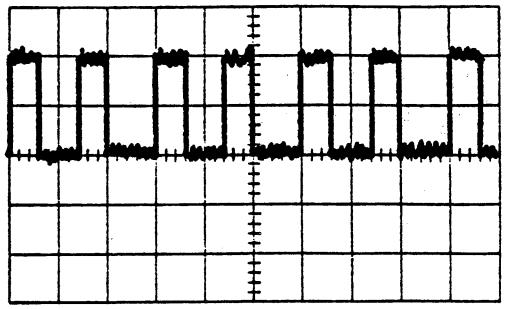
2V (V/DIV)

.1 μSEC (S/DIV)

2 (NO.)

U3-39

μP CLOCK IN



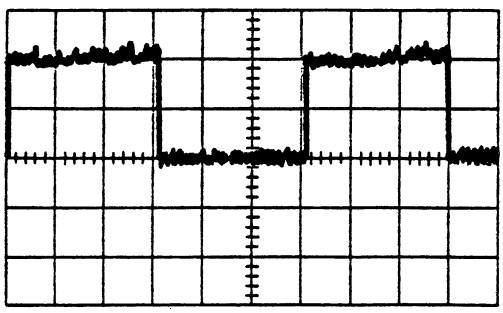
2V (V/DIV)

.2 μSEC (S/DIV)

3 (NO.)

U2-6

VMA.02



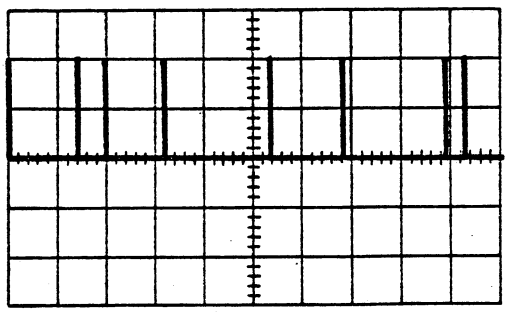
2V (V/DIV)

.2 μSEC (S/DIV)

4 (NO.)

U6-2

R/W



2V (V/DIV)

20 μSEC (S/DIV)

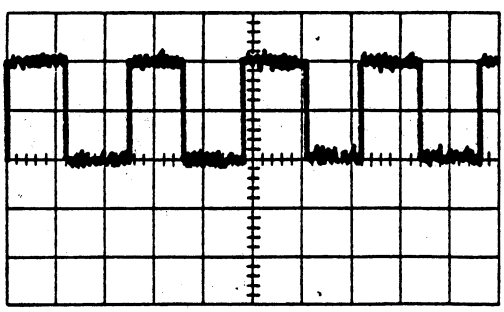
2.5 μSEC PULSES

POSITION OF PULSES WILL VARY

7 (NO.)

U13-5

B02



2V (V/DIV)

.5 μSEC (S/DIV)

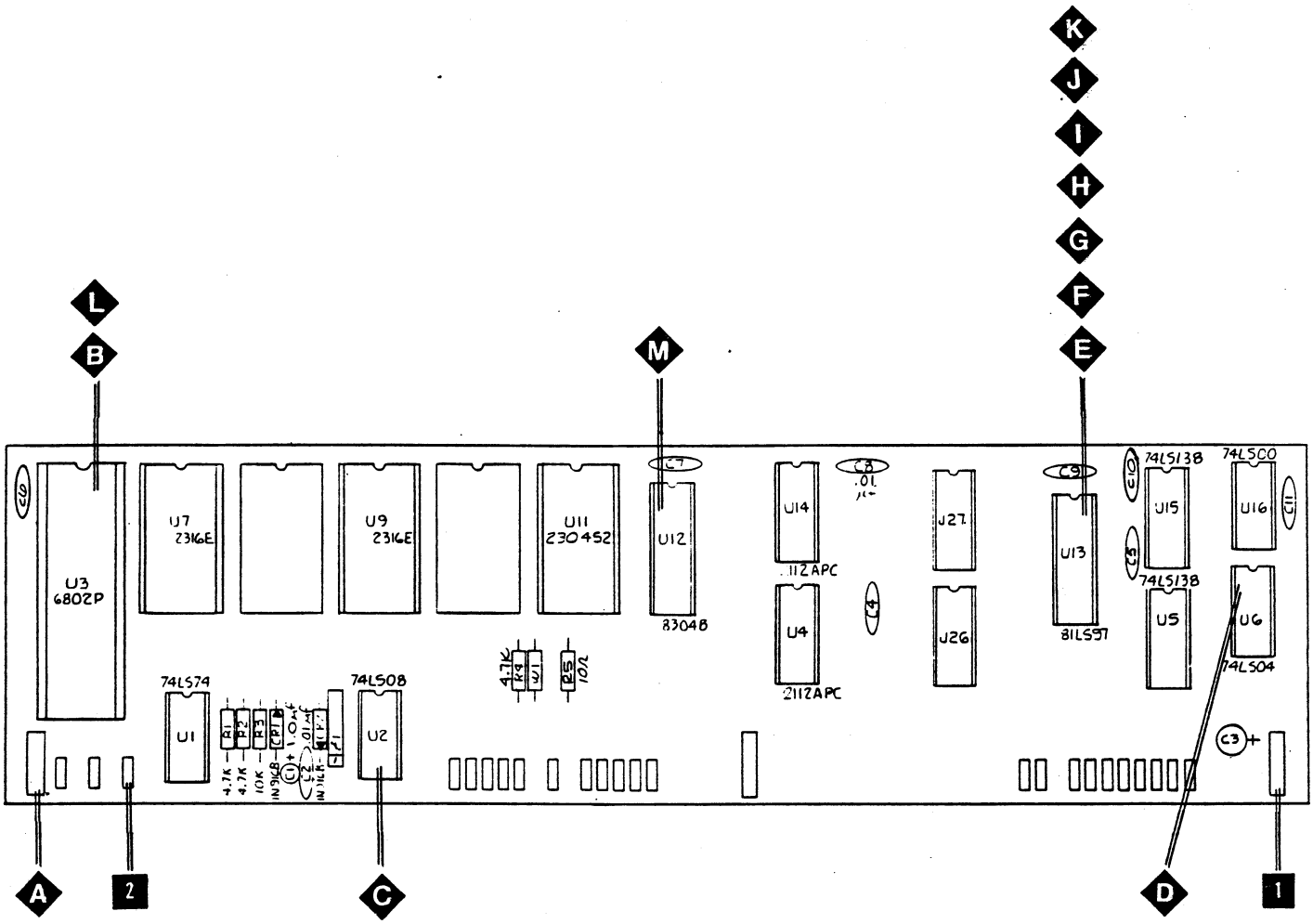


Figure 5.39 - Control PCB Assy 406925

Table 5.35 - I/O Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
The I/O assembly can only be tested to the point where certain "Knowns" can be verified. If responses to keyboard entries, made through the control assembly, do not result in valid data on the display; the unit must be exchanged with a factory tested assembly or CPU, RAM, and specially "Masked" ROMS must be retained as replacement spares.					
Extend the assembly with P/N 406855 card assembly.					Note: Measurement reference is made Anode, CR11 on the main logic board.
Caution: Be careful of the interconnection cables from I/O to the display and programmable pulse parameter assemblies. The weight of the I/O assembly necessitates insuring that the circuit side does not come in contact with the 9000A frame (common).					
Keyboard Switches: Norm/Hold: Norm Sep/Test/Com: Test Ch. A Slope: ↑ Ch. A Coupling: DC Ch. B Slope: ↓ Ch. B Coupling: DC					
Power Switch: On		Test Points Shown On Figure 5.40			
Internal Trigger	+5	P7-1	1		5 ± 0.25 Vdc
	−12	P7-78	2		−12 ± 0.5 Vdc
	10 MHz	U3-15	A		Waveform No. 2A
	5 MHz	U3-13	B		Waveform No. 3A
	MF ACC Clock	U1-9	C		Waveform No. 1A
Use as external trigger for scope	M.F. ACC Data	U7-2	D		Waveform No. 1
Use external trigger on the scope	QA	U15-3	E		Waveform No. 2
	QB	U15-2	F		Waveform No. 3
	QC	U15-6	G		Waveform No. 4
	QD	U15-7	H		Waveform No. 5

Table 5.35 - I/O Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	RAM IN (D3)	U14-12	I		Waveform No. 6
	RAM IN (D2)	U14-10	J		Waveform No. 6
	RAM IN (D1)	U14-6	K		Waveform No. 7
	RAM IN D0	U14-4	L		Waveform No. 8
	$\overline{S2}$	U14-3	M		Waveform No. 9
	RAM IN D3	U13-12	N		Waveform No. 10
	RAM IN D2	U13-10	O		Waveform No. 6
	RAM IN D1	U13-6	P		Waveform No. 10
	RAM IN D0	U13-4	Q		Waveform No. 10
	RAM OUT 0C	U14-9	R		Waveform No. 11
	RAM OUT 0D	U14-11	S		Waveform No. 13
	RAM OUT 0B	U14-7	T		Waveform No. 12
	RAM OUT 0A	U14-5	U		Waveform No. 14
	RAM OUT 1C	U13-9	V		Waveform No. 15
	RAM OUT 1D	U13-11	W		Waveform No. 15
	RAM OUT 1B	U13-7	X		Waveform No. 16
	RAM OUT 1A	U13-5	Y		Waveform No. 17
Keyboard Response .,ſl,FA,TI,8,4,4,0,	Input 1A	U6-2	Z		Waveform No. 18
CS,ſ,FC,P,9,5,1	Input 2A	U6-1B	a		Waveform No. 18
RS,TL(A),RA,AV,6.2,	Input 4A	U6-4	b		Waveform No. 18
AV,TL(B),ł,1/X,7	Input 6A	U6-16	c		Waveform No. 18
Ch A,/Ch B Coupling	Input 1B	U6-6	d		TTL Level Change
RM	Input RM	U6-14	e		TTL Level Change
Ch A/Ch B Slope	Input 4B	U6-8	f		TTL Level Change
Test/Com	Input 8B	U6-12	g		TTL Level Change

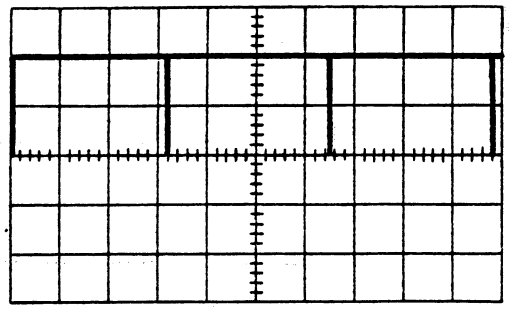
Table 5.35 - I/O Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Keyboard Switch to Com, Apply a 1V Scope Signal to Ch. A @ 1KHz.					
Keyboard "⎍"	$\overline{\text{Gate B}}$	U7-4	h		Waveform No. 19
Keyboard "⎍"	$\overline{\text{Data Ready}}$	U7-16	i		Waveform No. 20
Keyboard "⎍"	$\overline{\text{Gate A}}$	U7-18	j		Waveform No. 19
Keyboard "IT"	$\overline{\text{KY BD DATA}}$	U10-15	k		Waveform No. 21
	$\overline{\text{KYBD ENABLE}}$	U10-9	l		TTL Low
Keyboard "IT"	$\overline{\text{KYBD CLK}}$	U10-6	m		Waveform No. 22
Keyboard "IT"	$\overline{\text{PARALLEL ENABLE}}$	U10-16	n		Waveform No. 23
Keyboard "TI"	Control Reg. Clk	U1-12	o		Waveform No. 24
Keyboard "TI"	Control Reg. Data	U10-18	p		Waveform No. 25

WAVEFORMS FOR I/O SUBASSEMBLY PERFORMANCE TEST

1A (NO.) U1-9

MF ACC CLOCK

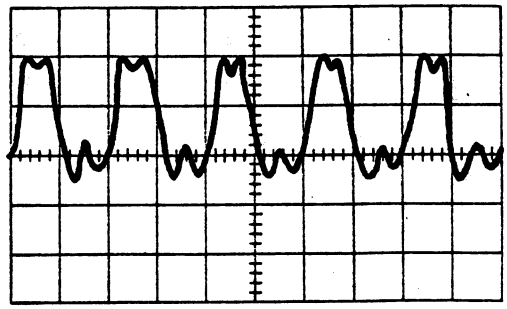


2V (V/DIV)

10 μSEC (S/DIV)

2A (NO.) U3-15

10 MHz

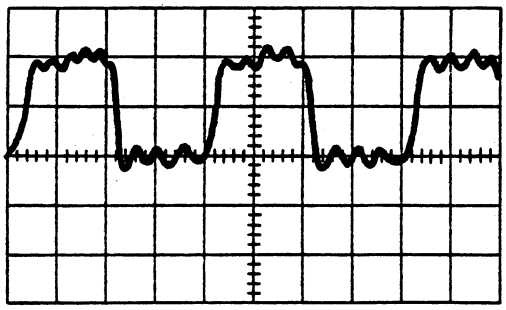


2V (V/DIV)

.05 μSEC (S/DIV)

3A (NO.) U3-13

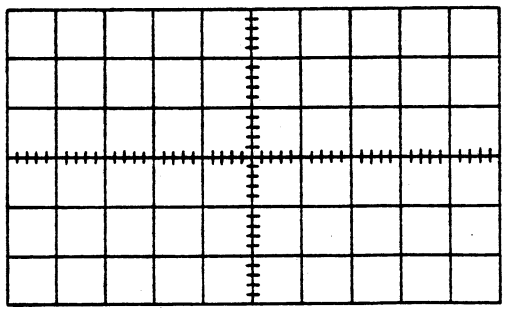
5 MHz



2V (V/DIV)

.05 μSEC (S/DIV)

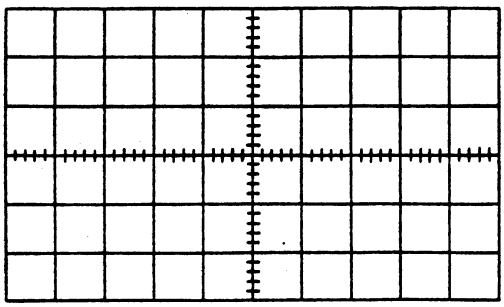
(NO.)



(V/DIV)

(S/DIV)

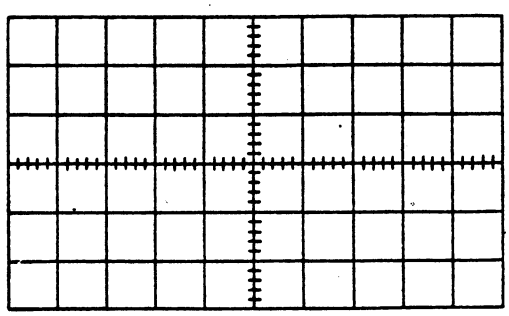
(NO.)



(V/DIV)

(S/DIV)

(NO.)



(V/DIV)

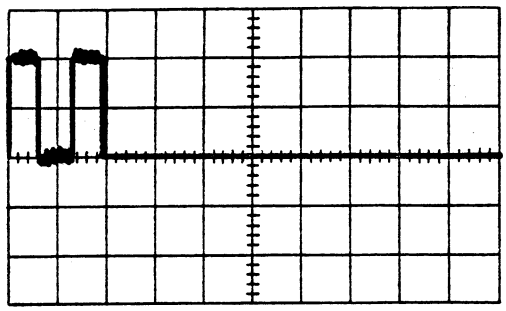
(S/DIV)

WAVEFORMS FOR I/O SUBASSEMBLY PERFORMANCE TEST Continued

1 (NO.)

U7-2

M.F. ACC DATA



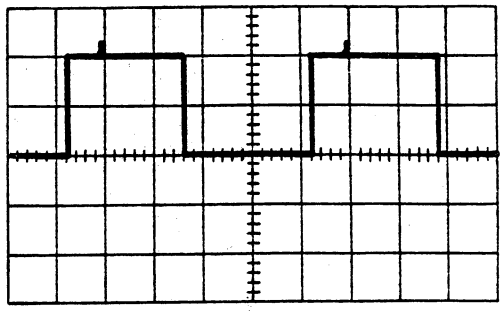
2V (V/DIV)

50 µSEC (S/DIV)

2 (NO.)

U15-3

QA



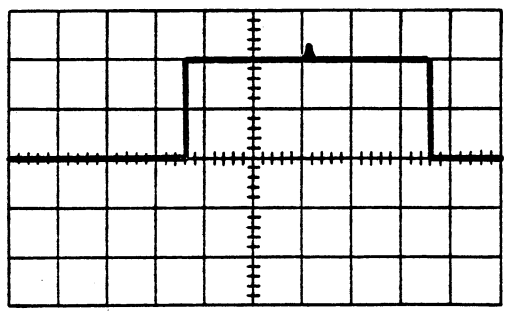
2V (V/DIV)

50 µSEC (S/DIV)

3 (NO.)

U15-2

QB



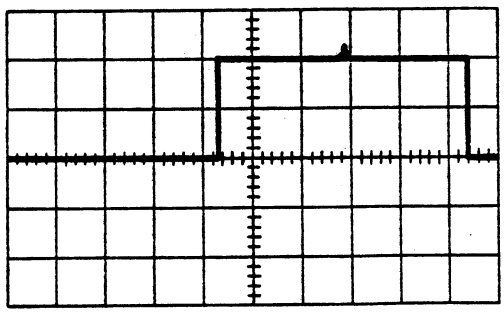
2V (V/DIV)

50 µSEC (S/DIV)

4 (NO.)

U15-6

QC



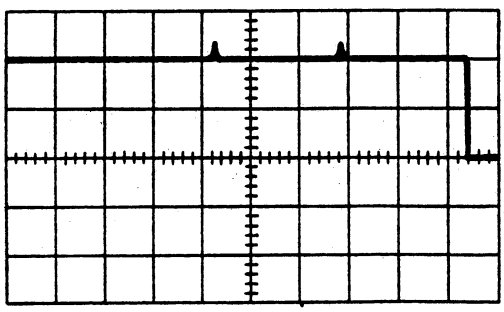
2V (V/DIV)

.1 MSEC (S/DIV)

5 (NO.)

U15-7

QD

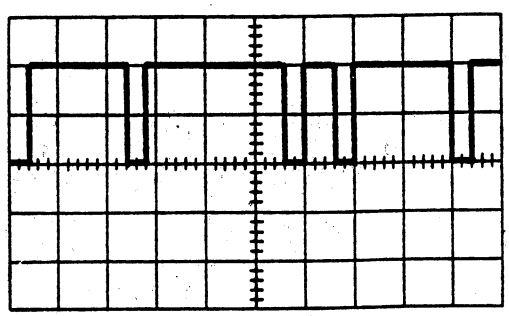


2V (V/DIV)

.1 MSEC (S/DIV)

6 (NO.)

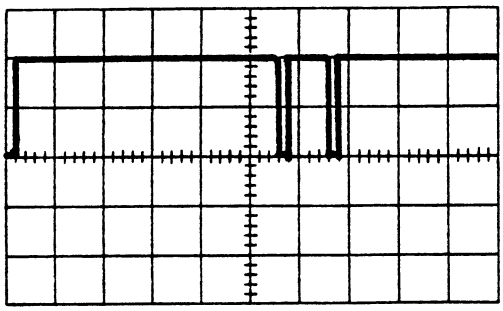
U14-12 & U14-10 & U13-10



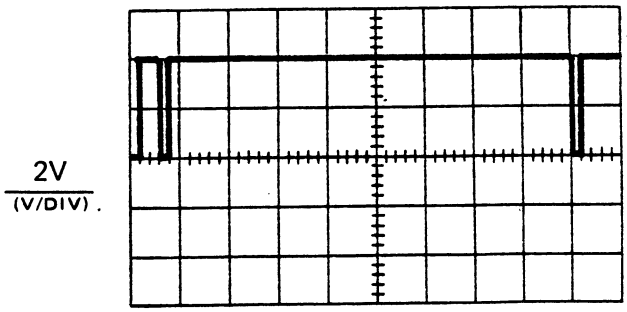
2V (V/DIV)

5 µSEC (S/DIV)

7 (NO.) U14-6

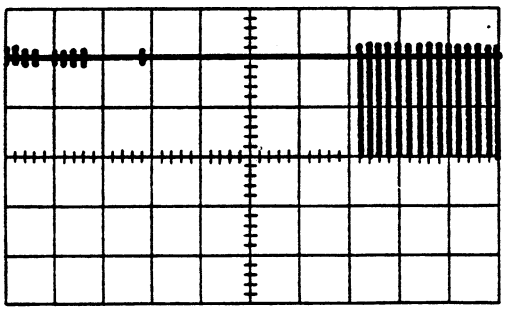


8 (NO.) U14-4

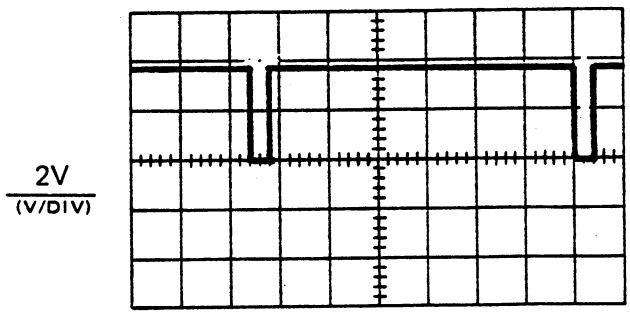


9 (NO.) U14-3

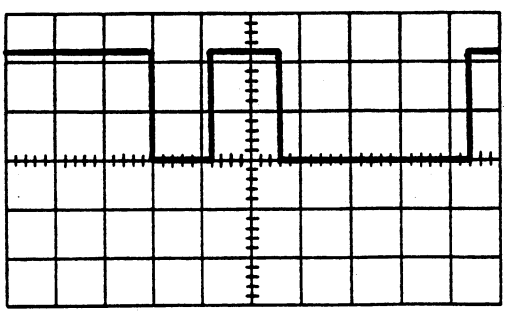
$\overline{S2}$



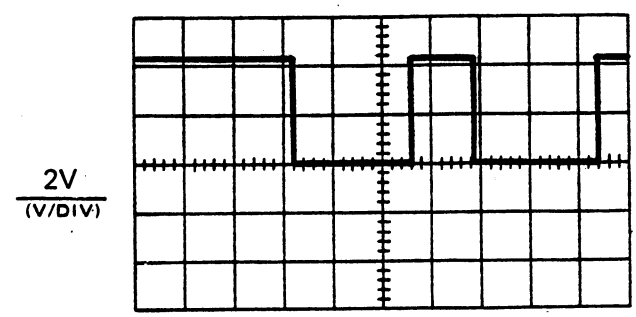
10 (NO.) U13-12 & U13-6 & U13-4



11 (NO.) U14-9

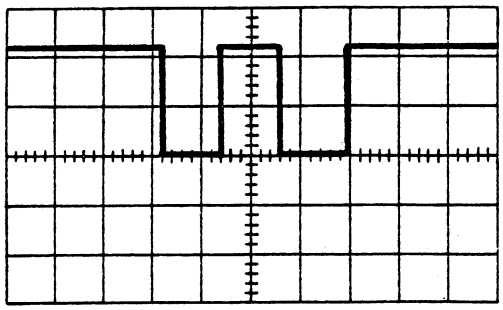


12 (NO.) U14-7



WAVEFORMS FOR I/O SUBASSEMBLY PERFORMANCE TEST Continued

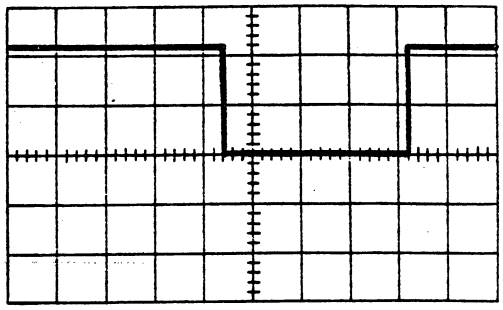
13 (NO.) U14-11



2V (V/DIV)

.1 MSEC (S/DIV)

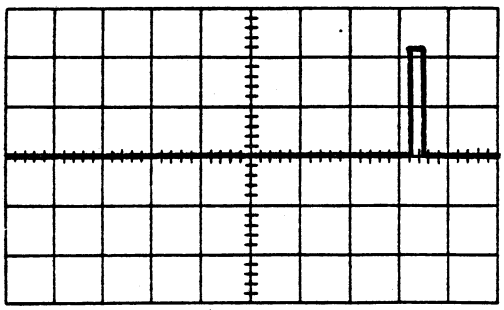
14 (NO.) U14-5



2V (V/DIV)

.1 μSEC (S/DIV)

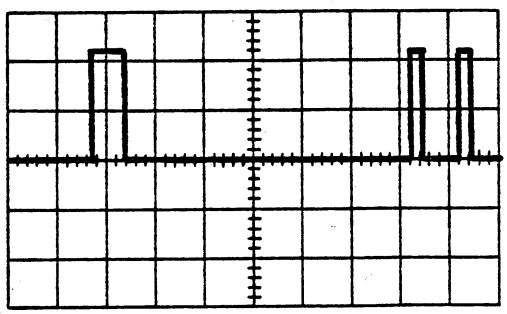
15 (NO.) U13-9, U13-11



2V (V/DIV)

.2 MSEC (S/DIV)

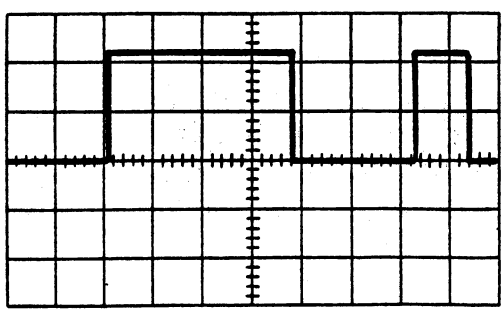
16 (NO.) U13-7



2V (V/DIV)

.2 MSEC (S/DIV)

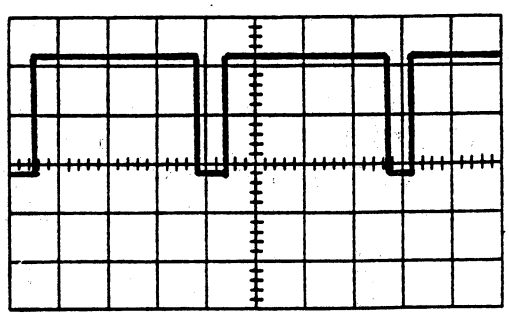
17 (NO.) U13-5



2V (V/DIV)

.1 MSEC (S/DIV)

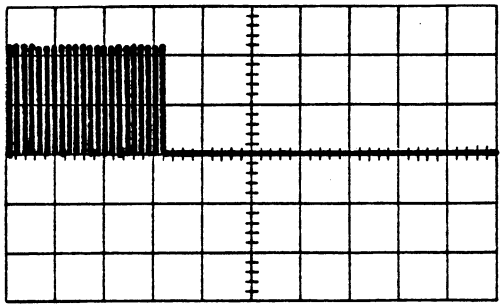
18 (NO.) KEYBOARD MATRIX OUTPUT



2V (V/DIV)

2 MSEC (S/DIV)

19 (NO.) U7-4, U7-18

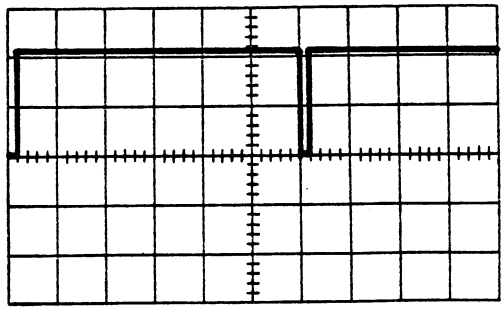


2V (V/DIV)

.2 SEC (S/DIV)

PULSE TRAIN

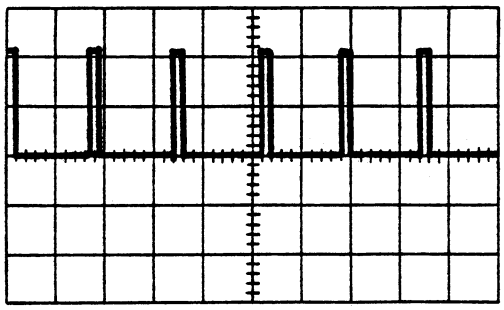
20 (NO.) U7-16



2V (V/DIV)

20 MSEC (S/DIV)

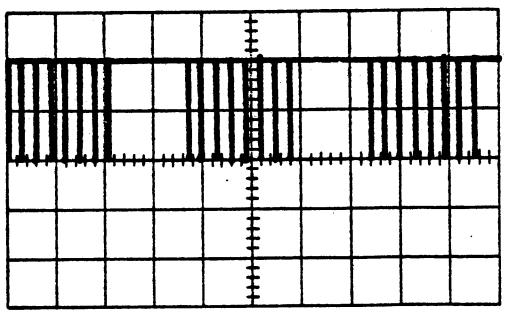
21 (NO.) U10-15



2V (V/DIV)

1 MSEC (S/DIV)

22 (NO.) U10-6

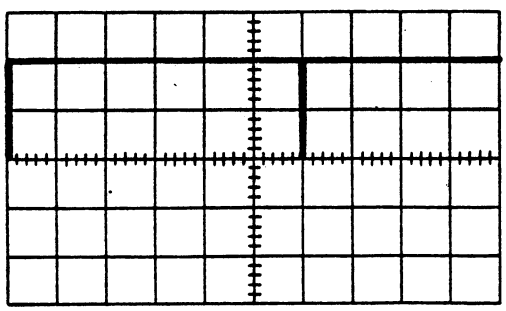


2V (V/DIV)

.5 MSEC (S/DIV)

PW = 30 μSEC

23 (NO.) U10-16

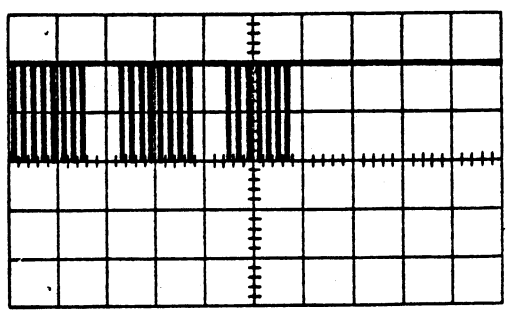


2V (V/DIV)

20 MSEC (S/DIV)

PW = 12 μSEC

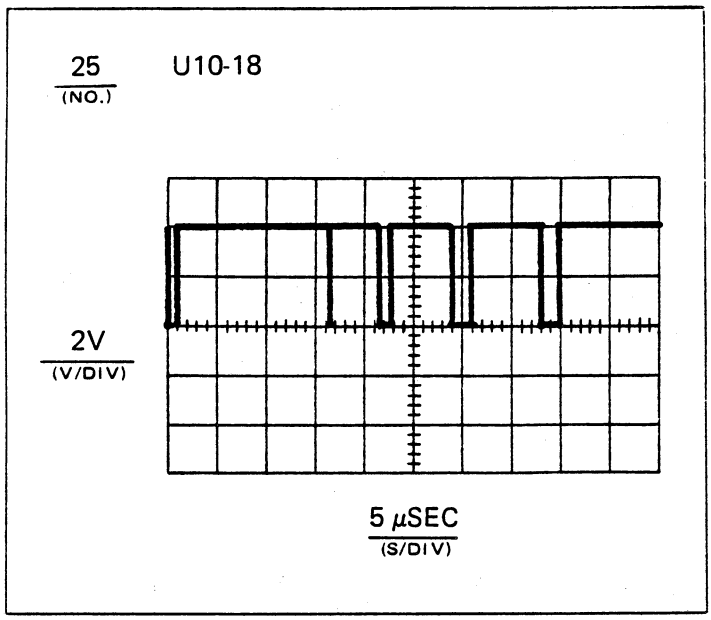
24 (NO.) U1-12



2V (V/DIV)

.1 MSEC (S/DIV)

PW = .5 μSEC


25
(NO.)
U10-18
2V
(V/DIV)
5 μSEC
(S/DIV)

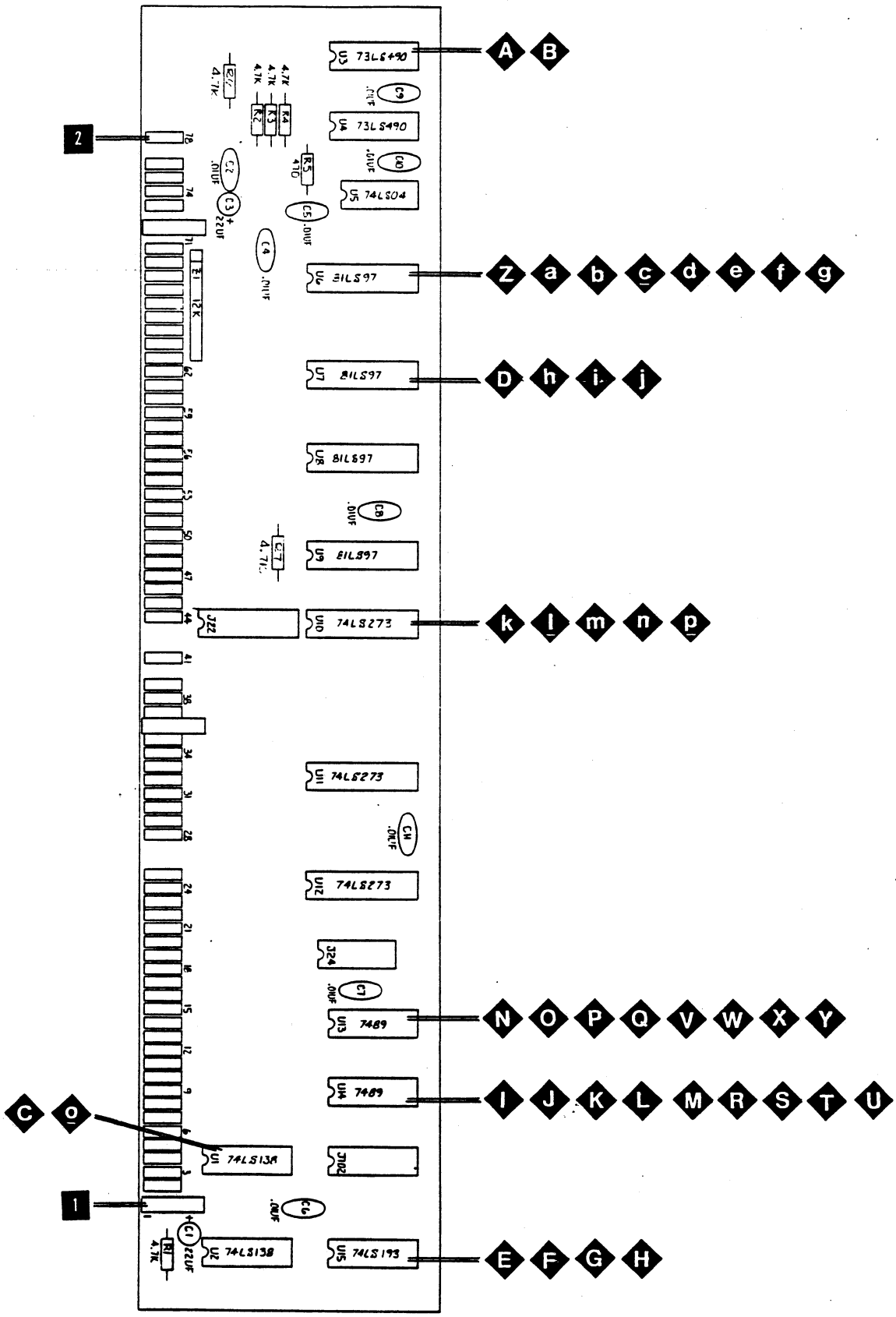


Figure 5.40 - I/O PC Board Assy, 406926

Table 5.36 - IC and Transistor Usage For (Main Logic) Function/Circuit Distribution

IC	Name	Type	Function/CKT
U1	Transistor (Array) Switch	CA3086	Switches Display Signals to Sig. Cond. A&B Test to SC A&B, Sep/Com to SCB, AC Coupling A&B to SC A&B.
U2	Quad 2 Input Nor Gate (4)	10102	100 MHz (ECL) to Synchronizer CKT EXT Arm to SIG DET ($\overline{\text{GATE A\&B}}$) and Synchronizer.
U3	Dual D (Master to Slave) F/F	10131	Synchronizer CKT for TI and TIA.
U4	Dual D (Master to Slave) F/F	10131	Synchronizer CKT for TI and TIA.
U5	Quad 2 Input Nor Gate	10102	Accumulator, Gate, and Timebase in Steering Logic CKTS.
U6	Quad 2 Input Nor Gate	10102	Signal Detect - FA, FB, and FC.
U7	Dual D (Master to Slave) F/F	10131	Marker CKT.
U8	Dual D (Master to Slave) F/F	10131	Signal Detect - $\overline{\text{GATE A\&B}}$
U9	2 Input Nand	74LS00	Timebase Out Steering Logic - Scaled Out Pulse Stretcher CKT - Gate Out Reference Out 10 MHz Test Signal to SCA and SCB.
U10	Dual D F/F	74LS74	Initialize CKT - Remote and Controller Gate Control CKT - $\overline{\text{DATA READY}}$
U11	Inverter	7404	Initialize CKT - $\overline{\text{REMOTE}}$ Clear Inverters (4) Gate Control CKT
U12	Quad 2 Input Nor Gate	10102	Synchronizer CKT
U13	Quad 2 Input Nor Gate	10102	Accumulator and Timebase in Steering Logic (3) Fast Counting Decade.
U14	Quad 2 Input Nor Gate	10102	Accumulator Steering Logic and Main Gate
U15	Dual 4/5 Input Or/Nor Gate	10109	Accumulator and Timebase in Steering Logic
U16	Dual 4/5 Input Or/Nor Gate	10109	Gate Steering Logic
U17	—	10102	Gate Steering and Gate Control
U18	Quad 2 Input Nor Gate	7402	Accumulator Steering, Gate Steering Logic Start/Stop CKT, and Clear CKT.
U19	Quad 2 Input Nand Gate	74LS00	Clear CKT - Periodic Rate
U20	Decade Counter	74LS90	÷ 10 Timebase Decade Counter
U21	Dual D (Master to Slave) F/F	10131	Fast-Counting (ECL) Decade
U22	Dual D (Master to Slave) F/F	10131	Fast-Counting (ECL) Decade
U23	Dual D (Master to Slave) F/F	10131	÷ 10 Timebase Decade Counter
U24	Dual D (Master to Slave) F/F	10131	÷ 10 Timebase Decade Counter
U25	Dual D (Master to Slave) F/F	10131	Gate Control CKT - Start/Stop
U26	Hex Inverter	74LS04	Initialize CKT, Start/Stop, and Clear CKT

Table 5.36 - IC and Transistor Usage For (Main Logic) Function/Circuit Distribution (continued)

IC	Name	Type	Function/CKT
U27	Hex Inverter	7400	Start/Stop, Clear CKTS
U28	MOS Timebase Counter	5009	$\div 10^{0-7}$ Timebase Decade Counter
U29	(3) 3-Input Positive Nand Gate	7412	Initialize, Start/Stop, and Clear CKTS
U30		74LS00	Initialize and Start/Stop (R-S F/F) CKTS
U31	Dual Monostable Multivibrator	74LS123	Initialize and Start/Stop CKT
U32	8 Bit Parallel Out Serial Shift Register	74LS164	Control Register
U33	8 Bit Parallel Out Serial Shift Register	74164	Control Register
U34	8 Bit Parallel Out Serial Shift Register	74LS164	Control Register
U35	Hex Inverter	7404	Synchronizer, Timebase Decade Counters, Timebase Out Steering Logic, Pulse Stretcher.
U36	Dual D Edge Trigger F/F	7474	Gate Control and Timebase Decade Counters
U37	Dual D Edge Trigger F/F	7400	Gate Control, Pulse Stretcher and Ripple Delay CKTS
U38	Dual 4 Bit Decade Counter	74LS490	Accumulator Decade Counters
U39	Dual 4 Bit Decade Counter	74LS490	Accumulator Decade Counters
U40	Dual 4 Bit Decade Counter	74LS490	Accumulator Decade Counters
U41	Dual 4 Bit Decade Counter	74LS490	Accumulator Decade Counters
U42	Parallel Load 8 Bit Shift Register	74LS165	Shift Register
U43	Parallel Load 8 Bit Shift Register	7404	Pulse Stretcher and Ripple Delay CKTS
U44	4-Wide 2-Input and 1Ω-Invert Gate	7454	Timebase Out Steering Logic
U45	4-Wide 2-Input and 1Ω-Invert Gate	74LS00	Ripple Delay and Overflow Latch (R-S F/F's)
U46	4-Wide 2-Input and 1Ω-Invert Gate	74LS165	Shift Register
U47		74LS165	Shift Register
U48		74LS165	Shift Register
U49		74LS165	Shift Register
U50		74LS00	Shift Register and Ripple Delay ($\overline{\text{UPDATE}}$)
U51		74LS74	Timebase Decade Counter CKT
U52		74LS02	Gate Control CKT ($\overline{\text{CLEAR}}$)
U53	Voltage Regulators	LM309K	+5.4 VDC
U54	Voltage Regulators	MC7812CK	+12 VDC
U55	Voltage Regulators	LM320K	−12 VDC
U56	Voltage Regulators	LM309K	+5 VDC } Power Supply Regulators
U57	Voltage Regulators	LM309K	+5 VDC
U58	Voltage Regulators	LM309K	+5 VDC

Table 5.36 - IC and Transistor Usage For (Main Logic) Function/Circuit Distribution (continued)

IC	Name	Type	Function/CKT
Q1	Silicon PNP	4248	Clear CKT
Q2	Silicon NPN	3646	Clear CKT
Q3		4248	Marker CKT
Q4		4248	Marker CKT
Q5		4248	Signal Detect $\overline{\text{GATE A}}$
Q6		4248	Signal Detect $\overline{\text{GATE B}}$
Q7	Silicon PNP	4258	Timebase In Steering Logic
Q8		4258	Timebase In Steering Logic
Q9		4248	Fast Counting (ECL) Decade
Q10		4248	Fast Counting (ECL) Decade
Q11		4248	Fast Counting (ECL) Decade
Q12		4258	Timebase Decade Counter
Q13		4258	Timebase Decade Counter
Q14		4248	Gate Control CKT
Q15		4248	Fast Counting (ECL) Decade
Q16		4248	Fast Counting (ECL) Decade
Q17		4248	Pulse Stretcher CKT
Q18		3646	Gate Control CKT
Q19		3646	Gate Control CKT
Q20		3646	Gate Delay CKT
Q21		3646	Gate Delay CKT
Q22		3646	RMT S/S Drive Signal.

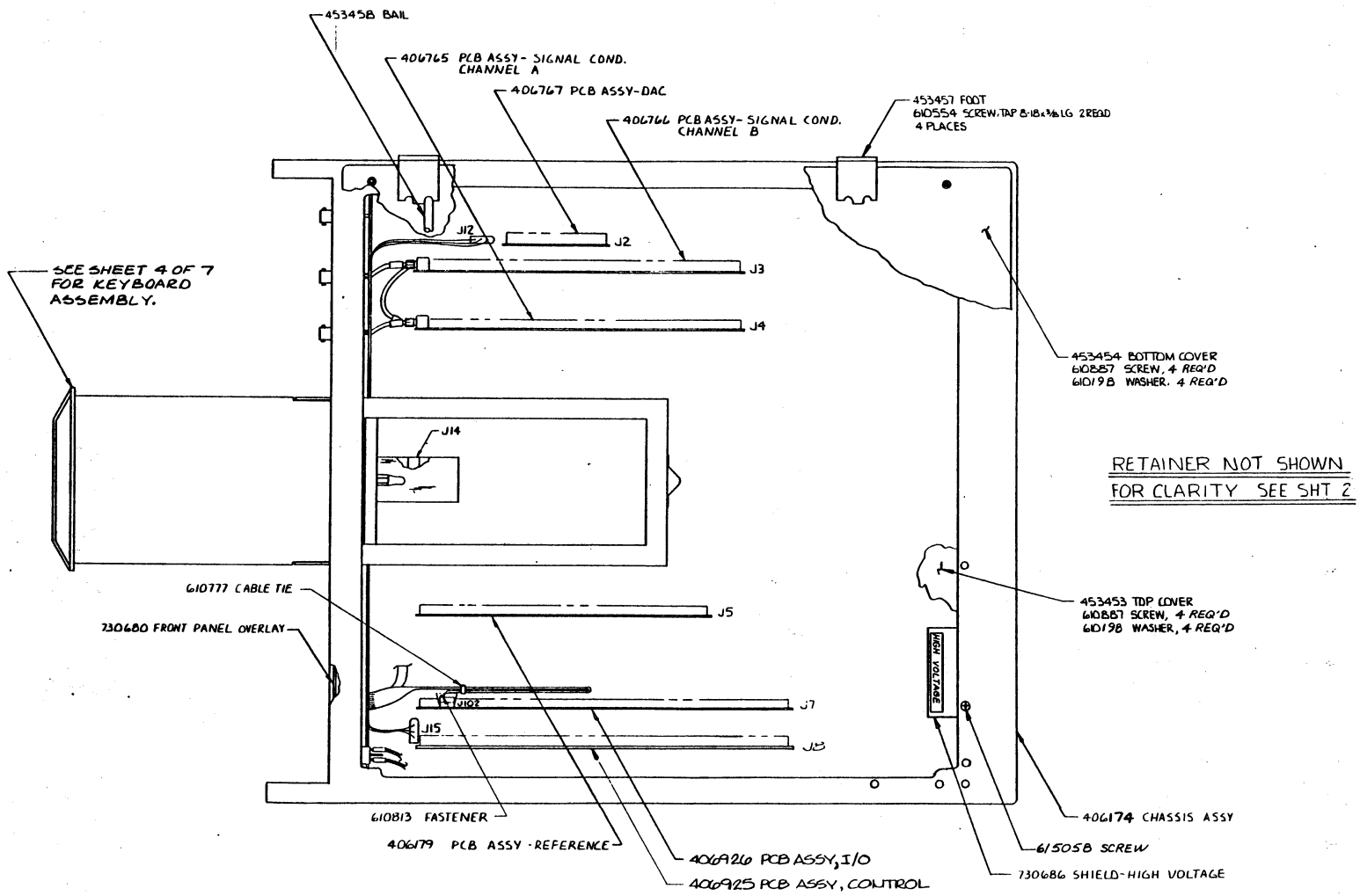
5.14 BOARD REVISION.

5.14.1 Every effort is made to keep the manual concurrent with the instrument despite changes to the design, which are an inevitable adjunct of the manufacturing process. The manual is updated and periodically reprinted throughout the year. In between printings, Addendums and Errata Sheets are added to the manual if required to implement the reprinted copy.

5.14.2 Any design change is accompanied by an updating of a board revision. Such change could be as simple as a revised hole size or as complex as major modifications of the circuitry. The revision of a board is indicated by the letter preceding the assembly number on the board; the revision of the assembly drawing in Section 6 or on an Errata Sheet is indicated by the letter following the assembly number, located below the drawing. Comparing the revision letters can indicate how closely the drawing corresponds to the board.

SECTION 6 DRAWINGS

Title	Page
Layout, 9015A Counter (406172)	6-2
Layout, 9035A Counter (406173)	6-3
Layout, 9015/11A Counter (406170)	6-4
Layout, 9035/11A Counter (406171)	6-5
Layout, Main Logic (406931)	6-6
Schematic, Main Logic (721931)	6-8
Schematic, Power Supply (Part of Main Logic)	6-7
Layout, I/O (406926)	6-10
Schematic, I/O (721926)	6-11
Layout, Control (406925)	6-12
Schematic, Control (721925)	6-13
Layout, Signal Conditioner A (406765)	6-15
Layout, Signal Conditioner B (406766)	6-16
Schematic, Signal Conditioner A&B (721765/6)	6-17
Layout, DAC (406767)	6-18
Schematic, DAC (721767)	6-19
Layout, Reference (406768)	6-20
Schematic, Reference (721768)	6-21
Layout, Display (406764)	6-23
Schematic, Display (721764)	6-24
Layout, Keyboard -- 9015A, 9035A (406831)	6-26
Layout, Keyboard -9015/11A, 9035/11A (406832)	6-27
Schematic, Keyboard (721831)	6-28
Chassis Assembly (406174)	6-29
Layout, Front Panel (406771)	6-30
Layout, Rear Panel (406772)	6-31
Layout, Prescaler --9035A, 9035/11A (406793)	6-32
Schematic, Prescaler --9035A, 9035/11A (721793)	6-33
Rear Input, Option 01 (406803)	6-34
Programmable Synchronous Window & Selective Gate Control Option 06PA (406939)	6-35
Layout, PCB, Option 06P (406875)	6-36
Schematic, PCB, Option 06P (721875)	6-36
Programmable 50 Ohm, Option 07 (406896 - Part of Option 06P)	6-37
Layout, Signal Conditioner A, Option 07 (406894 - Part of Option 06P)	6-38
Layout, Signal Conditioner B, Option 07 (406895 - Part of Option 06P)	6-39
Schematic, Signal Conditioner (721765/6)	6-17
Oven Oscillator, Option 22 (406805)	6-40
Layout, Oscillator (406818)	6-41
Layout, Power Supply (406795)	6-42
Schematic, Power Supply (721795)	6-43
Oven Oscillator, Option 24 (406806)	6-44
Layout, Oscillator (406819)	6-45
Layout, Power Supply (406795)	6-42
Schematic, Power Supply (721795)	6-43
GPIB IEEE 488-1975 Interface, Option 55 (406938)	6-46
Layout, GPIB (406929)	6-47
Schematic, GPIB (721929)	6-48
Layout, Address (406930)	6-49
Schematic, Address (721930)	6-50
High Speed Computer Interface, Option 56 (406942)	6-51
Layout, High Speed Computer Interface (406817)	6-52
Schematic, High Speed Computer Interface (721817)	6-53



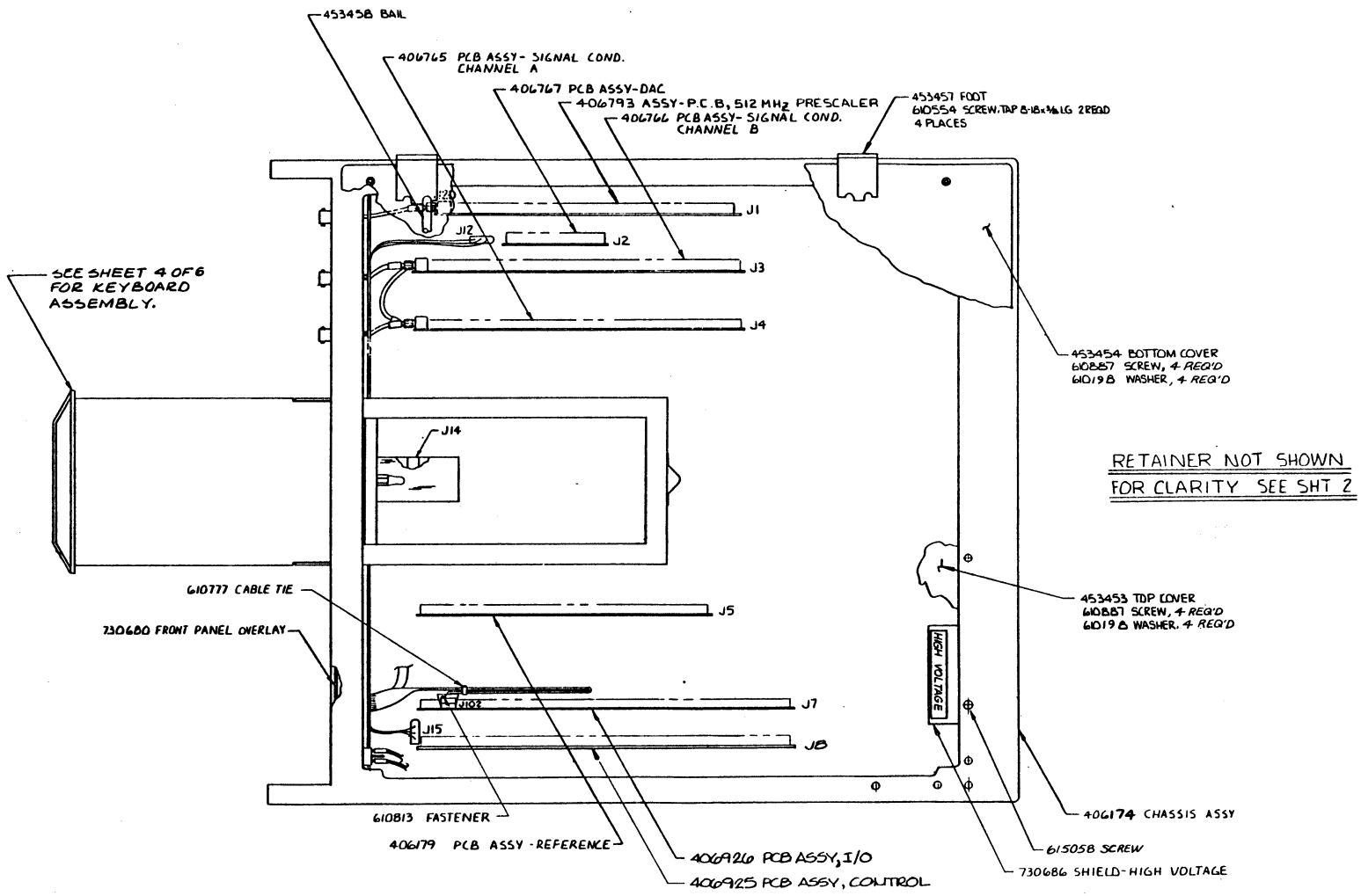
2. ASSEMBLE PER RACAL-DANA WORKMANSHIP STANDARD.
1. 600620 POWER CABLE IS PART OF THIS ASSY.

NOTES: UNLESS OTHERWISE SPECIFIED

COUNTER TIMER ASSY
9015A/ARITHMETIC

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406172	H

SCALE NONE SHEET 1 OF 6



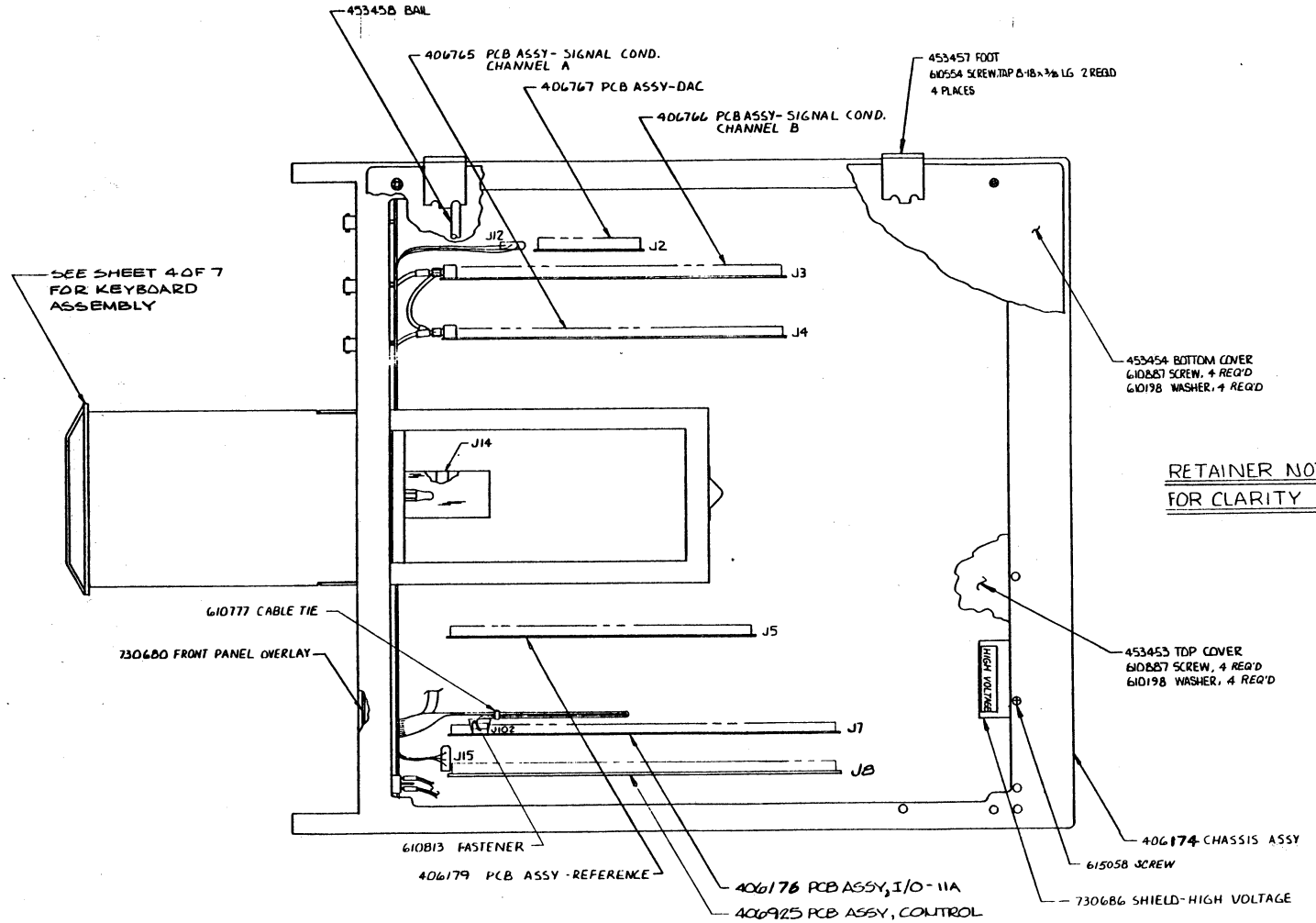
2. ASSEMBLE PER RACAL-DANA WORKMANSHIP STANDARD.
1. 600620 POWER CABLE IS PART OF THIS ASSY.

NOTES: UNLESS OTHERWISE SPECIFIED

COUNTER TIMER ASSY
9035A/ARITHMETIC

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406173	E

SCALE NONE SHEET 1 OF 6



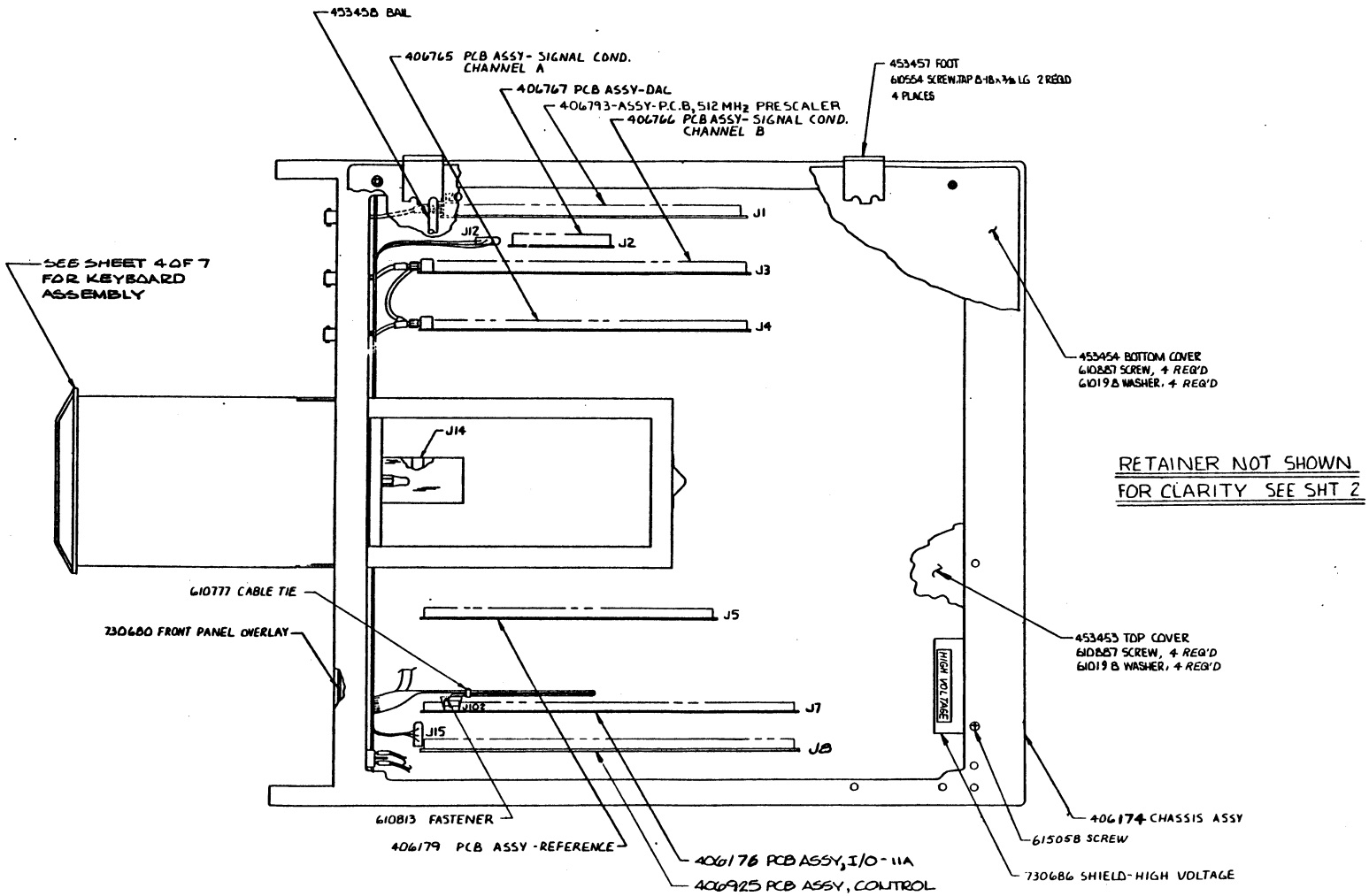
2. ASSEMBLE PER RACAL-DANA WORKMANSHIP STANDARD.
1. 600620 POWER CABLE IS PART OF THIS ASSY.

NOTES: UNLESS OTHERWISE SPECIFIED

COUNTER TIMER ASSY
9015/11A

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406170	H

SCALE NONE SHEET 1 OF 7



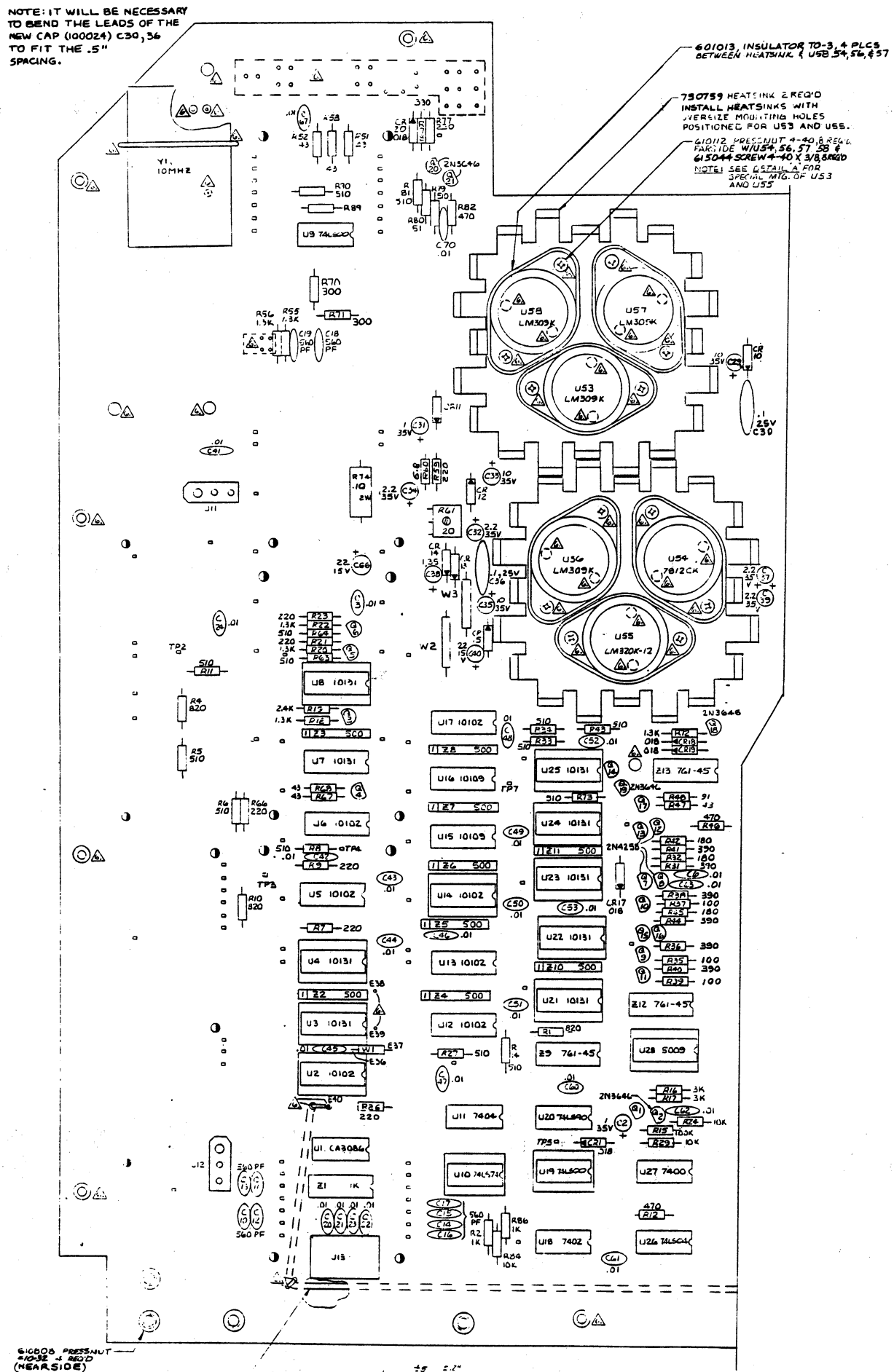
2. ASSEMBLE PER RACAL-DANA WORKMANSHIP STANDARD.
1. 600620 POWER CABLE IS PART OF THIS ASSY.

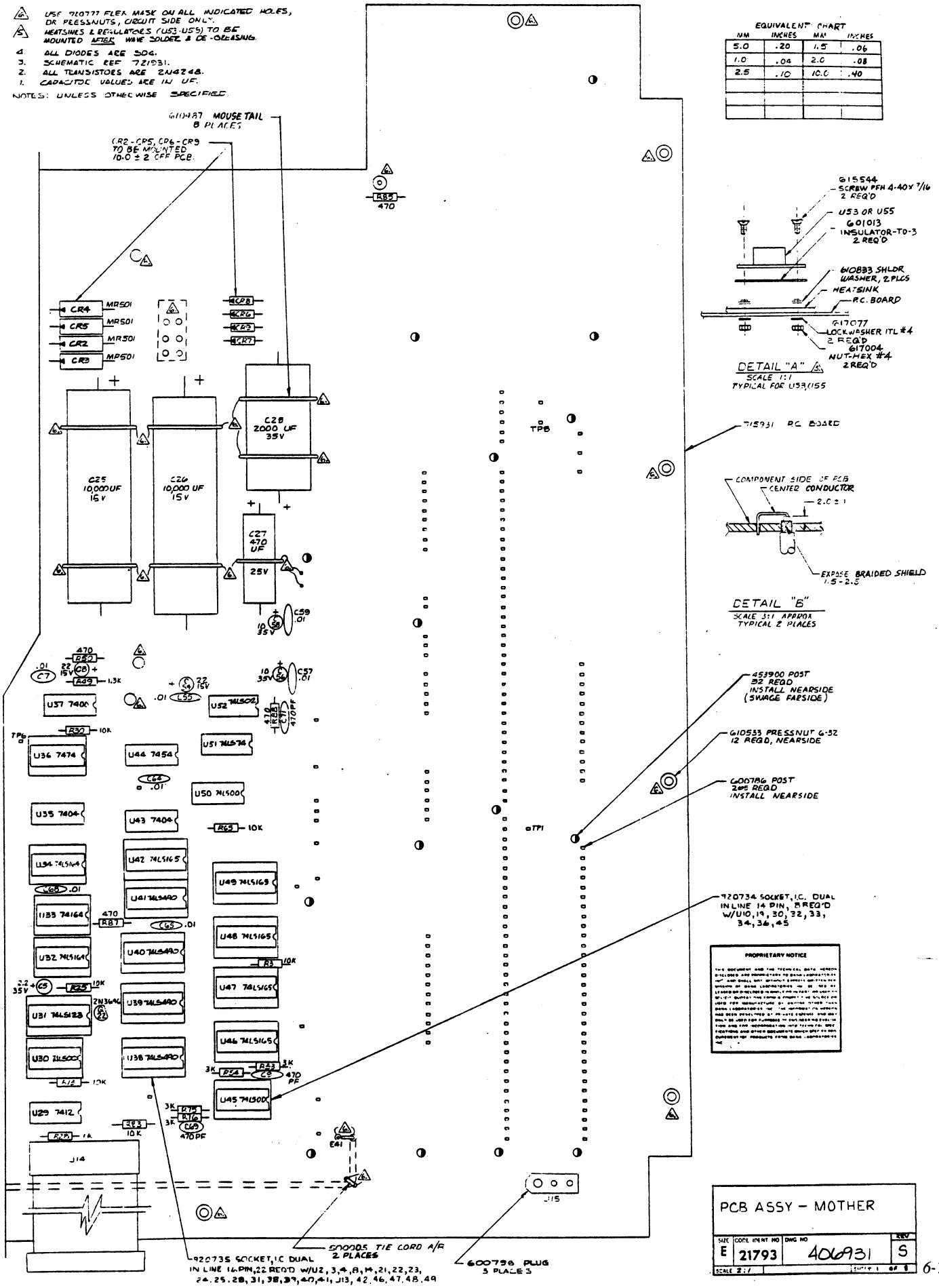
NOTES: UNLESS OTHERWISE SPECIFIED

COUNTER TIMER ASSY
9035/11A

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406171	D

SCALE NONE SHEET OF 7

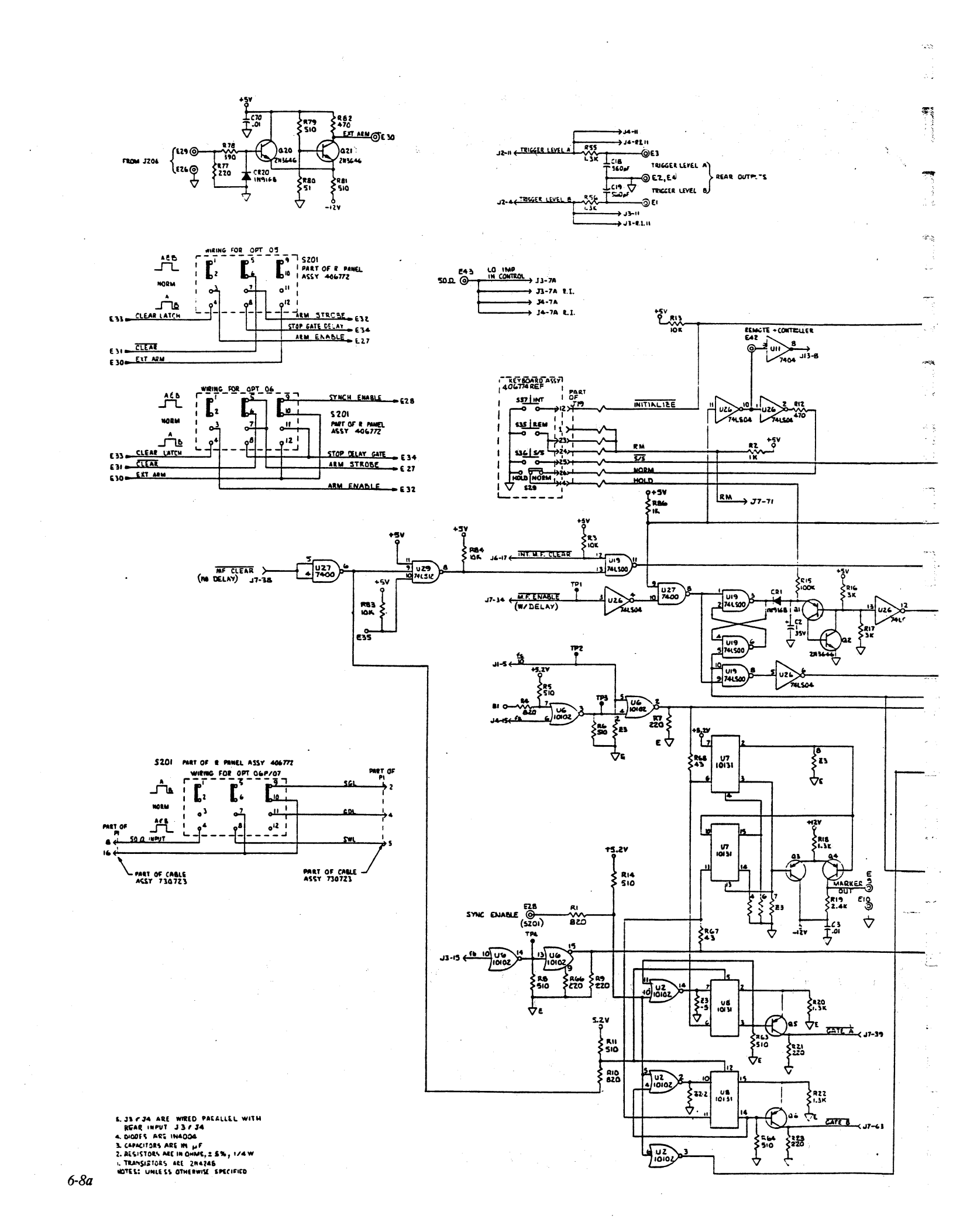

NOTE: IT WILL BE NECESSARY TO BEND THE LEADS OF THE NEW CAP (100024) C30,36 TO FIT THE .5" SPACING.
601013, INSULATOR TO-3, 4 PLCS BETWEEN HEATSINK & U58,54,56,&57
750759 HEATSINK 2 REQ'D INSTALL HEATSINKS WITH OVERSIZE MOUNTING HOLES POSITIONED FOR U53 AND U55.
610112 PRESSNUT 4-40,8 REQ'D. FARSIDE W/U54,56,57,58 & 615044 SCREW 4-40 X 3/8,8REQD
NOTE: SEE DETAIL A FOR SPECIAL MTG. OF U53 AND U55
U58 LM309K
U57 LM309K
U53 LM309K
U56 LM309K
U54 7812CK
U55 LM320K-12
610808 PRESSNUT #10-32 4 REQD (NEARSIDE)
501446 COAX CABLE A/D 3250 (128") LG. SEE DETAIL "B" FOR WIRE PREPARATION



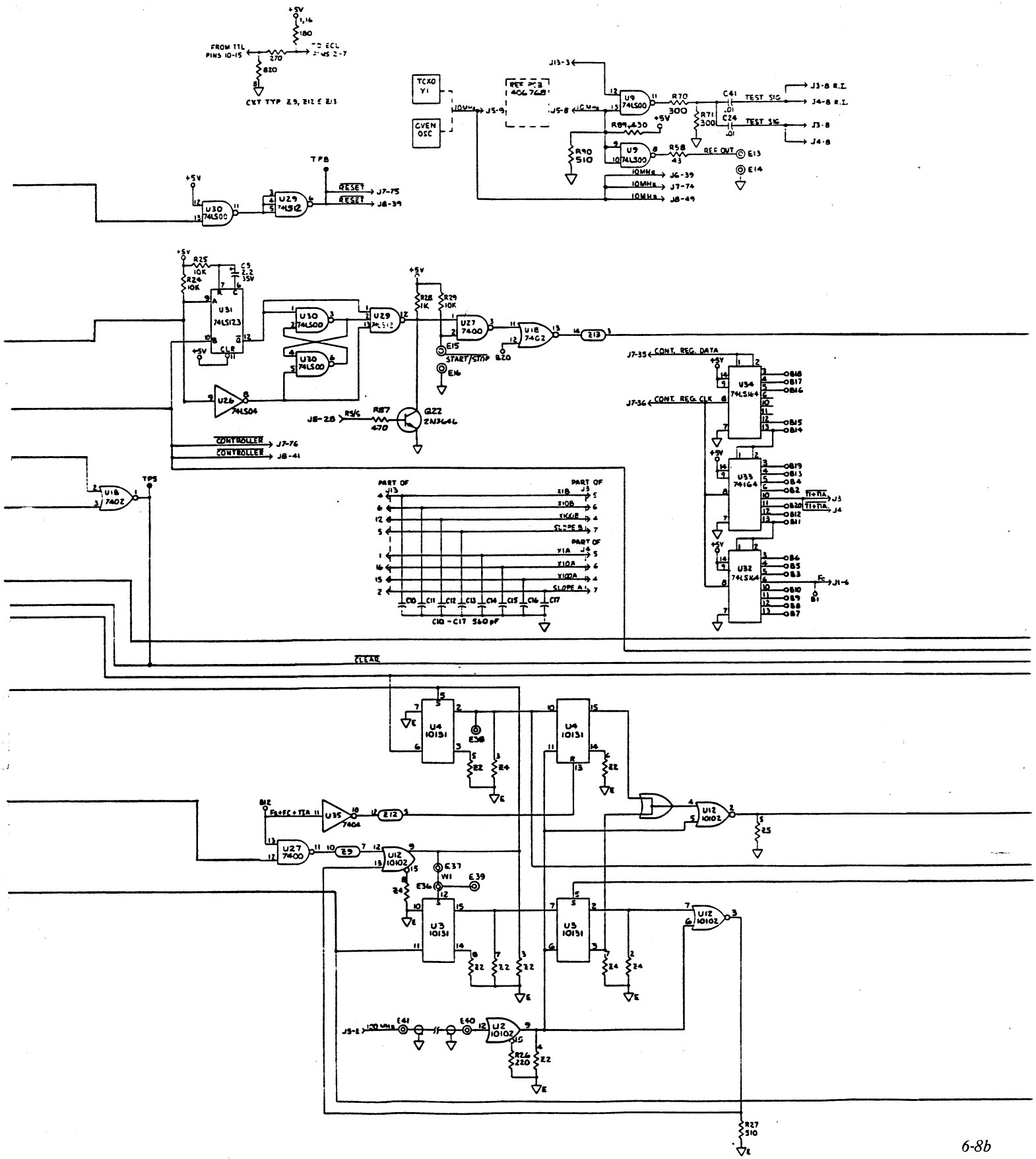
PCB ASSY – MOTHER

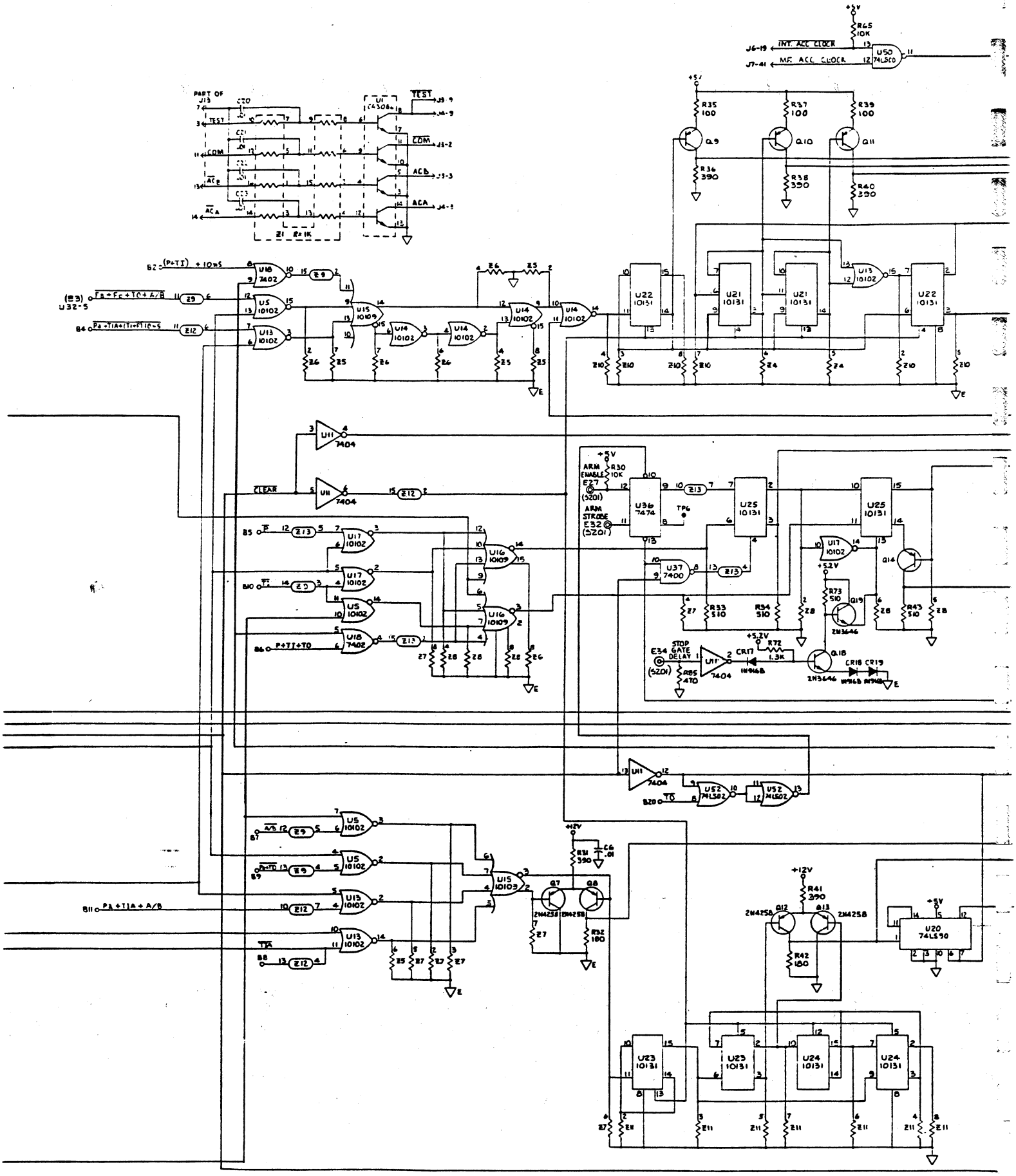
SIZE	CODE IDENT NO	DWG NO	REV
E	21793	406931	S

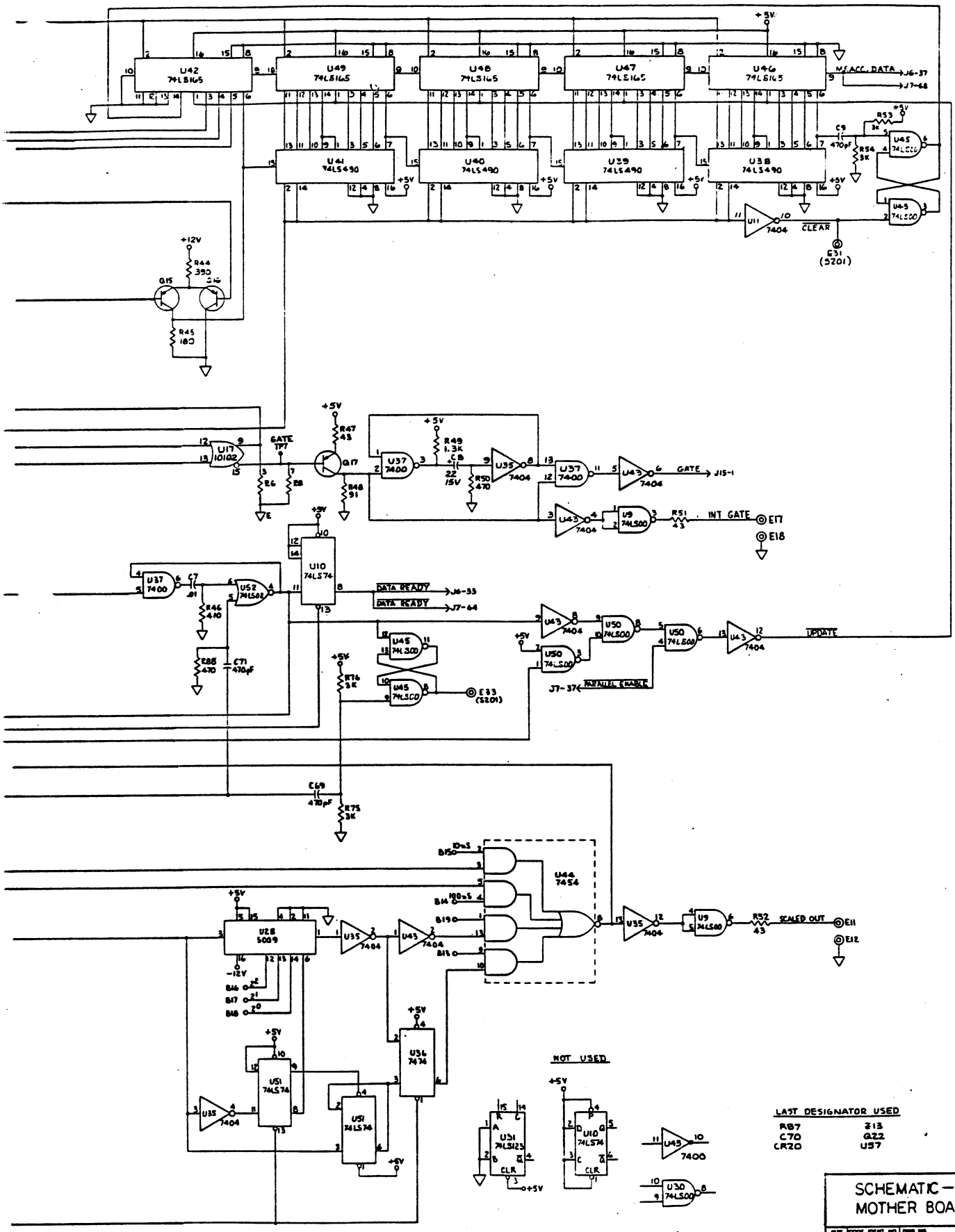
SCALE 2:1 SHEET 1 OF 1

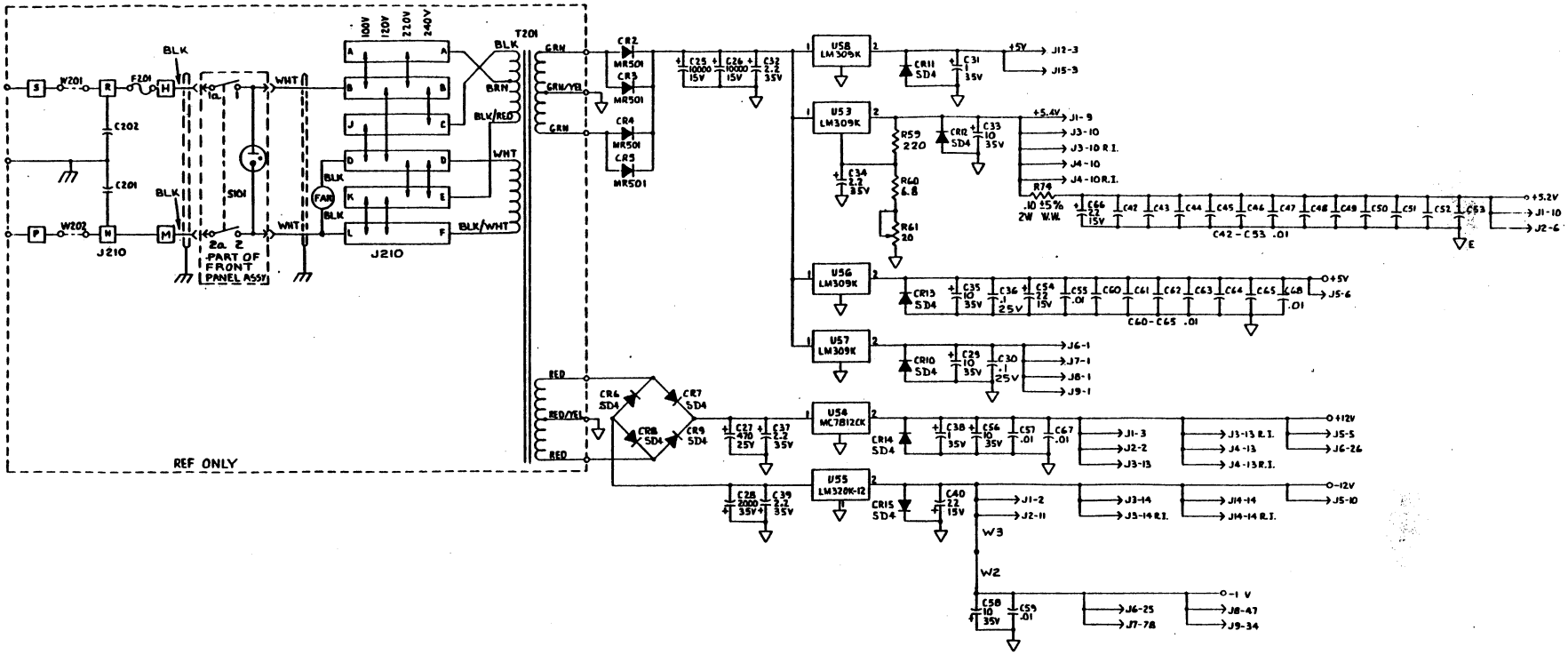


5. J3 & J4 ARE WIRED PARALLEL WITH REAR INPUT J3 & J4
4. DIODES ARE IN4004
3. CAPACITORS ARE IN μF
2. RESISTORS ARE IN OHMS, ± 5%, 1/4 W
1. TRANSISTORS ARE 2N4248
NOTES: UNLESS OTHERWISE SPECIFIED


+5V
FROM TTL PINS 10-15
270
820
CKT TYP E9, E12 & E13
TCXO Y1
OVEN OSC
10MHz
J5-9
J13-3
U9 74LS00
R70 300
C41
TEST SIG
J3-8 R.I.
J4-8 R.I.
R71 300
C24
J3-8
J4-8
R89 430
R90 510
R58 43
REF OUT
E13
E14
10MHz J6-39
10MHz J7-74
10MHz J8-49
TPB
U30 74LS00
U29 74S12
RESET J7-75
RESET J8-39
R25 10K
R24 10K
C5 2.2 35V
U31 74LS123
CLR
U26 74LS04
R28 1K
R29 10K
U27 7400
U18 7402
E15
START/STOP
E16
B20
213
J8-28
R56
R57 470
Q22 2N3646
CONTROLLER J7-76
CONTROLLER J8-41
J7-35 CONT. REG. DATA
J7-36 CONT. REG. CLK
U34 74LS164
U33 74164
U32 74LS164
B18
B17
B16
B15
B14
B19
B13
B4
B2
B20 TI+TA J3
TI+TA J4
B12
B11
B6
B5
B3
Fc J1-6
B1
B10
B9
B8
B7
TPS
PART OF J13
PART OF J4
X1B
X10B
X100B
SLOPE B
X1A
X10A
X100A
SLOPE A
C10 C11 C12 C13 C14 C15 C16 C17
C10 - C17 560 pF
CLEAR
U4 10131
U6 10131
U3 10131
U5 10131
U12 10102
U2 10102
E38
E22
E24
B12
FREQ + TIA 11
U35 7404A
E9
E37
W1
E39
E36
E34
E41
E40
J3-2
100 MHz
R26 220
R27 510


INT. ACC CLOCK
MF. ACC CLOCK
TEST
COM
ACB
ACA
ARM ENABLE E27 (5201)
ARM STROBE E32 (5201)
STOP GATE DELAY E34 (5201)
CLEAR
+5V
+5.2V
+12V
+8V
U50 74LS00
U11 7404
U36 7474
U37 7400
U52 74LS02
U20 74LS90
U15 10109
U16 10109
U15 10103
U1 CA3086
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q18
Q19
2N4258
2N3646
IN968B
CR17
CR18
CR19


U42 74LS165
U49 74LS165
U48 74LS165
U47 74LS165
U46 74LS165
M.F.ACC. DATA
J6-37
J7-68
U41 74LS490
U40 74LS490
U39 74LS490
U38 74LS490
U45 74LS00
U11 7404
CLEAR
E31 (5201)
+12V
R44 390
Q15
Q16
R45 180
U17 10102
GATE TP7
Q17
R47 43
R48 91
U37 7400
R49 1.3K
C8 22 15V
U35 7404
R50 470
U43 7404
GATE
J15-1
U9 74LS00
R51 43
INT GATE
E17
E18
U10 74LS74
C7 .01
R46 410
R88 470
C71 470pF
U52 74LS02
DATA READY
J6-33
DATA READY
J7-64
U50 74LS08
U50 74LS00
PARITEL ENABLE
J7-37
UPDATE
U45 74LS01
U45 74LS00
R74 3K
E33 (5201)
C69 470pF
R75 3K
U44 7454
B150
B14
B190
B13
U28 5009
-12V
B16
B17
B18
R52 43
SCALED OUT
E11
E12
U36 7474
U51 74LS74
U35 7404
NOT USED
U31 74LS123
U10 74LS74
CLR
U45 7400
U30 74LS00
LAST DESIGNATOR USED
RB7
C70
CR20
Z13
Q22
U57
SCHEMATIC – MOTHER BOARD
SIZE J
CODE IDENT NO. 21793
DWG NO. 721931
REV M
SCALE
SHEET 1 OF 2

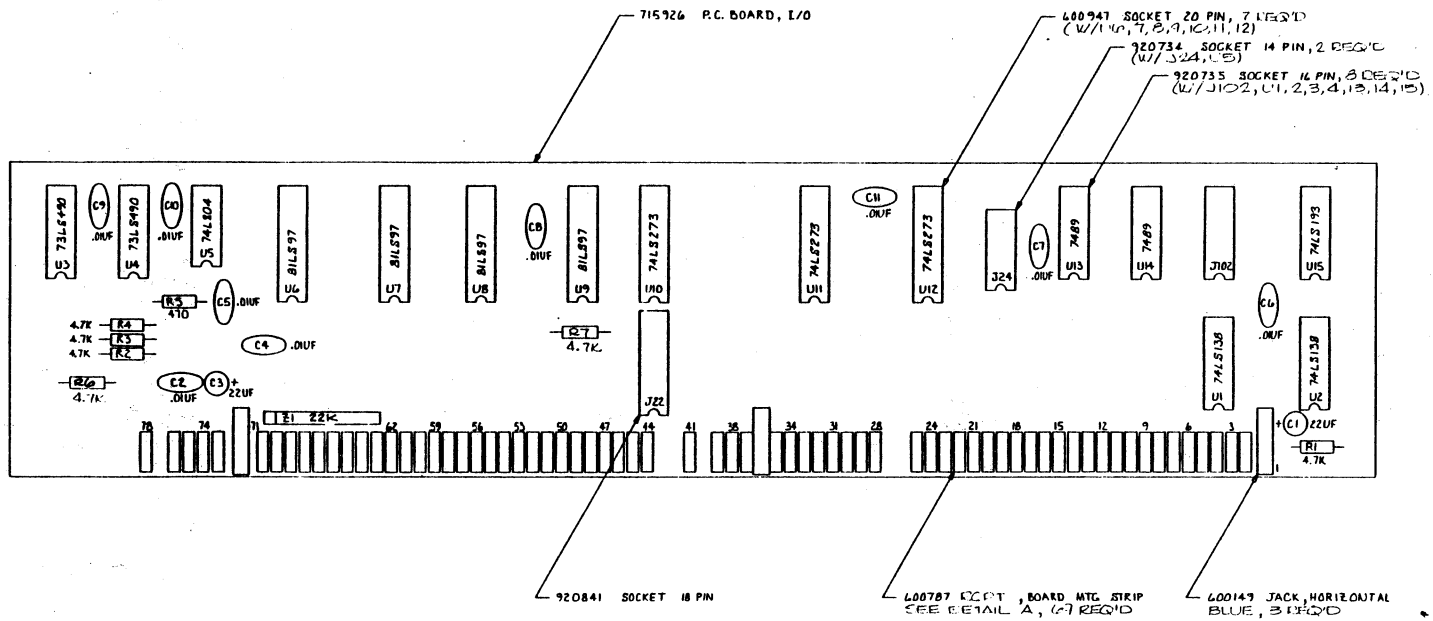


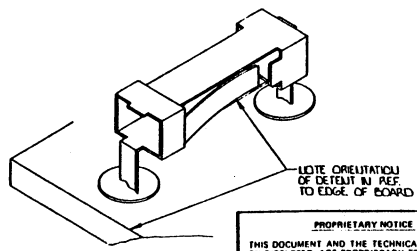
NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC MOTHER BOARD

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721931	M

SCALE NONE | SHEET 2 OF 2





DETAIL A
NO SCALE

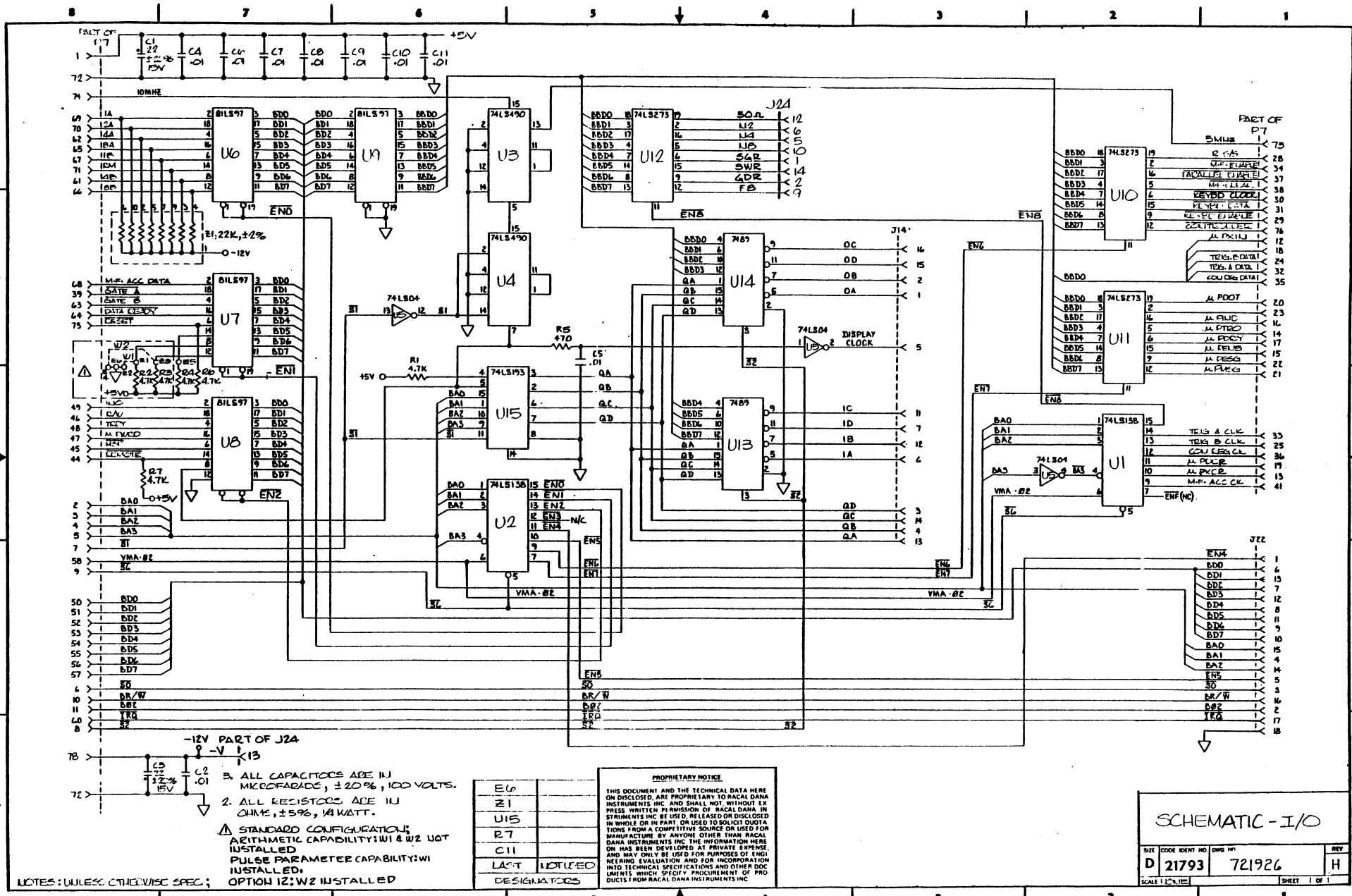
2. SCHEMATIC REFERENCE 721924.
1. ASSEMBLE PER RACAL-DANA WORKMANSHIP MANUAL.

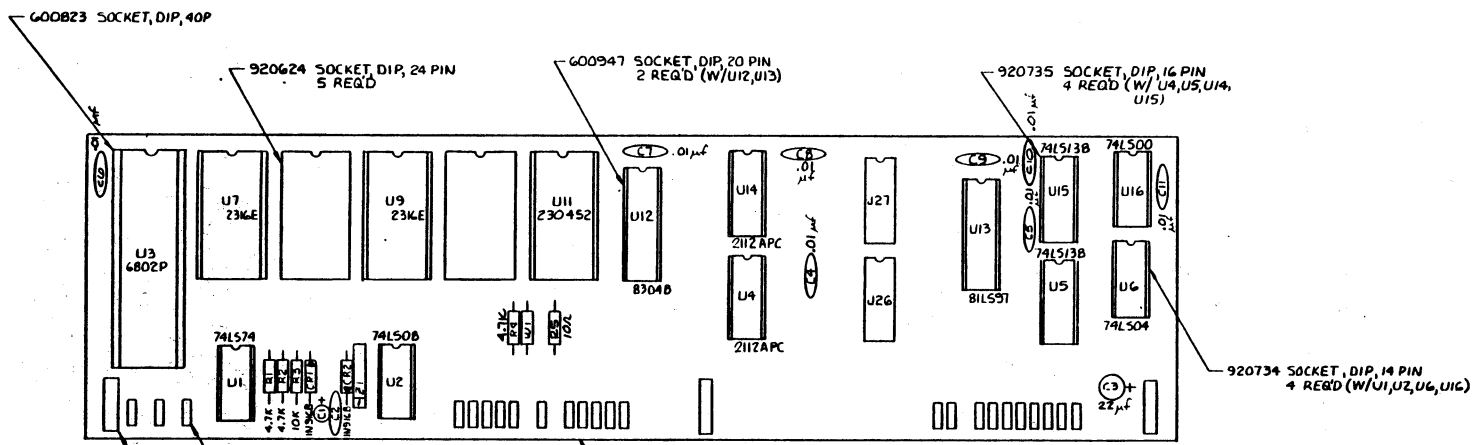
NOTES: UNLESS OTHERWISE SPECIFIED

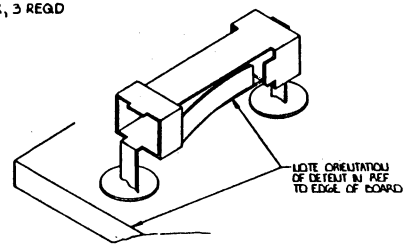
P.C. BOARD ASSY, I/O

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406926	D

SCALE NONE | SHEET 1 OF 1


PART OF U7
C1 22 ±20% 15V
C4 .01
C6 .01
C7 .01
C8 .01
C9 .01
C10 .01
C11 .01
+5V
10MHz
U6
U9
U3
U4
U12
U10
U11
U14
U13
U15
U2
U1
U7
U8
J24
J14
J22
PART OF P7
5MHz
R1 4.7K
R5 470
C5 .01
R7 4.7K
21; 22K, ±2%
0-12V
74LS490
74LS273
74LS193
74LS138
74LS04
74S89
8ILS97
DISPLAY CLOCK
KEYBD CLOCK
-12V PART OF J24
C3 22 ±20% 15V
C2 .01
3. ALL CAPACITORS ARE IN MICROFARADS, ±20%, 100 VOLTS.
2. ALL RESISTORS ARE IN OHMS, ±5%, ¼ WATT.
⚠ STANDARD CONFIGURATION; ARITHMETIC CAPABILITY: W1 & W2 NOT INSTALLED
PULSE PARAMETER CAPABILITY: W1 INSTALLED.
OPTION 12: W2 INSTALLED
NOTES: UNLESS OTHERWISE SPEC;
E6
Z1
U15
R7
C11
LAST DESIGNATORS
NOTUSED
PROPRIETARY NOTICE
THIS DOCUMENT AND THE TECHNICAL DATA HERE ON DISCLOSED, ARE PROPRIETARY TO RACAL DANA INSTRUMENTS INC AND SHALL NOT, WITHOUT EXPRESS WRITTEN PERMISSION OF RACAL DANA INSTRUMENTS INC BE USED, RELEASED OR DISCLOSED IN WHOLE OR IN PART, OR USED TO SOLICIT QUOTATIONS FROM A COMPETITIVE SOURCE OR USED FOR MANUFACTURE BY ANYONE OTHER THAN RACAL DANA INSTRUMENTS INC THE INFORMATION HERE ON HAS BEEN DEVELOPED AT PRIVATE EXPENSE, AND MAY ONLY BE USED FOR PURPOSES OF ENGINEERING EVALUATION AND FOR INCORPORATION INTO TECHNICAL SPECIFICATIONS AND OTHER DOCUMENTS WHICH SPECIFY PROCUREMENT OF PRODUCTS FROM RACAL DANA INSTRUMENTS INC
SCHEMATIC - I/O
SIZE D
CODE IDENT NO. 21793
DWG NO 721926
REV H
SHEET 1 OF 1





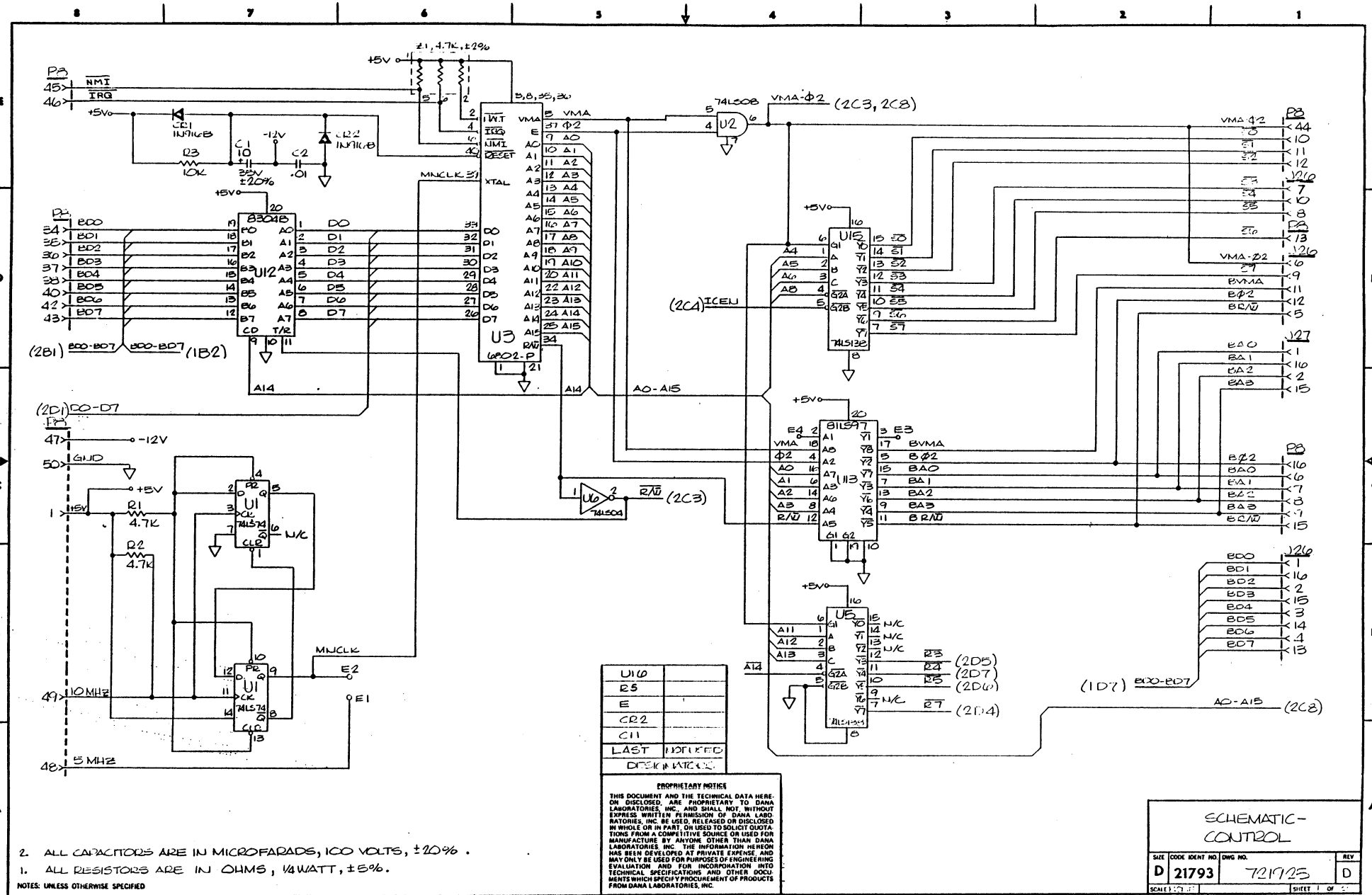
DETAIL "A"
NO SCALE

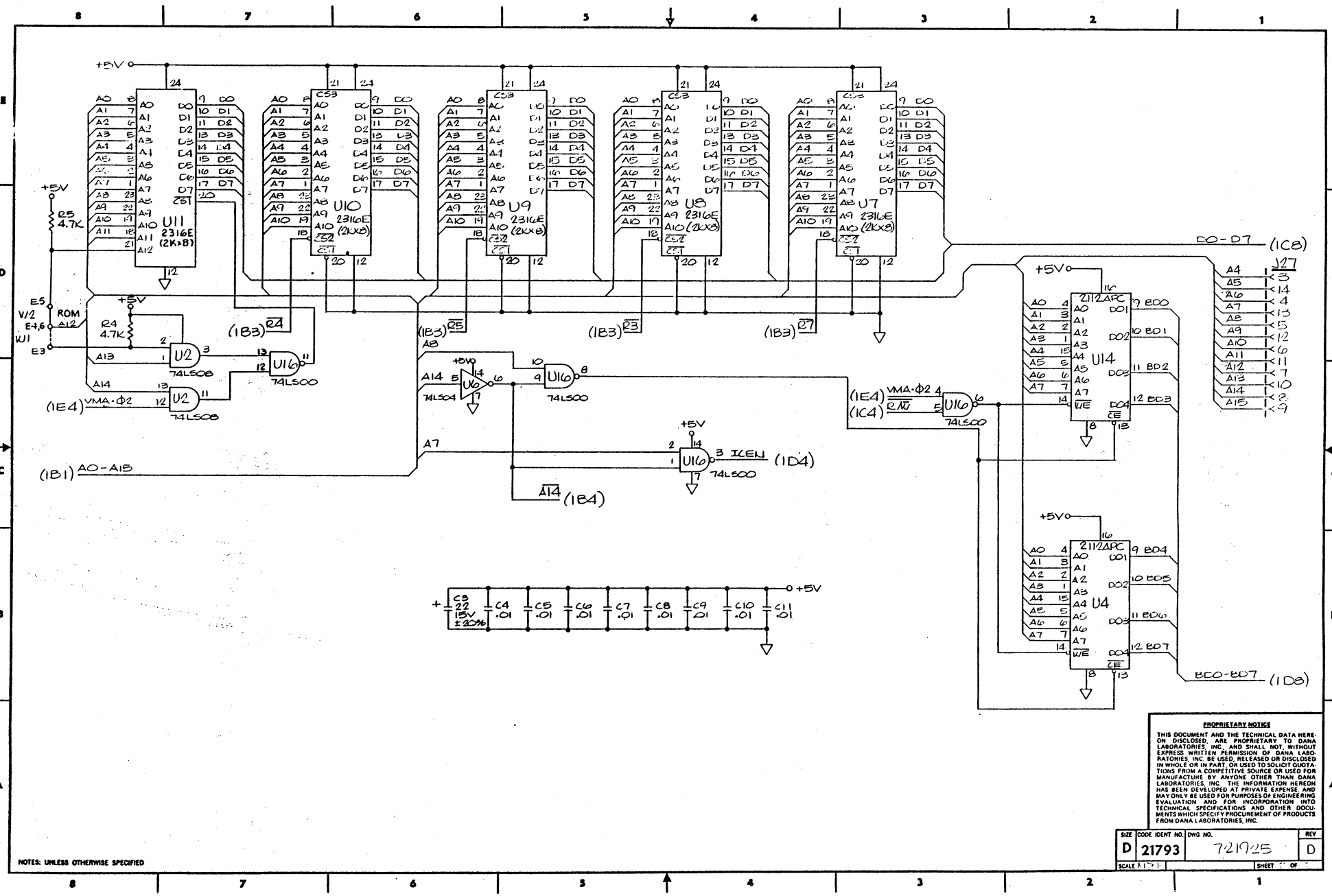
2. REFERENCE SCHEMATIC 721925.
1. ASSEMBLE PER DANA WORKMANSHIP STANDARD.
NOTES: UNLESS OTHERWISE SPECIFIED

CONTROL PCB ASSY

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406925	D

SCALE 2:1 SHEET 1 OF 3

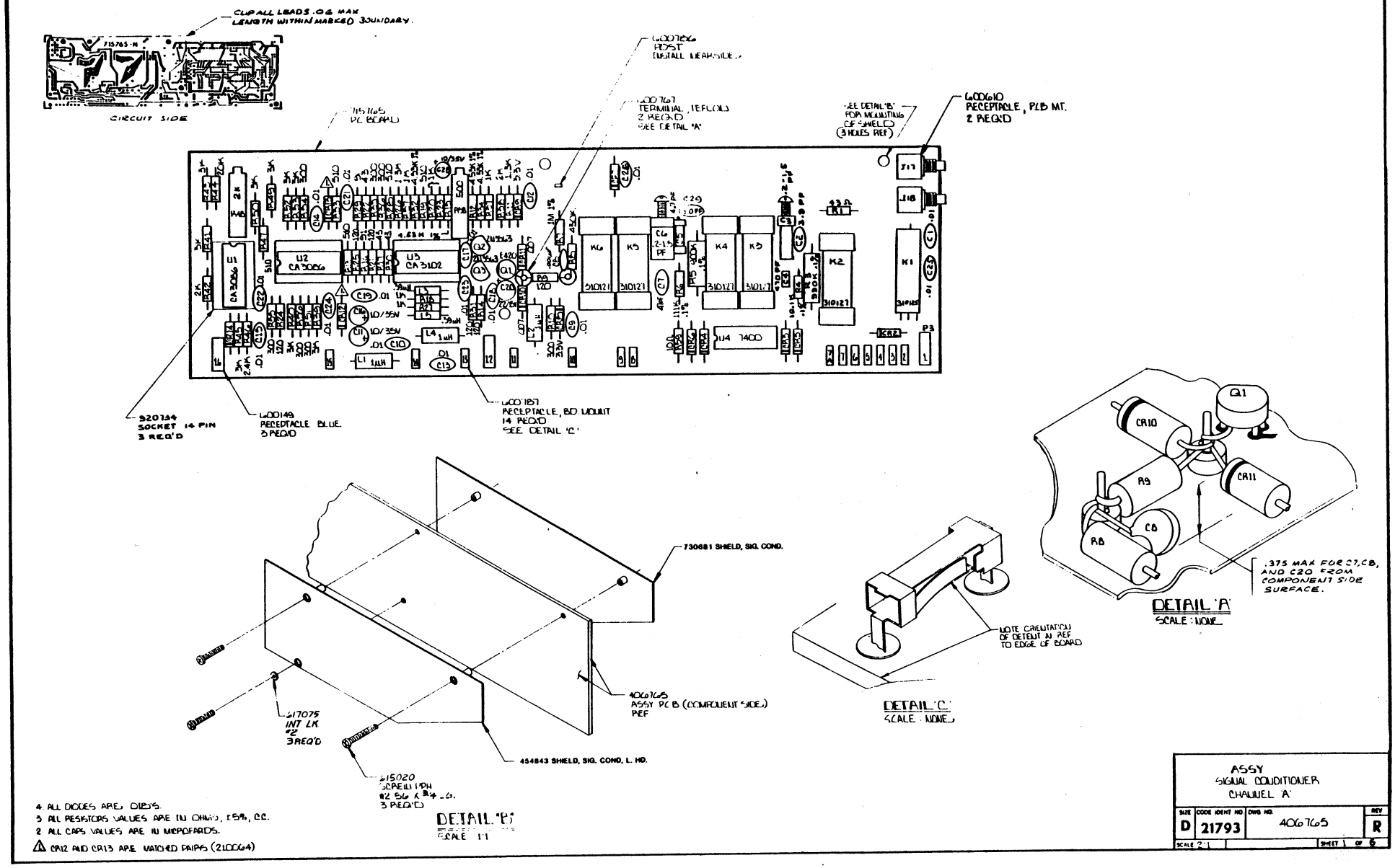

SCHEMATIC-
CONTROL
SIZE D
CODE IDENT NO. 21793
DWG NO. 721725
REV D
SHEET 1 OF
PROPRIETARY NOTICE
THIS DOCUMENT AND THE TECHNICAL DATA HEREON DISCLOSED, ARE PHOPRIETARY TO DANA LABORATORIES, INC. AND SHALL NOT, WITHOUT EXPRESS WRITTEN PERMISSION OF DANA LABORATORIES, INC. BE USED, RELEASED OR DISCLOSED IN WHOLE OR IN PART, OR USED TO SOLICIT QUOTATIONS FROM A COMPETITIVE SOURCE OR USED FOR MANUFACTURE BY ANYONE OTHER THAN DANA LABORATORIES, INC. THE INFORMATION HEREON HAS BEEN DEVELOPED AT PRIVATE EXPENSE, AND MAY ONLY BE USED FOR PURPOSES OF ENGINEERING EVALUATION AND FOR INCORPORATION INTO TECHNICAL SPECIFICATIONS AND OTHER DOCUMENTS WHICH SPECIFY PROCUREMENT OF PRODUCTS FROM DANA LABORATORIES, INC.
U10
R5
E
CR2
C11
LAST MODIFIED
DESIGNATION
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4 WATT, ±5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 100 VOLTS, ±20%.



SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	721925	D

SCALE NONE SHEET OF

NOTES: UNLESS OTHERWISE SPECIFIED

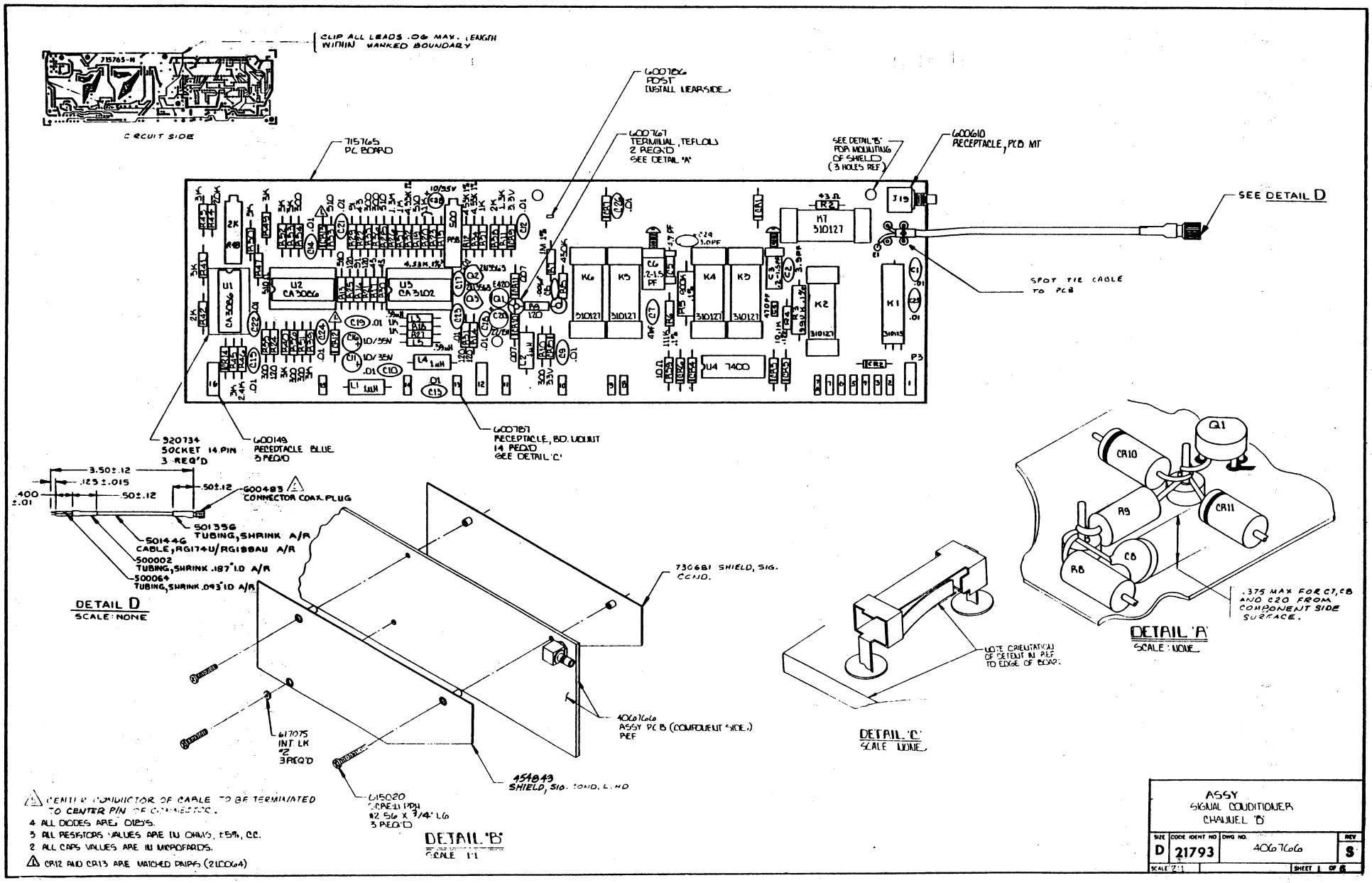


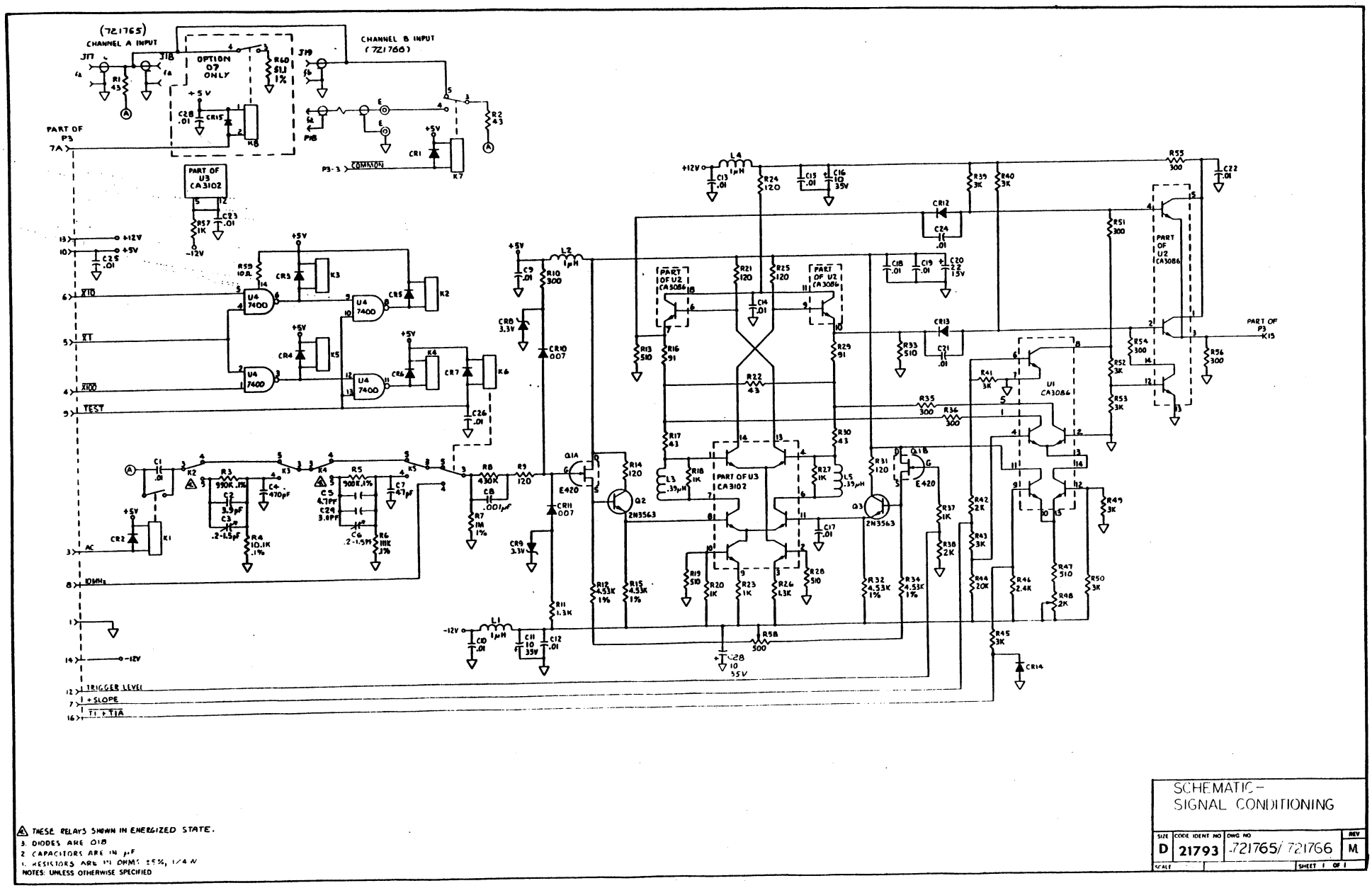
4. ALL DIODES ARE 1N914'S.
3. ALL RESISTORS VALUES ARE IN OHMS, ±5%, 1/2 W.
2. ALL CAPS VALUES ARE IN MICROFARDS.
⚠ CR12 AND CR13 ARE MATCHED PAIRS (210064)

ASSY SIGNAL CONDITIONER, CHANNEL 'A'

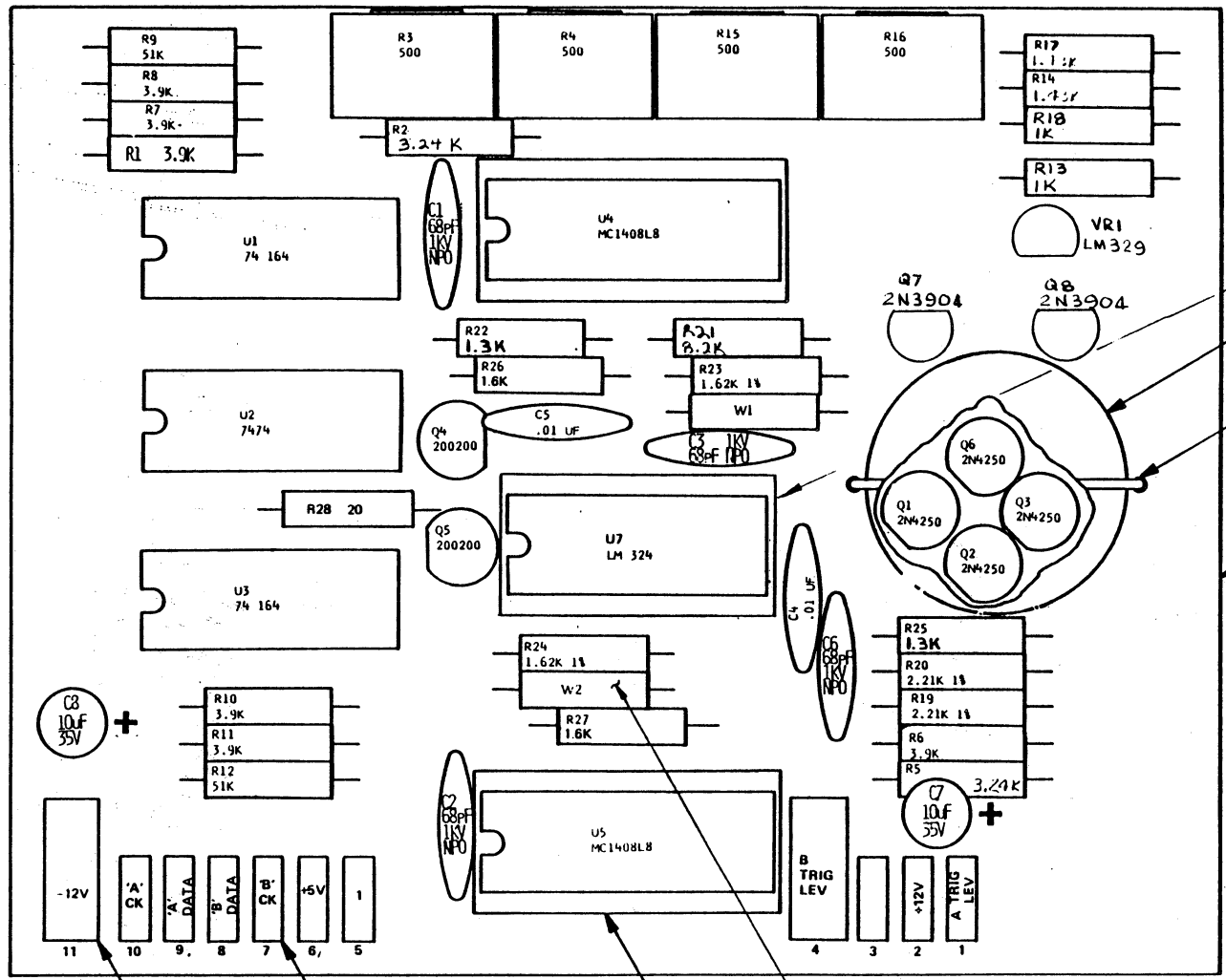
SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406765	R

SCALE 2:1 SHEET 1 OF 5

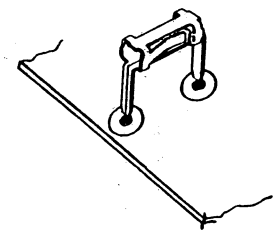

CLIP ALL LEADS .06 MAX. LENGTH WITHIN MARKED BOUNDARY
715765-M
CIRCUIT SIDE
715765 P.C. BOARD
600786 POST (INSTALL NEARSIDE)
600767 TERMINAL, TEFLON 2 REQ'D SEE DETAIL "A"
SEE DETAIL "B" FOR MOUNTING OF SHIELD (3 HOLES REF.)
600610 RECEPTACLE, PCB MT
SEE DETAIL D
SPOT TIE CABLE TO PCB
920734 SOCKET 14 PIN 3 REQ'D
600149 RECEPTACLE BLUE 5 REQ'D
600787 RECEPTACLE, BD. MOUNT 14 REQ'D SEE DETAIL 'C'
3.50±.12
.125±.015
.400 ±.01
50±.12
50±.12
600483 CONNECTOR COAX. PLUG
501356 TUBING, SHRINK A/R
501446 CABLE, RG174U/RG188AU A/R
500002 TUBING, SHRINK .187" I.D A/R
500064 TUBING, SHRINK .093" I.D A/R
DETAIL D
SCALE: NONE
730681 SHIELD, SIG. COND.
406706 ASSY PC B (COMPONENT SIDE) REF
617075 INT LK #2 3 REQ'D
454843 SHIELD, SIG. COND. L. HD
615020 SCREW PAN #2-56 X 3/4" LG 3 REQ'D
DETAIL 'B'
SCALE 1:1
CR10
Q1
R9
CR11
C8
R8
.375 MAX FOR C7, C8 AND C20 FROM COMPONENT SIDE SURFACE.
DETAIL 'A'
SCALE: NONE
NOTE ORIENTATION OF DETENT IN REF TO EDGE OF BOARD
DETAIL 'C'
SCALE NONE
1. CENTER CONDUCTOR OF CABLE TO BE TERMINATED TO CENTER PIN OF CONNECTOR.
4 ALL DIODES ARE 1N914'S.
3 ALL RESISTORS VALUES ARE IN OHMS, ±5%, 1/4W.
2 ALL CAPS VALUES ARE IN MICROFARDS.
CR12 AND CR13 ARE MATCHED PAIRS (2LC004)
ASSY SIGNAL CONDITIONER CHANNEL "B"
SIZE D
CODE IDENT NO 21793
DWG NO. 406706
REV S
SCALE 2:1
SHEET 1 OF 6



⚠ THESE RELAYS SHOWN IN ENERGIZED STATE.
3. DIODES ARE 018
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS ±5%, 1/4 W
NOTES: UNLESS OTHERWISE SPECIFIED

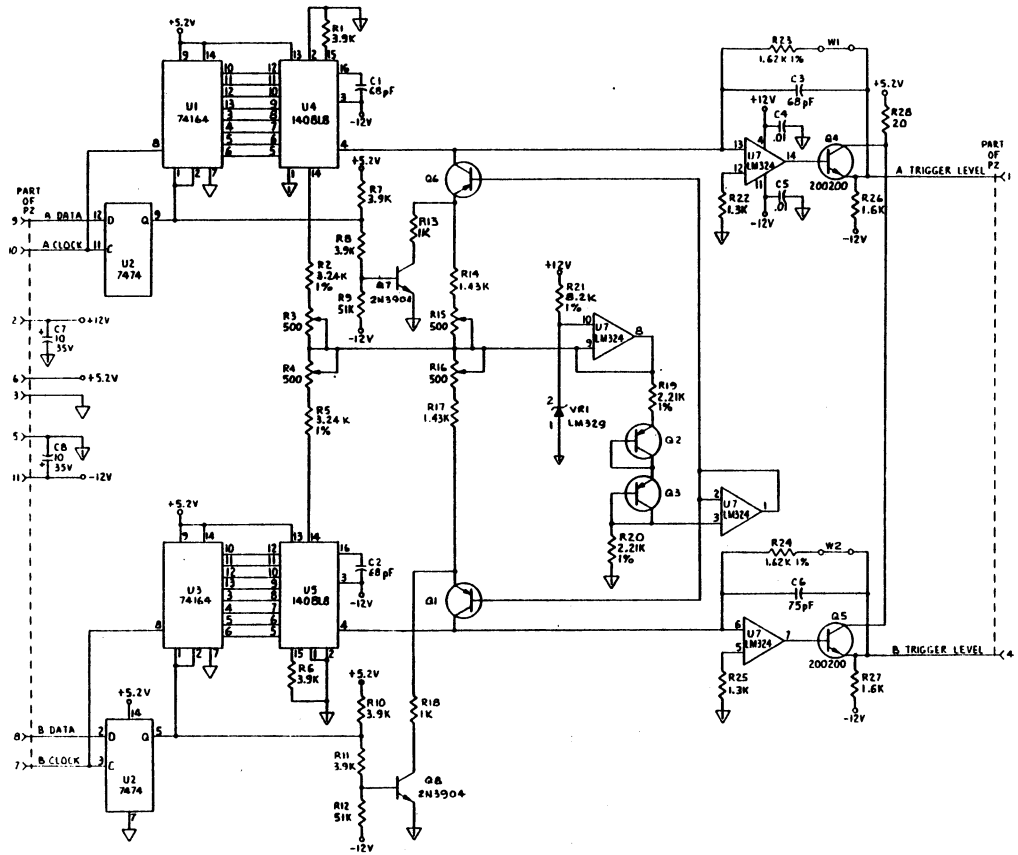


NOTE
ORIENTATION OF RECEPTACLE SHOWN IN DETAIL "A".



DETAIL "A"
NO SCALE

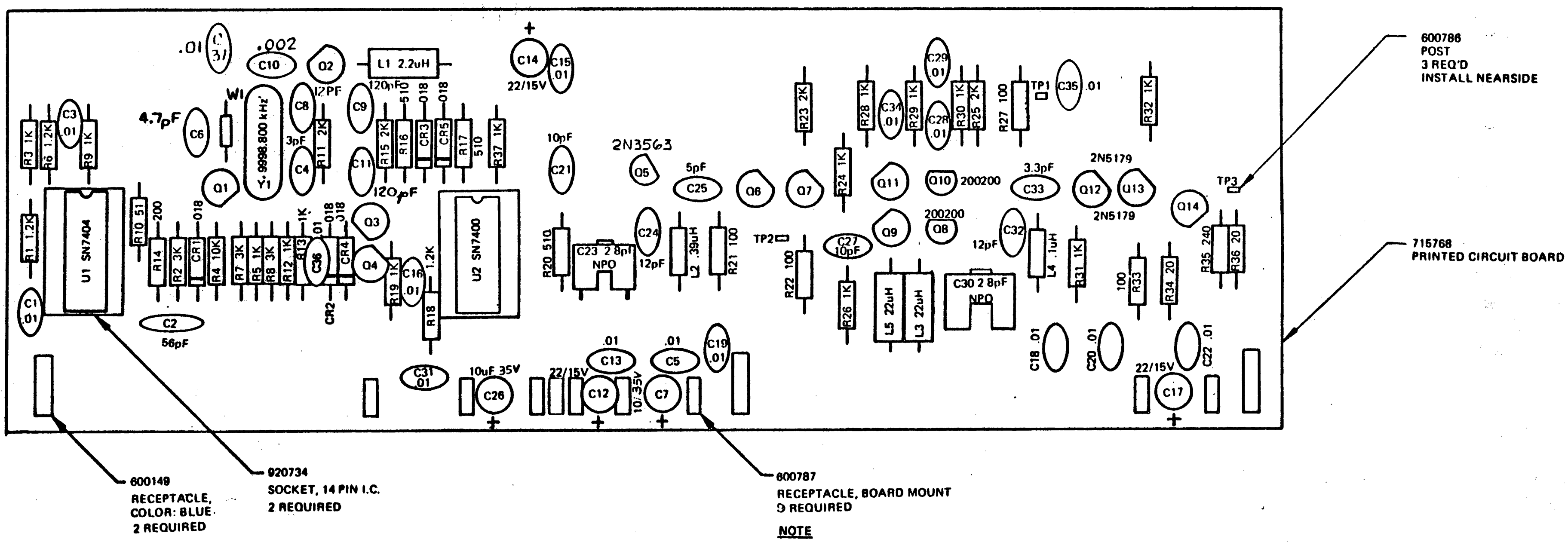
-ASSY- DAC PCB			
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406767	H
SCALE 4X		SHEET 1 OF 4	



NOTES. UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE IN OHMS, 25%, 1/4W
2. CAPACITORS ARE IN μF
3. TRANSISTORS ARE 2N4250

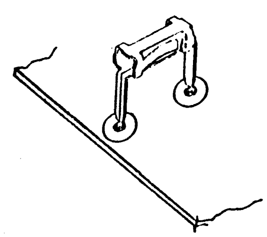
SCHEMATIC - DAC

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721767	H
SCALE		SHEET 1 OF 1	



NOTE

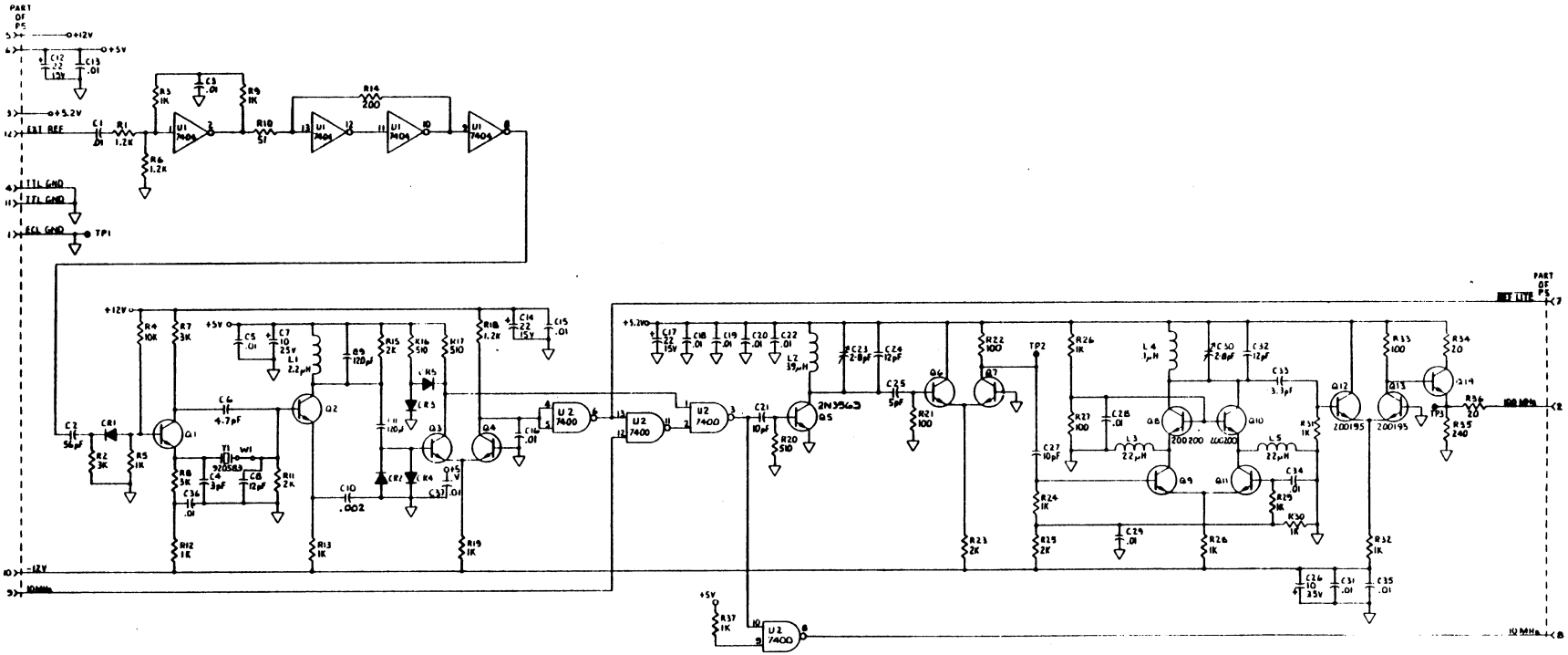
ORIENTATION OF RECEPTACLE SHOWN IN DETAIL "A".



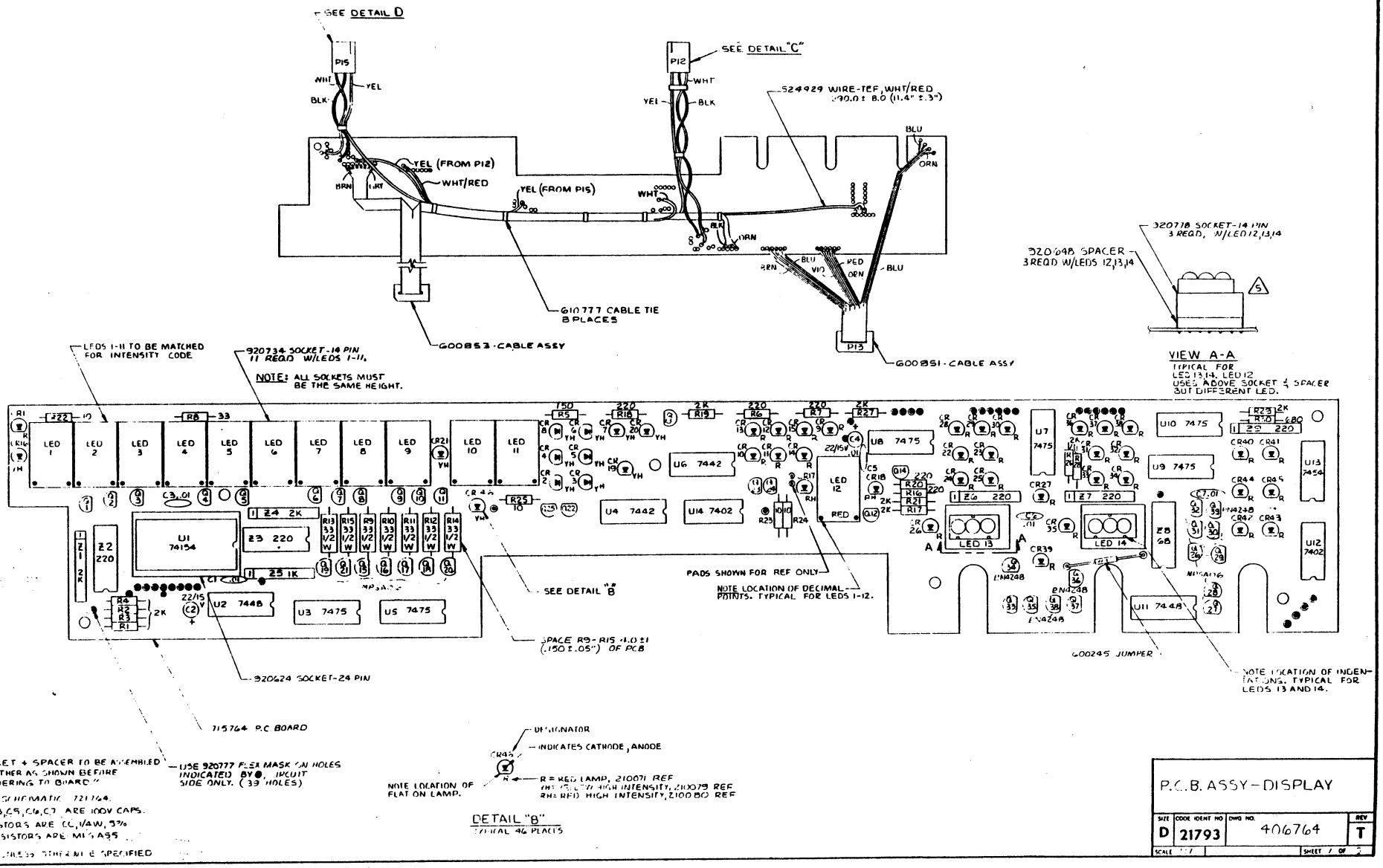
DETAIL "A"
NO SCALE

ASSY
REFERENCE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406768	N
SCALE 2:1		SHEET 1 OF 1	



5. DIODES ARE 01B
4. LAST REF. DES. USED: U36
C38
L19
L5
CR5
Q7
3. TRANSISTORS ARE 2N3646
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS ±5% 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED



5 SOCKET + SPACER TO BE ASSEMBLED TOGETHER AS SHOWN BEFORE SOLDERING TO BOARD.

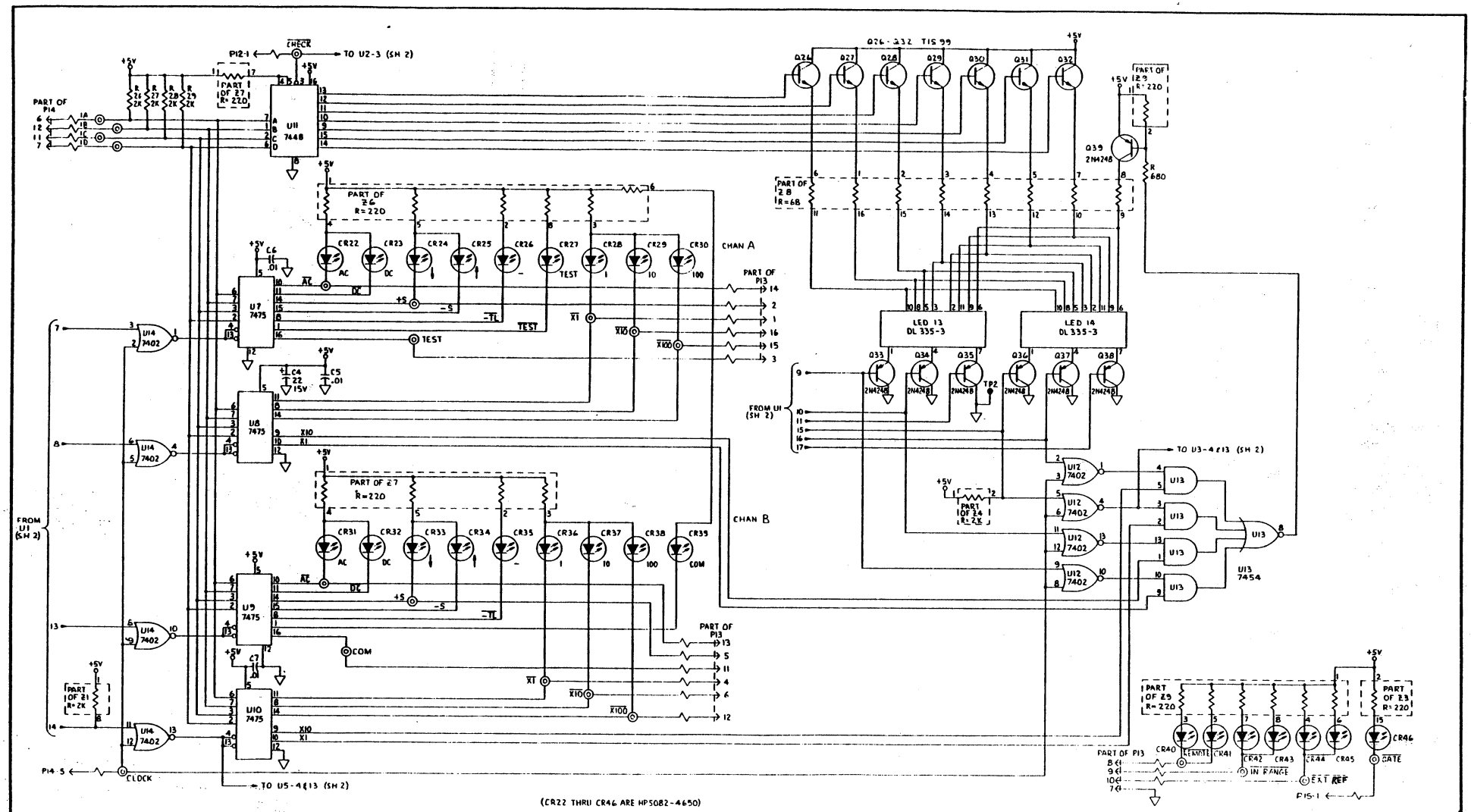
4 REF SCHEMATIC 721764.

3 C1, C3, C5, C6, C7 ARE 100V CAPS.

2 RESISTORS ARE EC, 1/4W, 5%

1 TRANSISTORS ARE MPS A55

NOTES: UNLESS OTHERWISE SPECIFIED

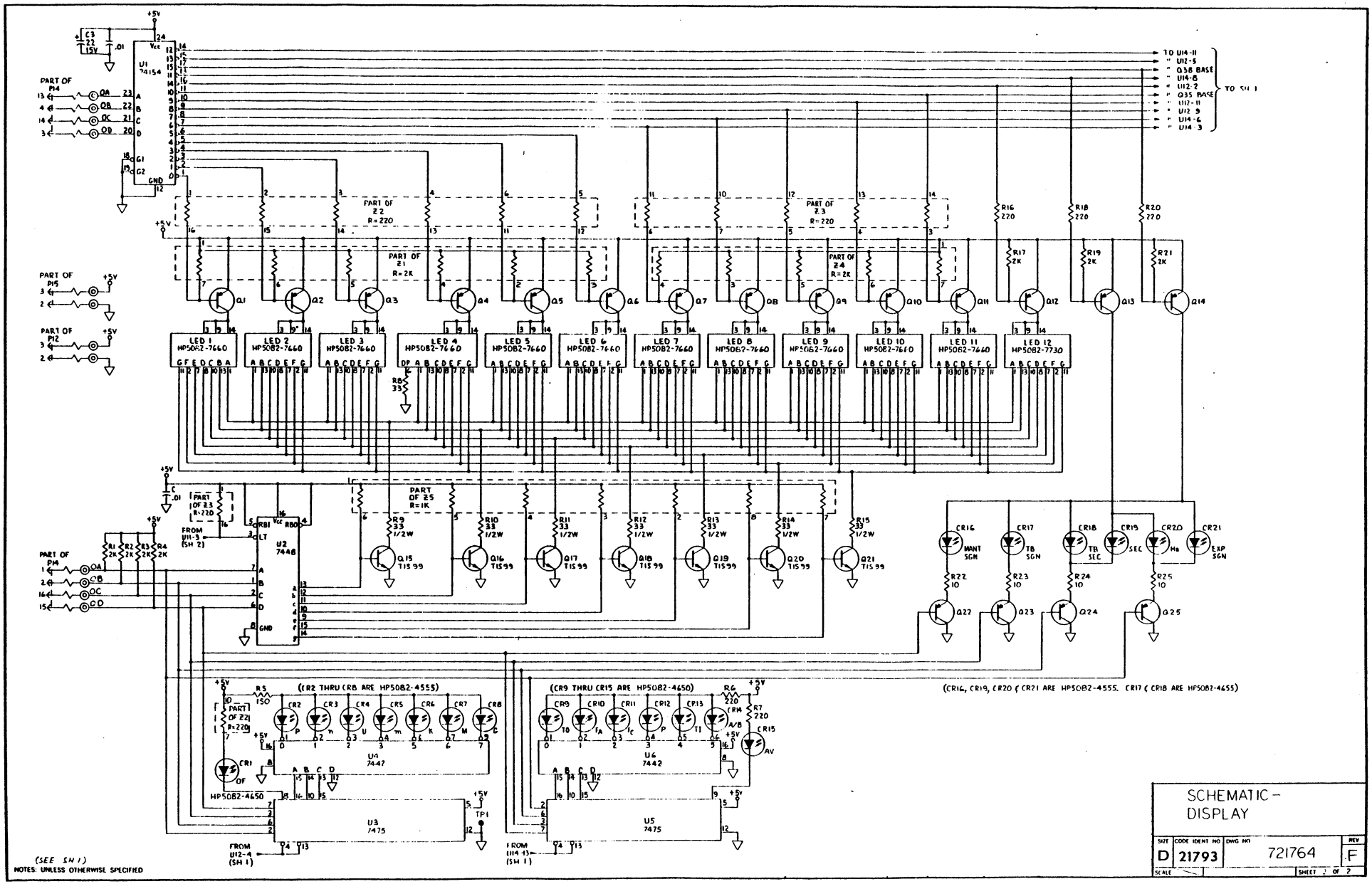


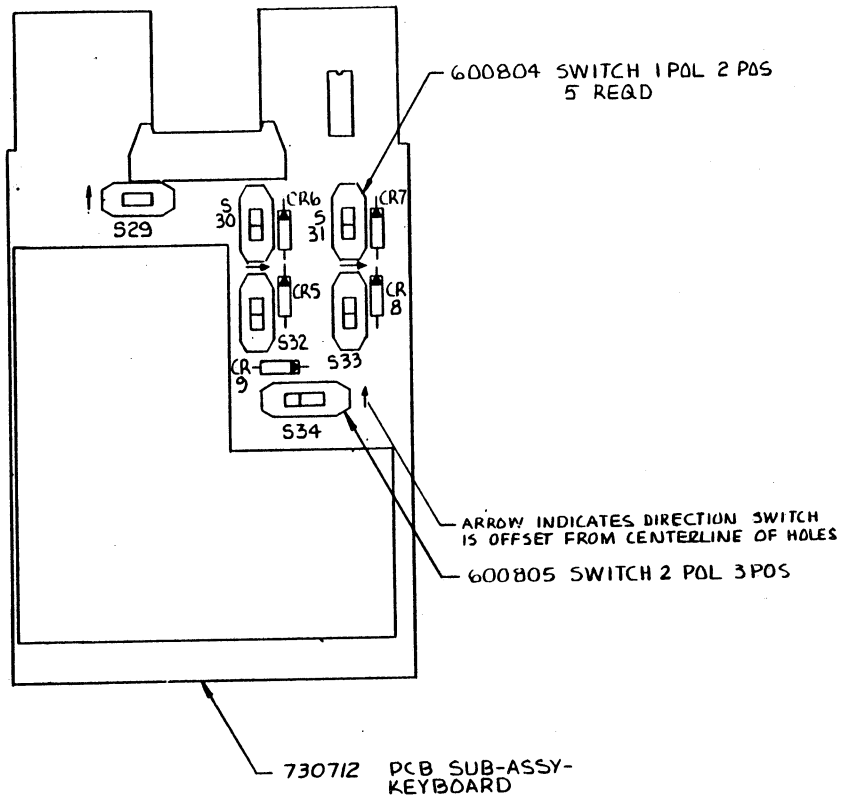
3. TRANSISTORS ARE MPS-A55
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC – DISPLAY

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721764	F

SCALE | SHEET 1 OF 2


SCHEMATIC – DISPLAY
SIZE D
CODE IDENT NO 21793
DWG NO 721764
REV F
SCALE
SHEET 1 OF 2
(SEE SH 1)
NOTES: UNLESS OTHERWISE SPECIFIED
(CR2 THRU CR8 ARE HP5082-4555)
(CR9 THRU CR15 ARE HP5082-4650)
(CR16, CR19, CR20 & CR21 ARE HP5082-4555. CR17 & CR18 ARE HP5082-4655)
TO SH 1
FROM SH 1



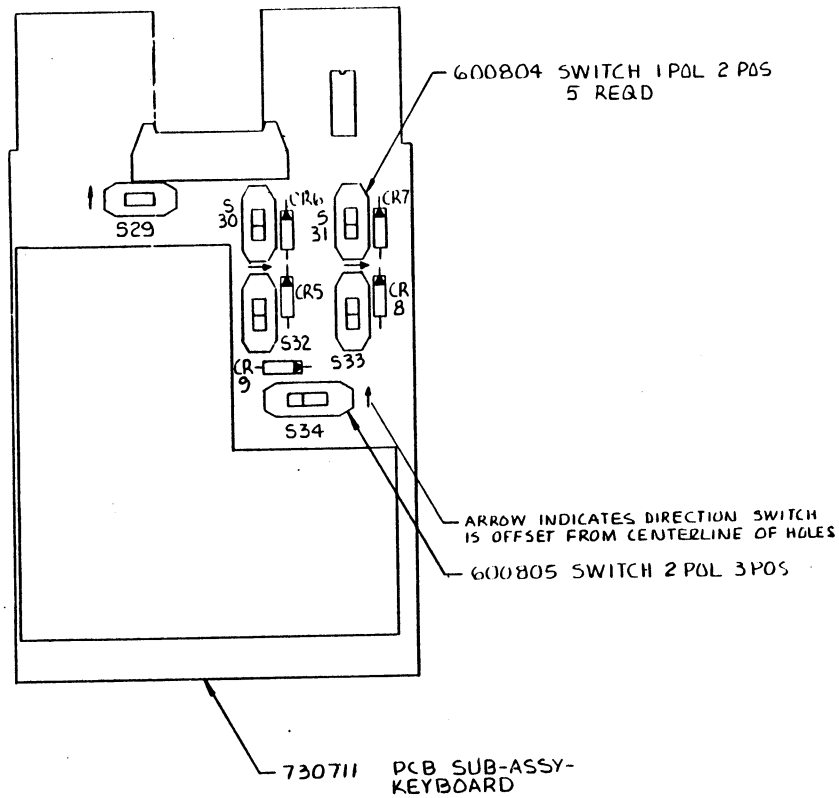
1. DIODES ARE 018.

NOTES: UNLESS OTHERWISE SPECIFIED

PCB ASSY-KEYBOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406831	A

SCALE NONE SHEET 1 OF 2



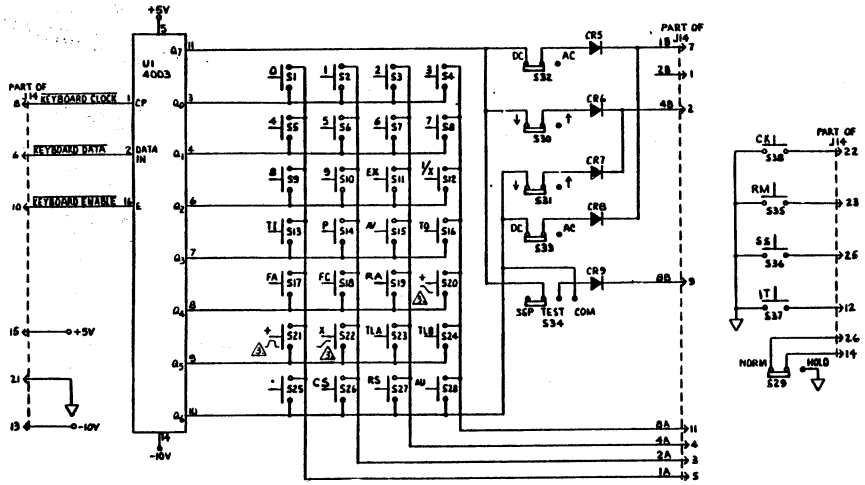
1. DIODES ARE 018.

NOTES: UNLESS OTHERWISE SPECIFIED

PCB ASSY-KEYBOARD
OPTION 11

SIZE	CODE IDENT NO	DWG NO	REV
C	21793	406832	A

SCALE AS MAY BE | SHEET 1 OF 2

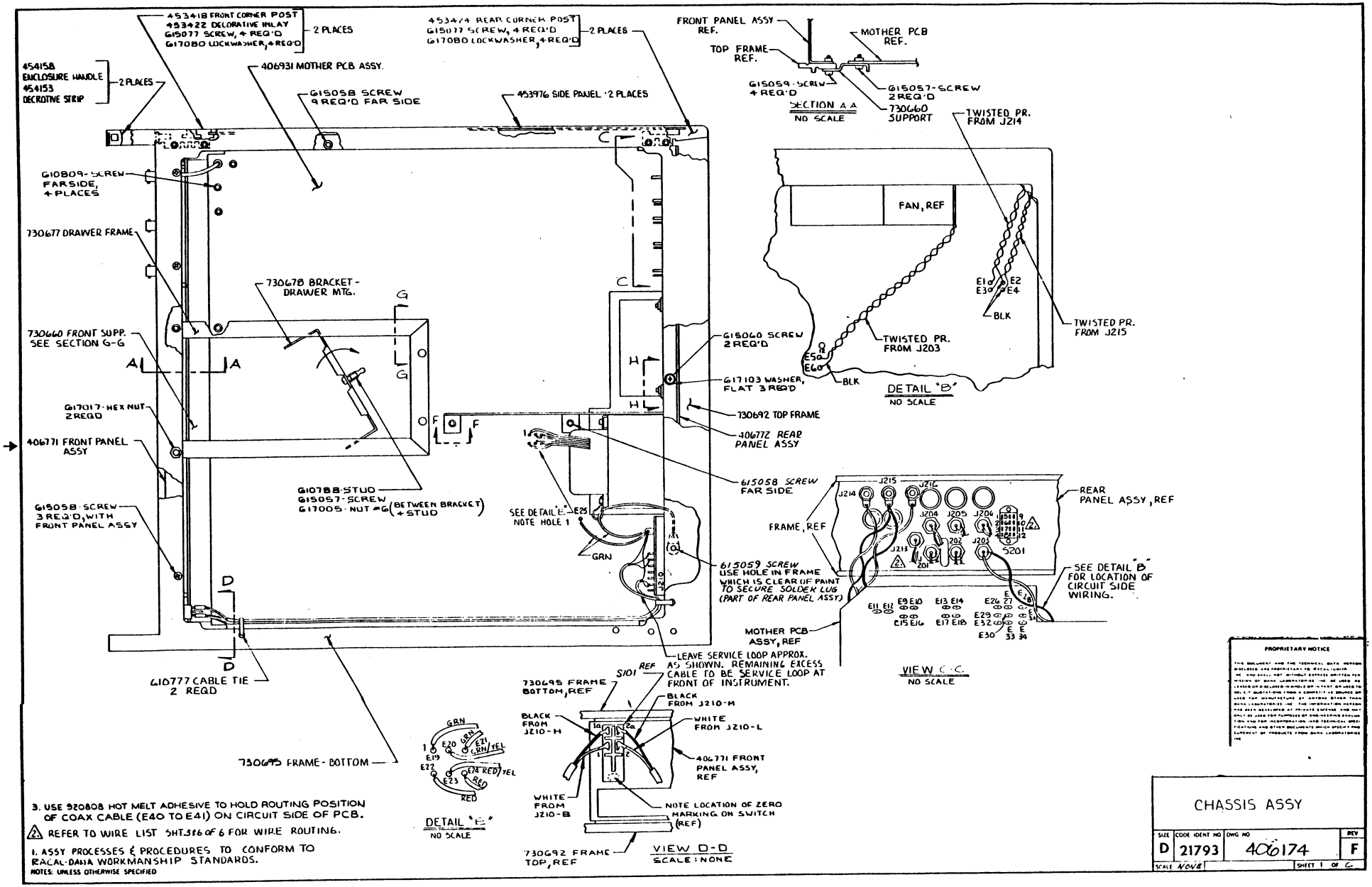


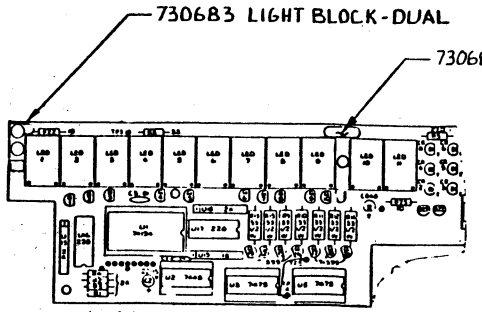
NOTES: UNLESS OTHERWISE SPECIFIED
1. DIODES ARE DIB.
2. RESISTORS ARE 1/4 W, 5%.
3. USED WITH OPTION 11.

SCHEMATIC - KEYBOARD

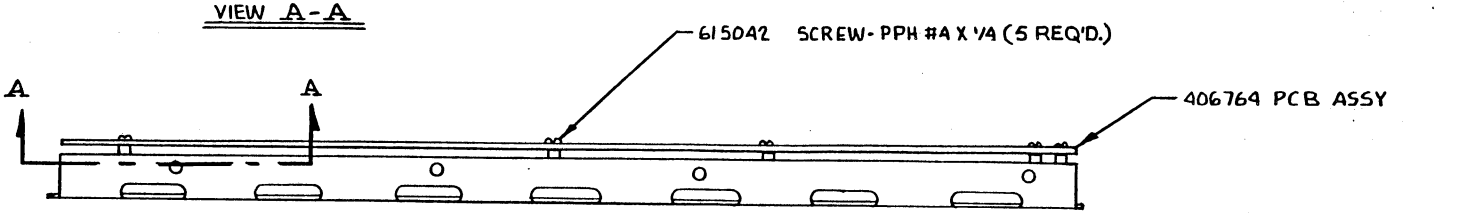
SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	721831	C

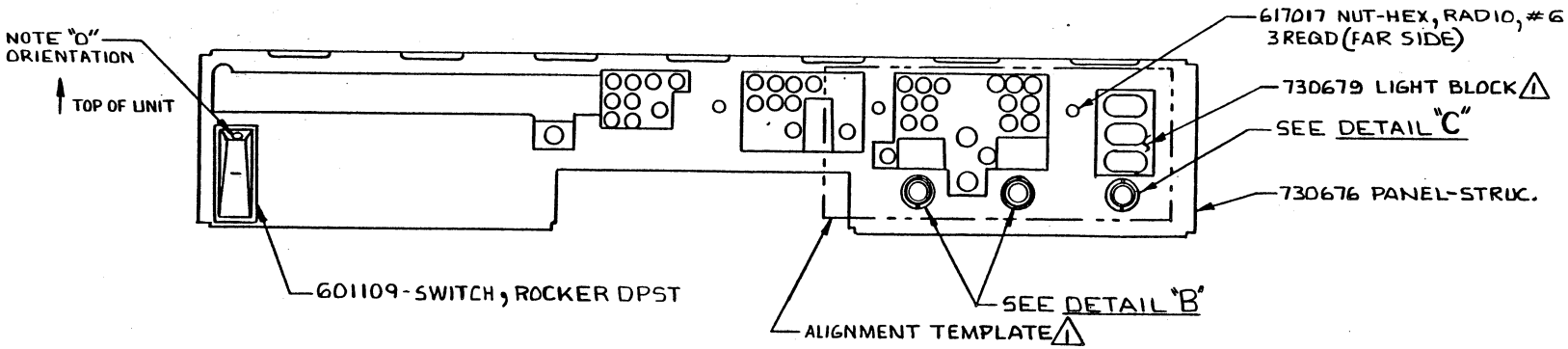
SCALE NONE SHEET 1 OF 1


453418 FRONT CORNER POST
453422 DECORATIVE INLAY
615077 SCREW, 4 REQ'D
617080 LOCKWASHER, 4 REQ'D
2 PLACES
453474 REAR CORNER POST
615077 SCREW, 4 REQ'D
617080 LOCKWASHER, 4 REQ'D
2 PLACES
454158 ENCLOSURE HANDLE
454153 DECROTIVE STRIP
2 PLACES
406931 MOTHER PCB ASSY.
615058 SCREW 9 REQ'D FAR SIDE
453976 SIDE PANEL 2 PLACES
610809 SCREW FARSIDE, 4 PLACES
730677 DRAWER FRAME
730678 BRACKET - DRAWER MTG.
730660 FRONT SUPP. SEE SECTION G-G
617017 HEX NUT 2 REQD
406771 FRONT PANEL ASSY
615058 SCREW 3 REQ'D, WITH FRONT PANEL ASSY
610788 STUD
615057 SCREW
617005 NUT (BETWEEN BRACKET + STUD)
610777 CABLE TIE 2 REQD
730695 FRAME - BOTTOM
615060 SCREW 2 REQ'D
617103 WASHER, FLAT 3 REQ'D
730692 TOP FRAME
406772 REAR PANEL ASSY
615058 SCREW FAR SIDE
615059 SCREW USE HOLE IN FRAME WHICH IS CLEAR OF PAINT TO SECURE SOLDER LUG (PART OF REAR PANEL ASSY)
SEE DETAIL "E" NOTE HOLE 1
GRN
LEAVE SERVICE LOOP APPROX. AS SHOWN. REMAINING EXCESS CABLE TO BE SERVICE LOOP AT FRONT OF INSTRUMENT.
MOTHER PCB ASSY, REF
FRONT PANEL ASSY REF.
TOP FRAME REF.
MOTHER PCB REF.
615059 SCREW 4 REQ'D
615057 SCREW 2 REQ'D
730660 SUPPORT
SECTION A A
NO SCALE
TWISTED PR. FROM J214
FAN, REF
TWISTED PR. FROM J203
TWISTED PR. FROM J215
BLK
DETAIL "B"
NO SCALE
REAR PANEL ASSY, REF
FRAME, REF
J215
J216
J214
J204
J205
J213
J201
J202
J203
S201
SEE DETAIL "B" FOR LOCATION OF CIRCUIT SIDE WIRING.
VIEW C-C
NO SCALE
730695 FRAME BOTTOM, REF
S101 REF
BLACK FROM J210-M
WHITE FROM J210-L
BLACK FROM J210-H
406771 FRONT PANEL ASSY, REF
WHITE FROM J210-B
NOTE LOCATION OF ZERO MARKING ON SWITCH (REF)
730692 FRAME TOP, REF
VIEW D-D
SCALE: NONE
DETAIL "E"
NO SCALE
3. USE 920808 HOT MELT ADHESIVE TO HOLD ROUTING POSITION OF COAX CABLE (E40 TO E41) ON CIRCUIT SIDE OF PCB.
⚠ REFER TO WIRE LIST SHT 3 & 6 OF 6 FOR WIRE ROUTING.
1. ASSY PROCESSES & PROCEDURES TO CONFORM TO RACAL-DANA WORKMANSHIP STANDARDS.
NOTES: UNLESS OTHERWISE SPECIFIED
PROPRIETARY NOTICE
CHASSIS ASSY
SIZE D
CODE IDENT NO 21793
DWG NO 406174
REV F
SCALE NONE
SHEET 1 OF 6



VIEW A-A





⚠4 STRIP LENGTH .3 ± 1/32", 2 PLACES. SEE SHT 3 OF 4.

3. CENTER CONDUCTOR OF CABLE TO BE TERMINATED TO CENTER PIN OF CONN. TYP. SEE SHT 3 OF 4.
2. USE LOCTITE ON ALL MOUNTING SCREWS.

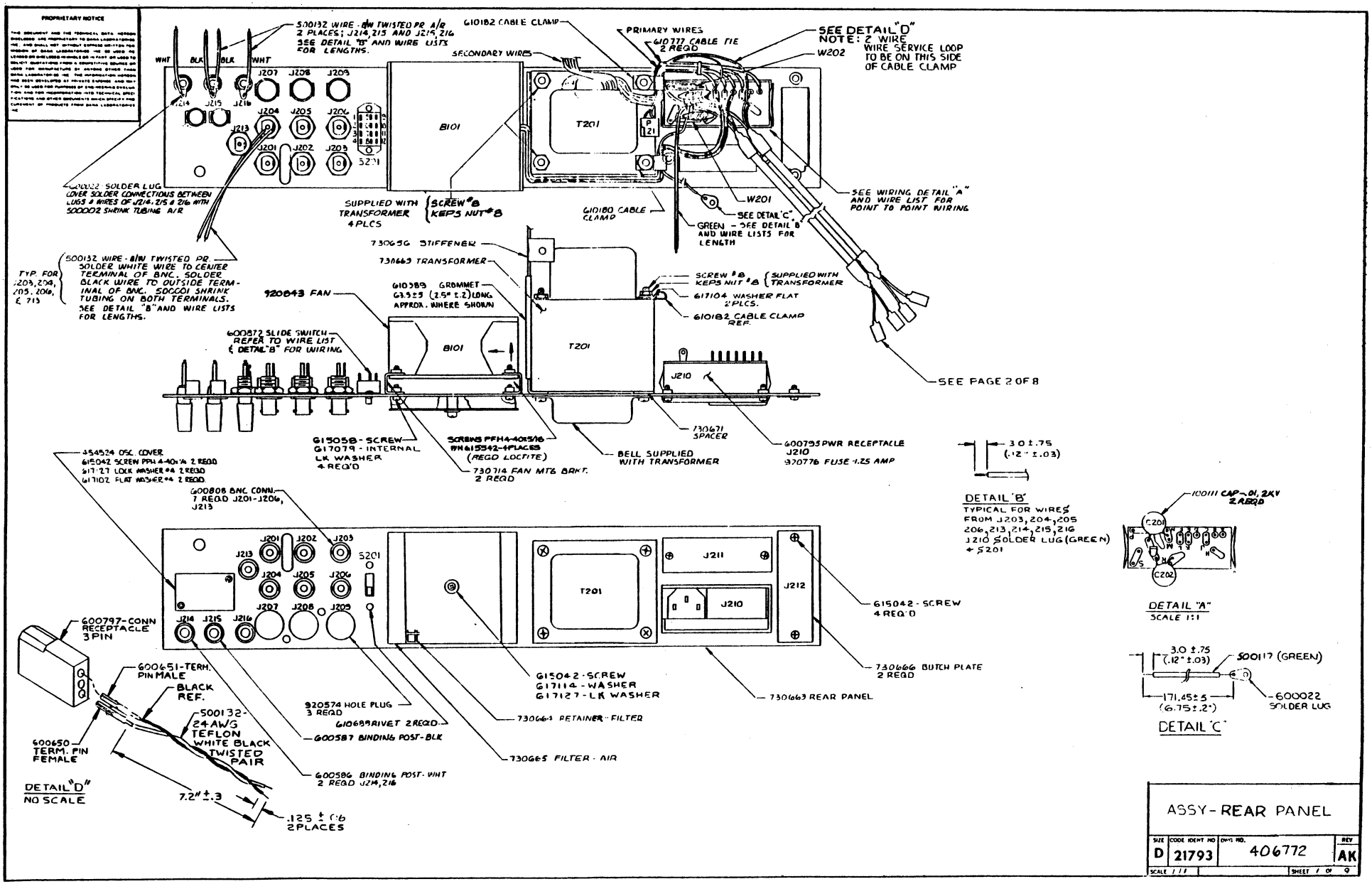
⚠1 LIGHT BLOCK TO BE POSITIONED USING TEMPLATE AS SHOWN SHT 2 OF 4.

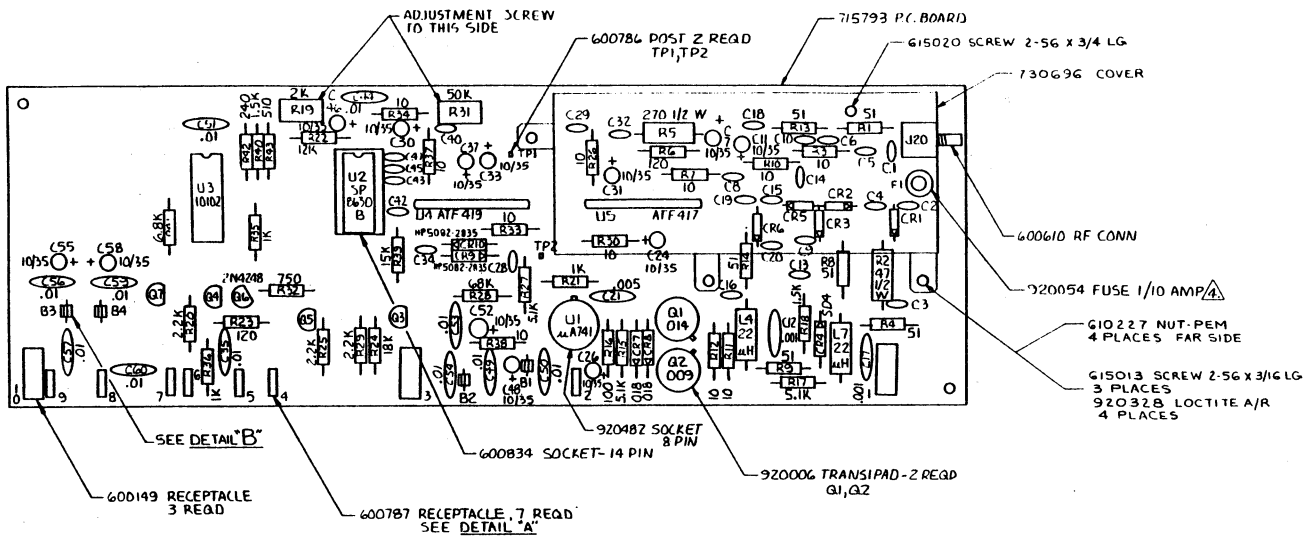
NOTES: UNLESS OTHERWISE SPECIFIED

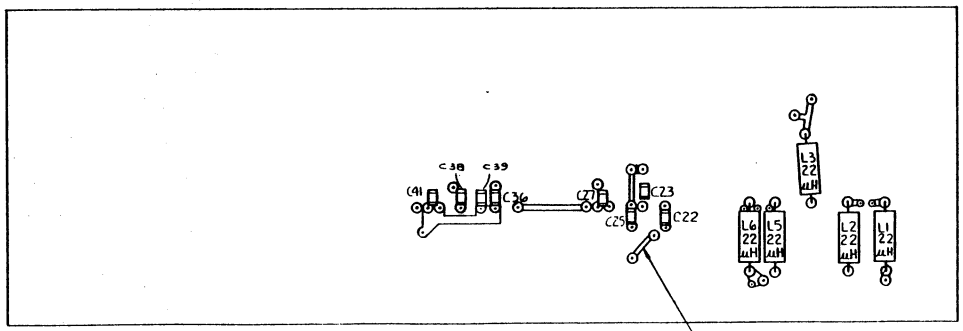
PANEL ASSY-FRONT

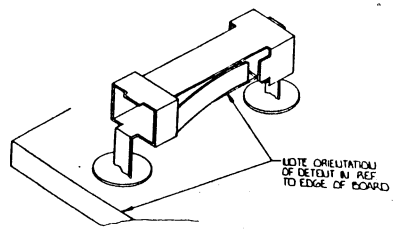
SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406771	K

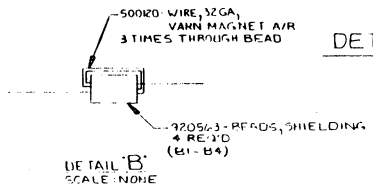
SCALE NONE | SHEET 1 OF 4


PROPRIETARY NOTICE
500132 WIRE - 8IN TWISTED PR A/R 2 PLACES; J214,215 AND J215,216 SEE DETAIL "B" AND WIRE LISTS FOR LENGTHS.
610182 CABLE CLAMP
PRIMARY WIRES
610777 CABLE TIE 2 REQD
SECONDARY WIRES
SEE DETAIL "D" NOTE: 2 WIRE WIRE SERVICE LOOP TO BE ON THIS SIDE OF CABLE CLAMP
W202
WHT BLK BLK WHT
J207 J208 J209
J214 J215 J216
J204 J205 J206
J213
J201 J202 J203
S201
B101
T201
P 21
600022 SOLDER LUG LOWER SOLDER CONNECTIONS BETWEEN LUGS & WIRES OF J214,215 & 216 WITH 500002 SHRINK TUBING A/R
SUPPLIED WITH TRANSFORMER 4 PLCS
SCREW #8
KEPS NUT #8
610180 CABLE CLAMP
W201
SEE DETAIL "C"
GREEN - SEE DETAIL B AND WIRE LISTS FOR LENGTH
SEE WIRING DETAIL "A" AND WIRE LIST FOR POINT TO POINT WIRING
TYP. FOR J203, 204, 205, 206, & 213
500132 WIRE - 8IN TWISTED PR. SOLDER WHITE WIRE TO CENTER TERMINAL OF BNC. SOLDER BLACK WIRE TO OUTSIDE TERMINAL OF BNC. SOCCOI SHRINK TUBING ON BOTH TERMINALS. SEE DETAIL "B" AND WIRE LISTS FOR LENGTHS.
730656 STIFFENER
730663 TRANSFORMER
920643 FAN
610389 GROMMET G3.5±5 (2.5" ±.2) LONG APPROX. WHERE SHOWN
SCREW #8
KEPS NUT #8
(SUPPLIED WITH TRANSFORMER)
617104 WASHER FLAT 2 PLCS.
610182 CABLE CLAMP REF.
600872 SLIDE SWITCH REFER TO WIRE LIST & DETAIL "B" FOR WIRING
J210
SEE PAGE 2 OF 8
615058 - SCREW G17079 - INTERNAL LK WASHER 4 REQ'D
SCREWS PFH4-40X5/16 PN 615542-4 PLACES (REQD LOCTITE)
730714 FAN MTG BRKT. 2 REQD
BELL SUPPLIED WITH TRANSFORMER
730671 SPACER
600795 PWR RECEPTACLE J210
920776 FUSE 1.25 AMP
3.0 ±.75 (.12" ±.03)
DETAIL "B" TYPICAL FOR WIRES FROM J203, 204, 205 206, 213, 214, 215, 216 J210 SOLDER LUG (GREEN) & S201
354524 OSC. COVER
615042 SCREW PPH 4-40X1/4 2 REQD
617127 LOCK WASHER #4 2 REQD
617102 FLAT WASHER #4 2 REQD.
600808 BNC CONN. 7 REQD J201-J206, J213
J211
J212
T201
J210
615042 - SCREW 4 REQ'D
730666 BUTCH PLATE 2 REQD
730663 REAR PANEL
615042 - SCREW G17114 - WASHER G17127 - LK WASHER
730664 RETAINER - FILTER
730665 FILTER - AIR
920574 HOLE PLUG 3 REQD
610689 RIVET 2 REQD
600587 BINDING POST - BLK
600586 BINDING POST - WHT 2 REQD J214,216
600797 - CONN RECEPTACLE 3 PIN
600651 - TERM. PIN MALE
BLACK REF.
500132 - 24 AWG TEFLON WHITE BLACK TWISTED PAIR
600650 TERM. PIN FEMALE
7.2" ±.3
.125 ± .06 2 PLACES
DETAIL "D" NO SCALE
100111 CAP - .01, 2KV 2 REQD
C201
C202
DETAIL "A" SCALE 1:1
3.0 ±.75 (.12" ±.03)
500117 (GREEN)
171.45±5 (6.75±.2")
600022 SOLDER LUG
DETAIL "C"
ASSY - REAR PANEL
SIZE D
CODE IDENT NO 21793
DWG NO. 406772
REV AK
SCALE 1/1
SHEET 1 OF 9







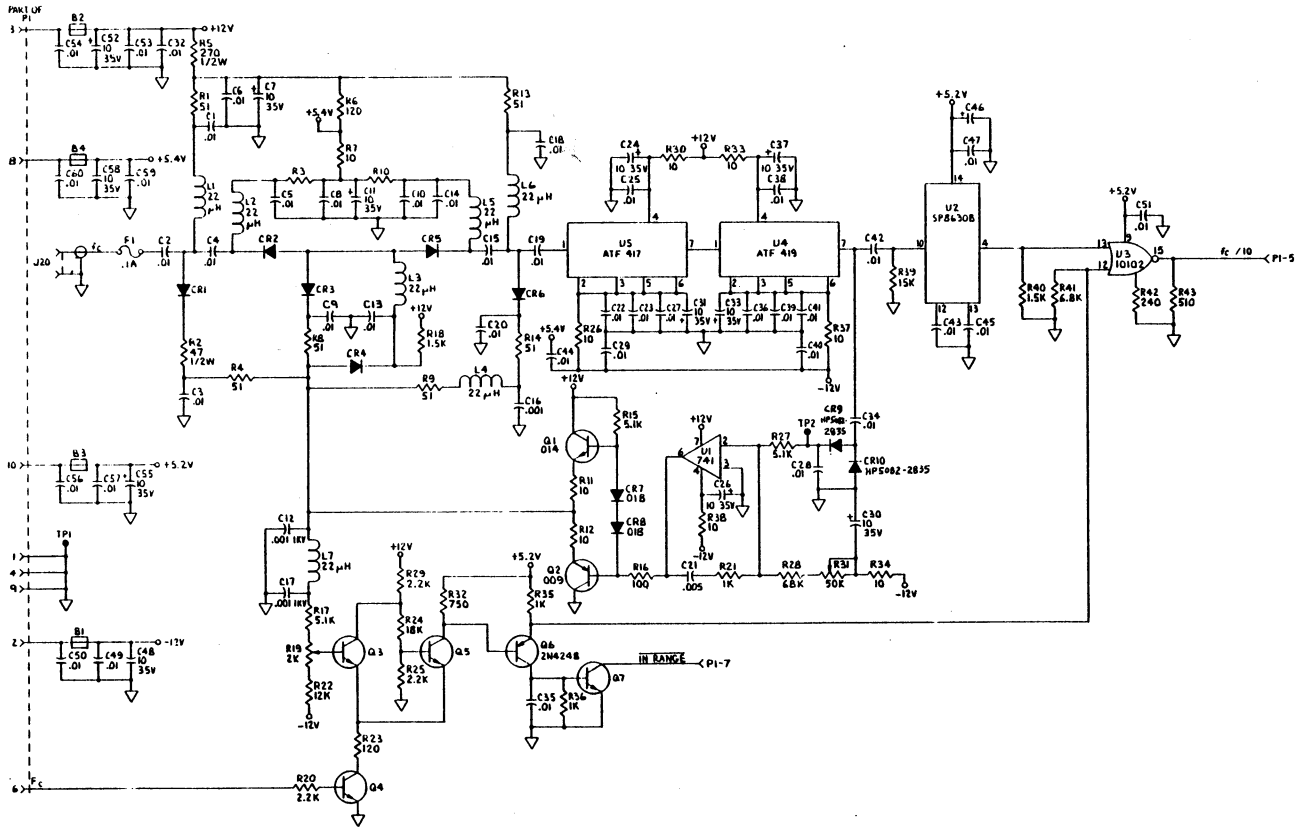


4 FUSE F1 IS A HEAT SENSITIVE DEVICE. INSTALL WITH 0.015" CLEARANCE OFF PC BOARD AND USE HEAT SHUNT WHILE SOLDERING LEADS.
3. TRANSISTORS ARE 200200.
2. CAPS ARE .01.
1. ALL DIODES ARE 30A0.
NOTES UNLESS OTHERWISE SPECIFIED

PCB ASSY - 512 MHz PRESCALER

SIZE	CODE IDENT NO	ENG NO	REV
D	21793	406193	J

SHEET 1 OF 3

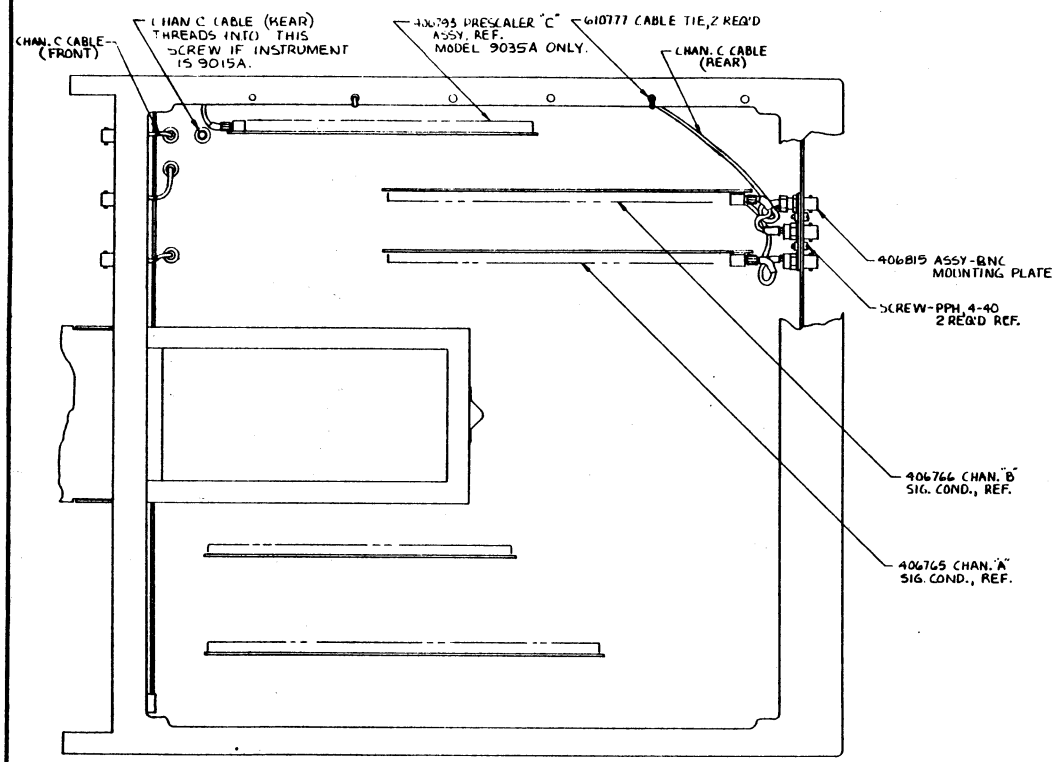


SCHEMATIC-
PRESCALER

SIZE	CODE IDENT. NO	REV
D	21793	C

721793

SCALE: 1 SHEET 1 OF 1



ASSEMBLY INSTRUCTIONS

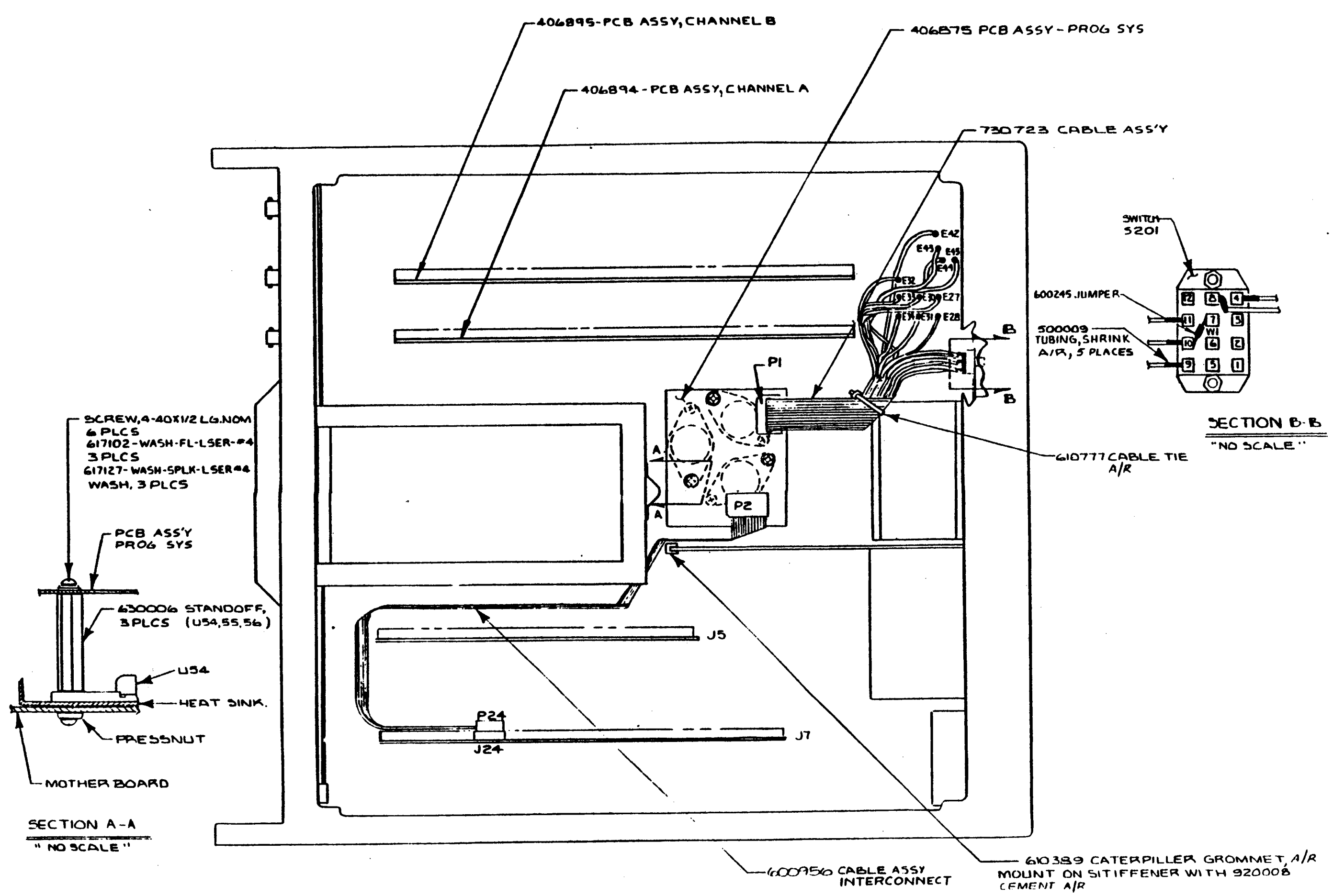
1. DISCONNECT CABLES FROM CHAN. A CHAN. B & CHAN. C P.C. BOARDS. THREAD CABLES INTO SCREWS AS SHOWN. NOTE: IF INSTRUMENT IS MODEL 9015 OR 9015A CHAN. C CABLE IS ALREADY SECURED.
2. UNPLUG CHAN. A & CHAN. B P.C. BOARDS. PLUG BOARDS BACK INTO MOTHER P.C. BOARD IN POSITION SHOWN.
3. DELETE 3 HOLE PLUGS IN REAR PANEL FOR CHAN. A, B, & C MOUNTING HOLES IF INSTRUMENT IS MODEL 9015.
4. MOUNT BNC MOUNTING PLATE ASSY TO REAR PANEL AS SHOWN OR 9015A CHAN. C CABLE IS ALREADY SECURED.
5. RECONNECT CABLES FROM BNC MOUNTING PLATE ASSY TO APPROPRIATE P.C. BOARDS AS SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSY-REAR INPUT, OPTION 01

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406803	C

SCALE 4"/IN" | SHEET 1 OF 2



3. COMPLETELY REMOVE ALL EXISTING S201 WIRING BEFORE REWIRING AS SHOWN ON THIS DRAWING.

2. TYPE OPTION NO. 06PA ON SERIAL NO. TAG USED ON BASIC ASSY UNIT.

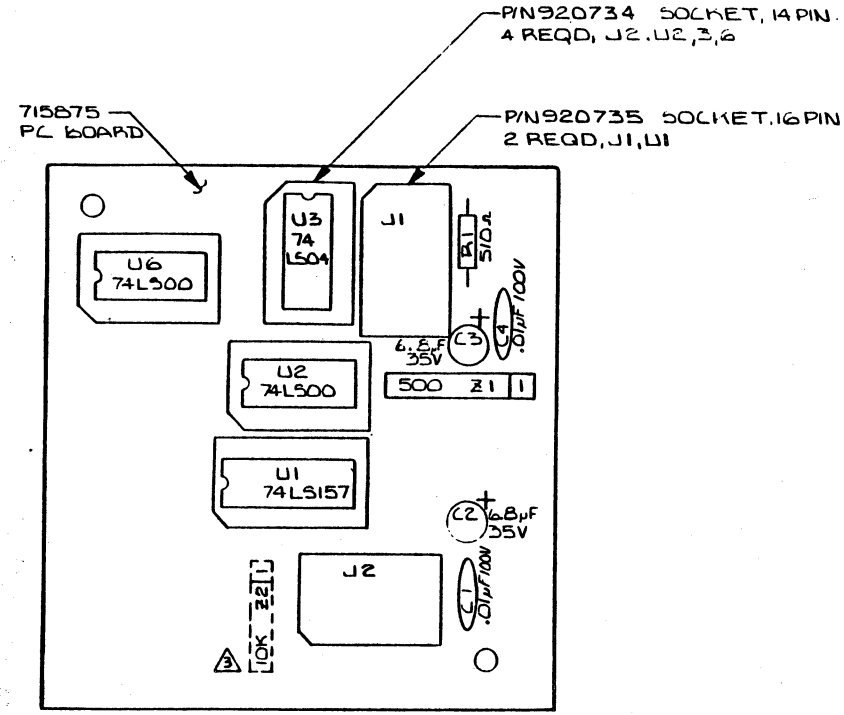
1. ASSY PROCESSES & PROCEDURES TO CONFORM TO RACAL-DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

PROGRAMMABLE SYNCHRONOUS WINDOW AND SELECTIVE GATE CONTROL ASS'Y-OPT 06PA

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	406737	D

SCALE | SHEET 1 OF 3



3 Z2 P/N 080005 MUST BE INSTALLED WHEN RETRO-FITTING ASSY TO 9000 SERIES P/N 406770 & 406802.

2. ALL RESISTORS VALUES ARE IN OHMS, ±5%, CC.

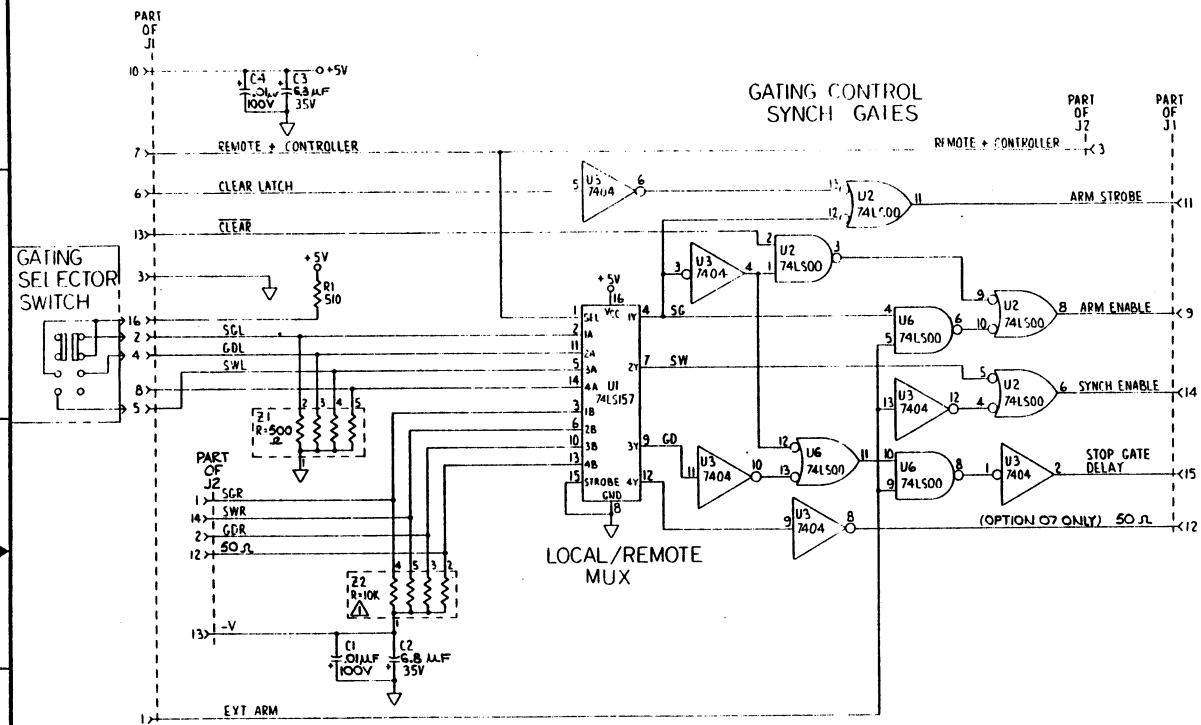
1. ALL CAPS VALUES ARE IN MICROFARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSY PC BOARD
PROGRAMABLE SYNCHRONOUS. WINDOW & SELECTIVE GATE CONTROL

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406875	B

SCALE 2/1 SHEET 1 OF 2



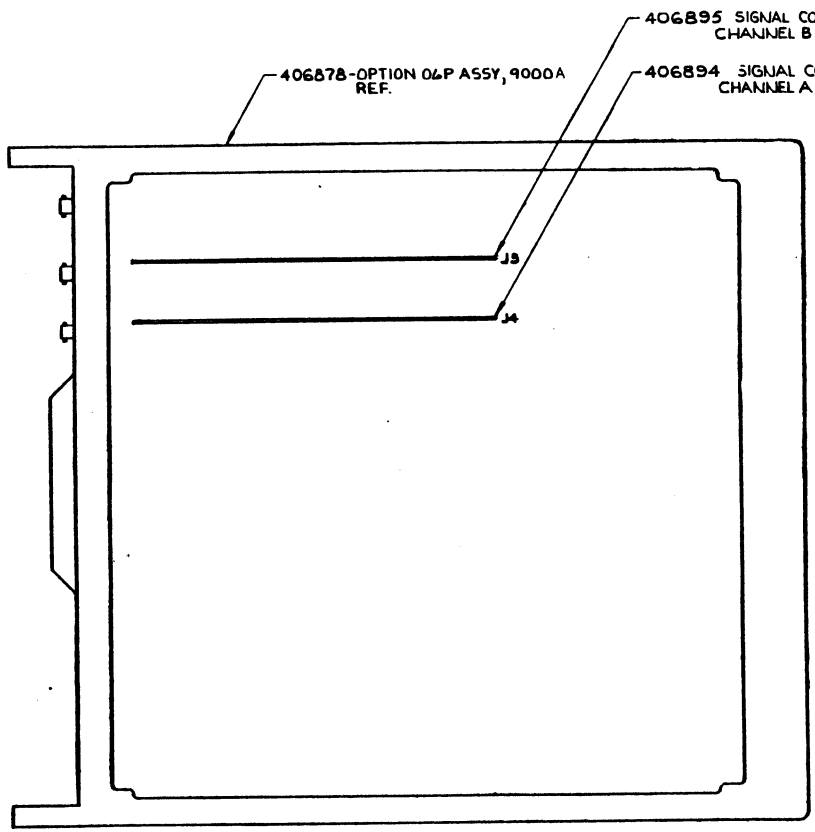
⚠ Z2 P/N 080005 MUST BE INSTALLED WHEN RETRO FITTING ASSEMBLY TO 9000 SERIES H/N 406770 AND 406802.

NOTES. UNLESS OTHERWISE SPECIFIED

MODEL 9000 OPT 06P
PROGRAMMABLE SYNCHRONOUS WINDOW AND SELECTIVE GATE CONTROL

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	721875	H

SHEET 1 OF 1



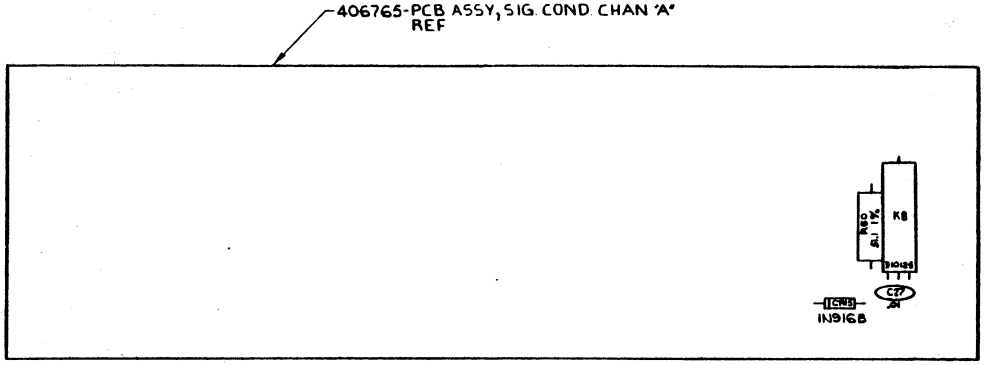
1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARD.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSY-9000A OPT. 07
PROGRAMMABLE 50Ω

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	406896	B

SCALE NONE SHEET 1 OF 2



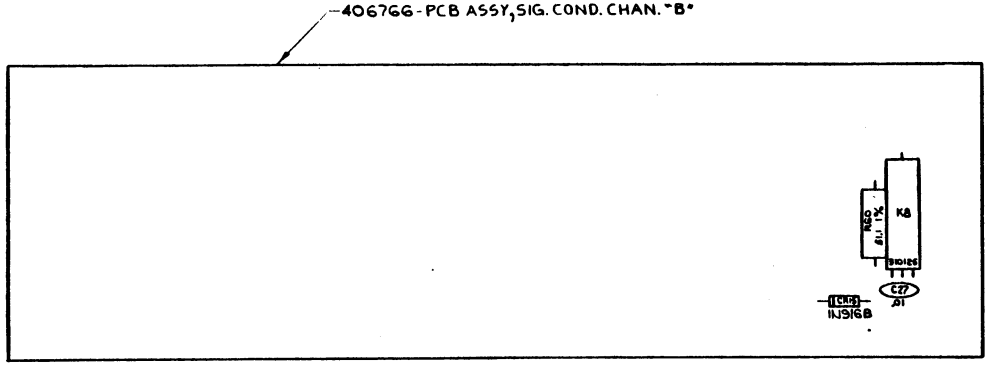
NOTES. UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PROCEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.
2. REFERENCE SCHEMATIC NUMBER 721765.
3. ADD COMPONENTS AS SHOWN.

ASSEMBLY-P.C. BOARD
SIGNAL CONDITIONER
CHANNEL "A" OPTION 07

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	406894	B

SCALE 2/1 SHEET 1 OF 2



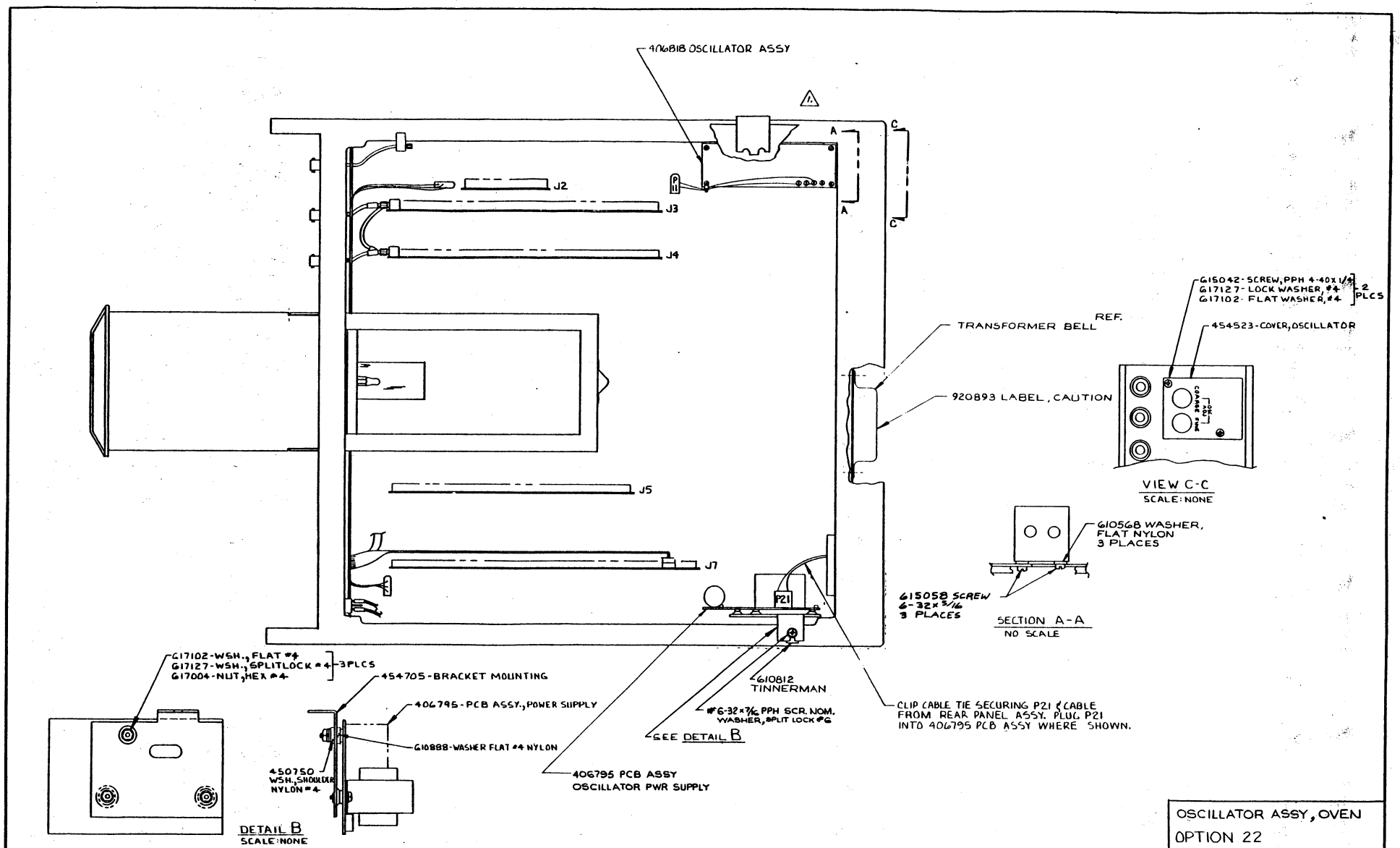
3. ADD COMPONENTS AS SHOWN.
2. REFERENCE SCHEMATIC NUMBER 721766.
1. ASSEMBLY PROCEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES. UNLESS OTHERWISE SPECIFIED

ASSEMBLY-P.C. BOARD
SIGNAL CONDITIONER
CHANNEL "B" OPTION 07

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406895	B

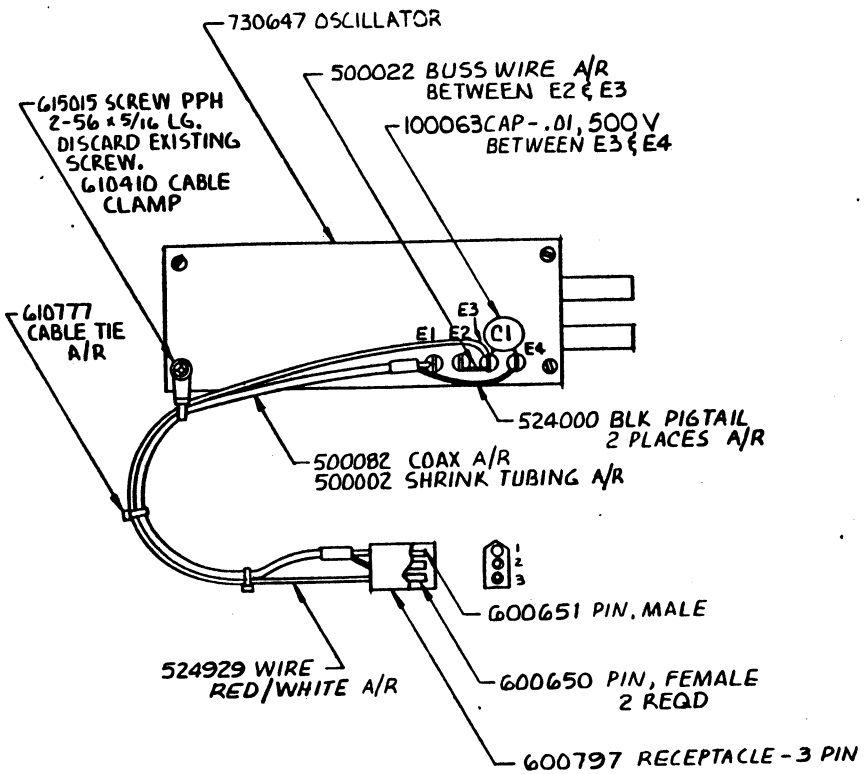
SCALE 2/1 SHEET 1 OF 2



OSCILLATOR ASSY, OVEN
OPTION 22

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406805	H

SCALE NONE — SHEET 1 OF 2



WIRE LENGTHS

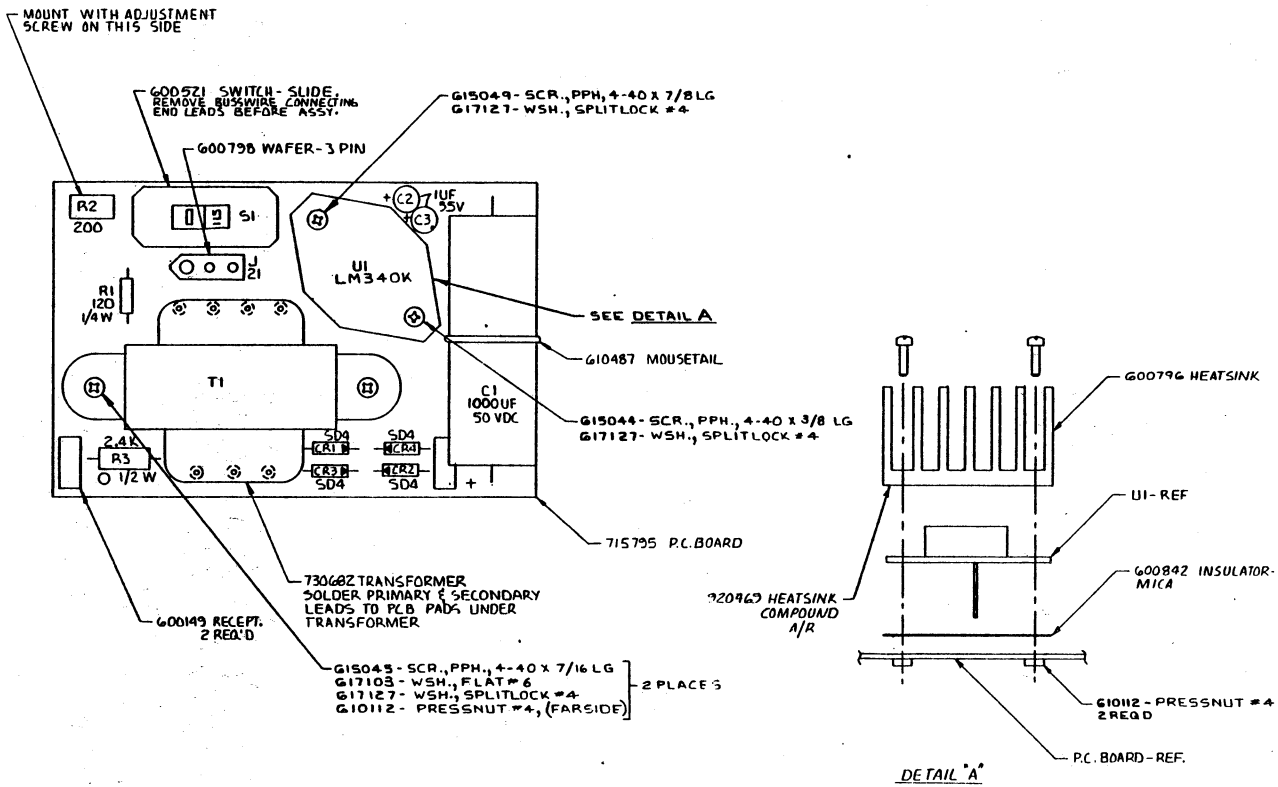
COAX CABLE ——— 6.5 ±.25
RED/WHITE WIRE – 7.0 ±.25

1. ASSEMBLY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSY-OSCILLATOR, OPT.22

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406818	C
SCALE NONE		SHEET 1 OF 2	



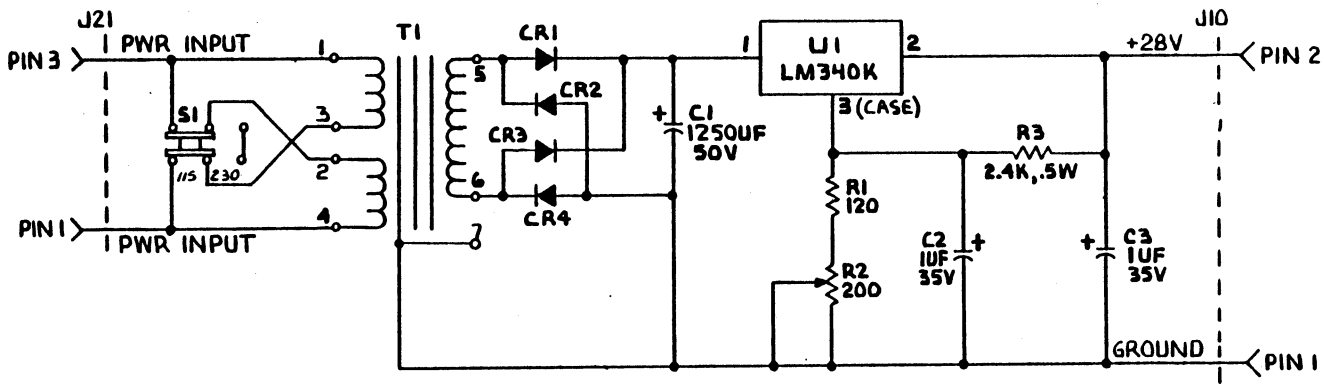
1. SCHEMATIC REFERENCE 721795.

NOTES: UNLESS OTHERWISE SPECIFIED

P.C.B. ASSY-HIGH STABILITY OSCILLATOR POWER SUPPLY

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406795	H

SCALE 2:1 SHEET 1 OF 3



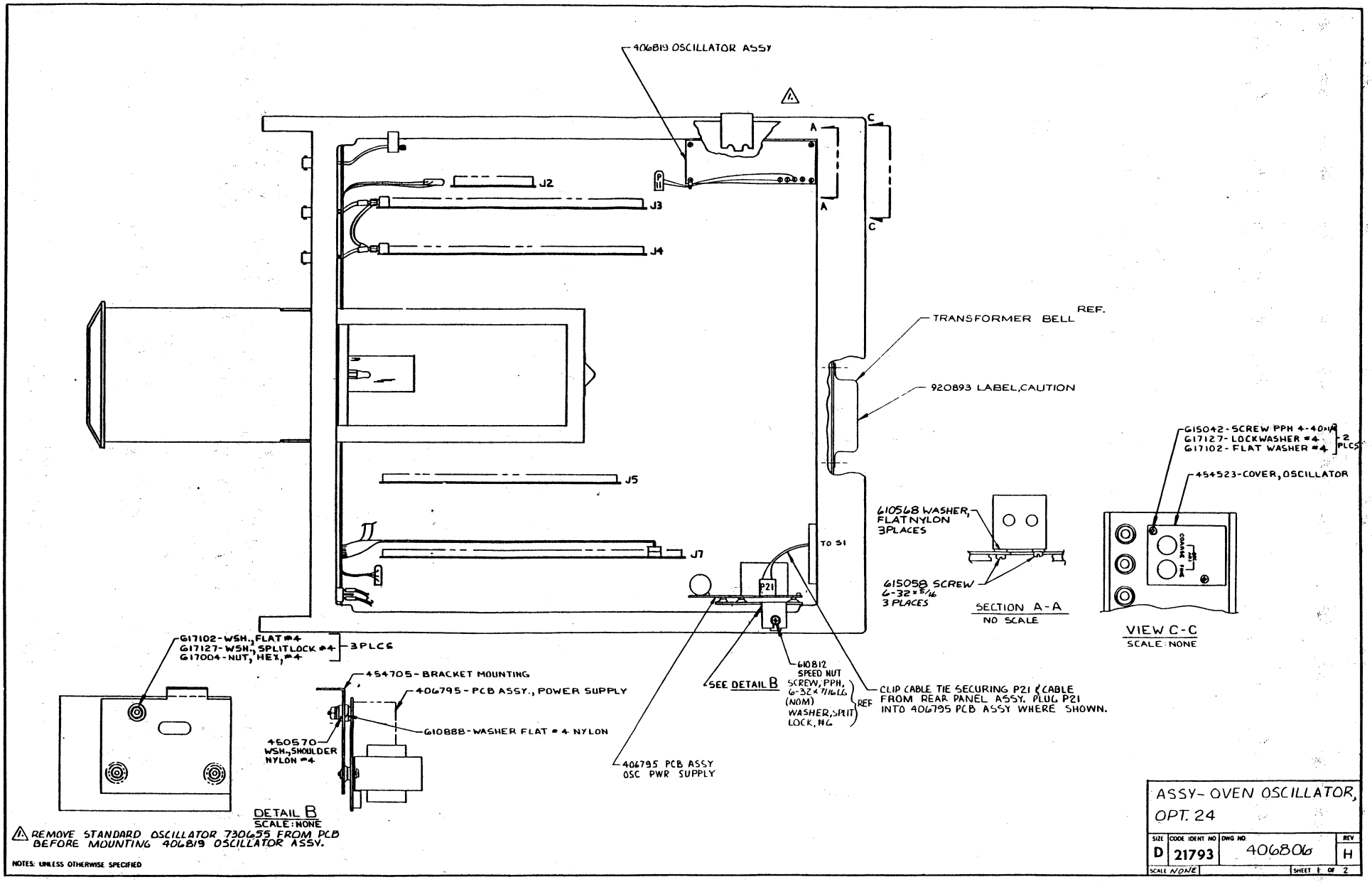
1. DIODES ARE SD4.

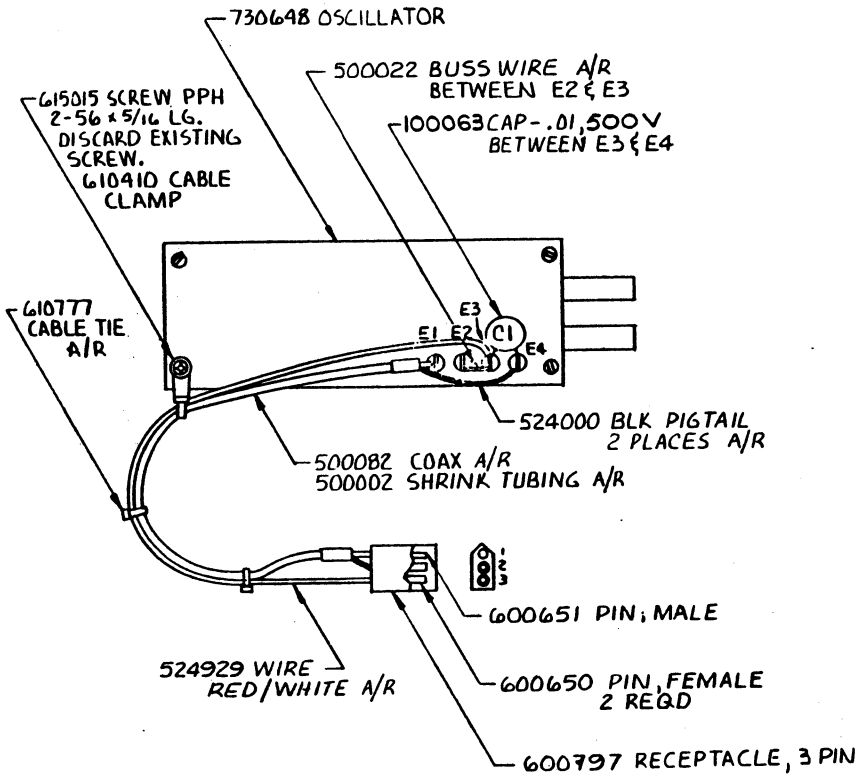
NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC - HIGH STAB. OSCILLATOR PWR. SUPPLY

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	721795	B

SCALE | SHEET 1 OF 1


406819 OSCILLATOR ASSY
J2
J3
J4
J5
J7
P21
TO S1
TRANSFORMER BELL REF.
920893 LABEL,CAUTION
610568 WASHER, FLAT NYLON 3PLACES
615058 SCREW 6-32 x 5/16 3 PLACES
SECTION A-A
NO SCALE
615042 - SCREW PPH 4-40 x 1/2 - 2 PLCS
617127 - LOCKWASHER #4
617102 - FLAT WASHER #4
454523 - COVER, OSCILLATOR
VIEW C-C
SCALE: NONE
617102 - WSH., FLAT #4
617127 - WSH., SPLITLOCK #4
617004 - NUT, HEX, #4 - 3PLCS
454705 - BRACKET MOUNTING
406795 - PCB ASSY., POWER SUPPLY
610888 - WASHER FLAT #4 NYLON
450570 WSH., SHOULDER NYLON #4
DETAIL B
SCALE: NONE
SEE DETAIL B
610812 SPEED NUT SCREW, PPH, 6-32 x 7/16 LG (NOM) WASHER, SPLIT LOCK, #6 - REF
CLIP CABLE TIE SECURING P21 & CABLE FROM REAR PANEL ASSY. PLUG P21 INTO 406795 PCB ASSY WHERE SHOWN.
406795 PCB ASSY OSC PWR SUPPLY
REMOVE STANDARD OSCILLATOR 730655 FROM PCB BEFORE MOUNTING 406819 OSCILLATOR ASSY.
NOTES: UNLESS OTHERWISE SPECIFIED
ASSY- OVEN OSCILLATOR, OPT. 24
SIZE D
CODE IDENT NO 21793
DWG NO 406806
REV H
SCALE NONE
SHEET 1 OF 2



WIRE LENGTHS

COAX CABLE ——— 6.5 ±.25
RED/WHITE WIRE – 7.0 ±.25

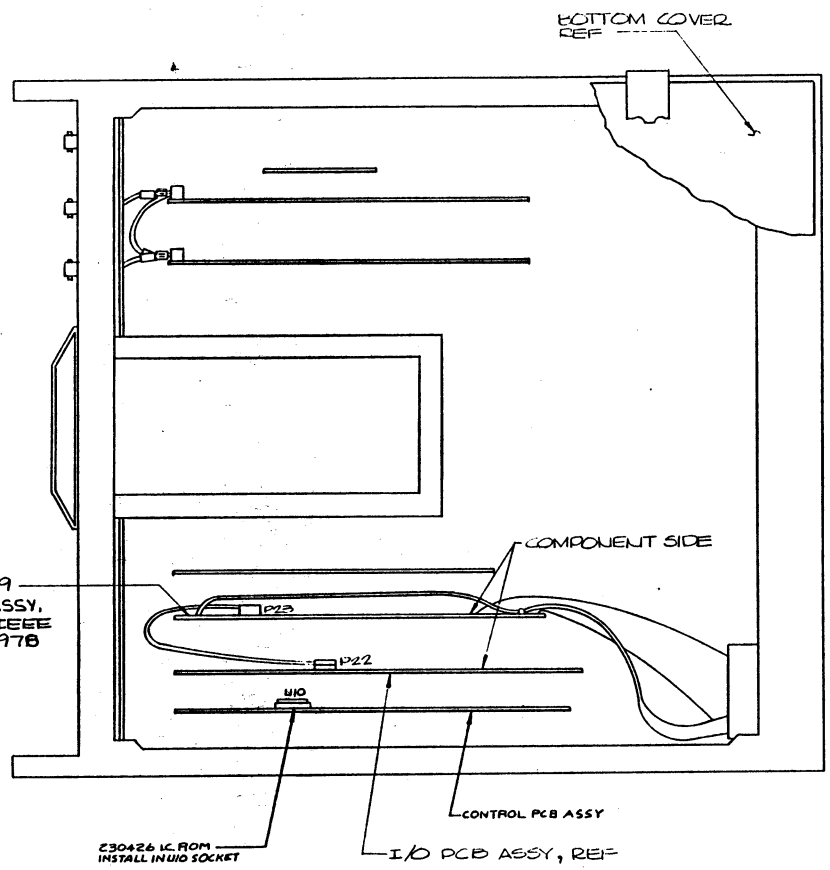
1. ASSEMBLY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

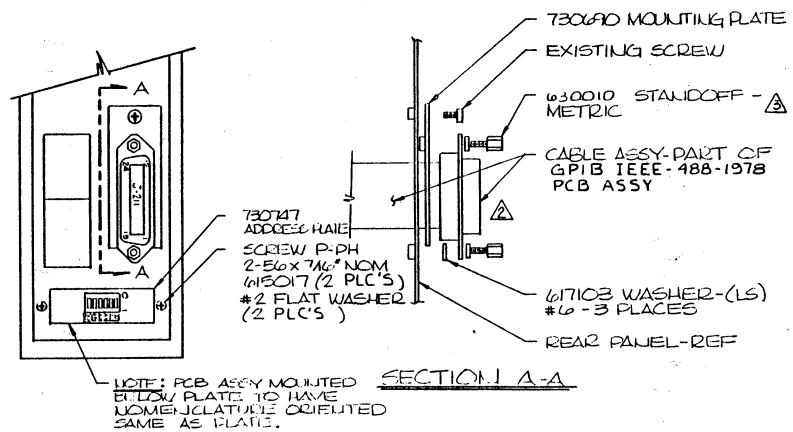
NOTES: UNLESS OTHERWISE SPECIFIED

ASSY-OSCILLATOR, OPT. 24

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406819	C

SCALE NONE | SHEET 1 OF 2





⚠2 DISCARD NUTS AND LOCK WASHERS.

⚠1 REMOVE DUTCH PLATES BEFORE MTG. CONNECTOR & P.C. BOARD.

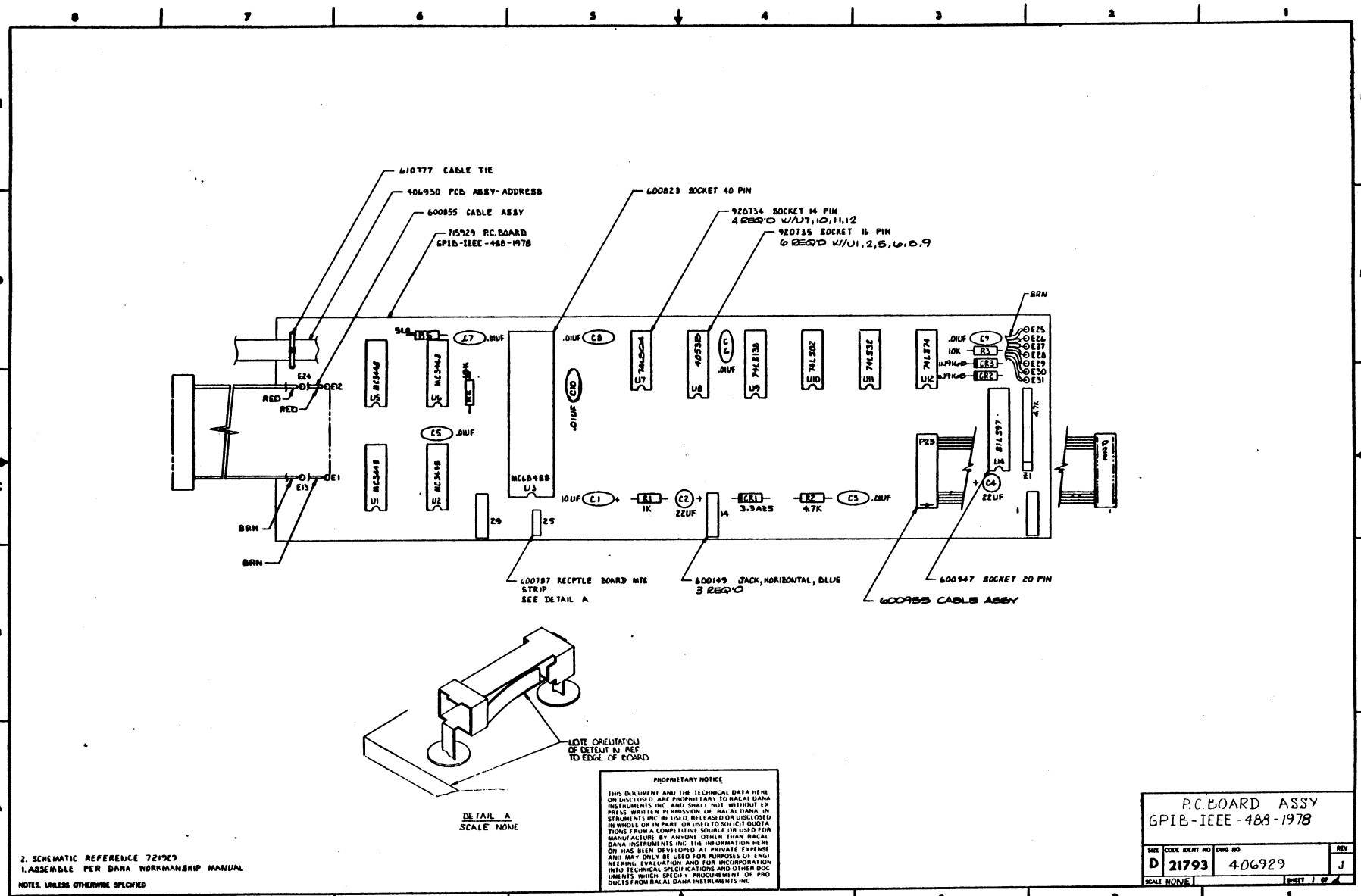
1. ALL PROCESS AND PROCEDURES TO DANA WORKMANSHIP STANDARD.

NOTES: UNLESS OTHERWISE SPECIFIED

OPTION 55A ASSY, GPIB IEEE-488-1978

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	406938	E

SCALE NONE SHEET 1 OF



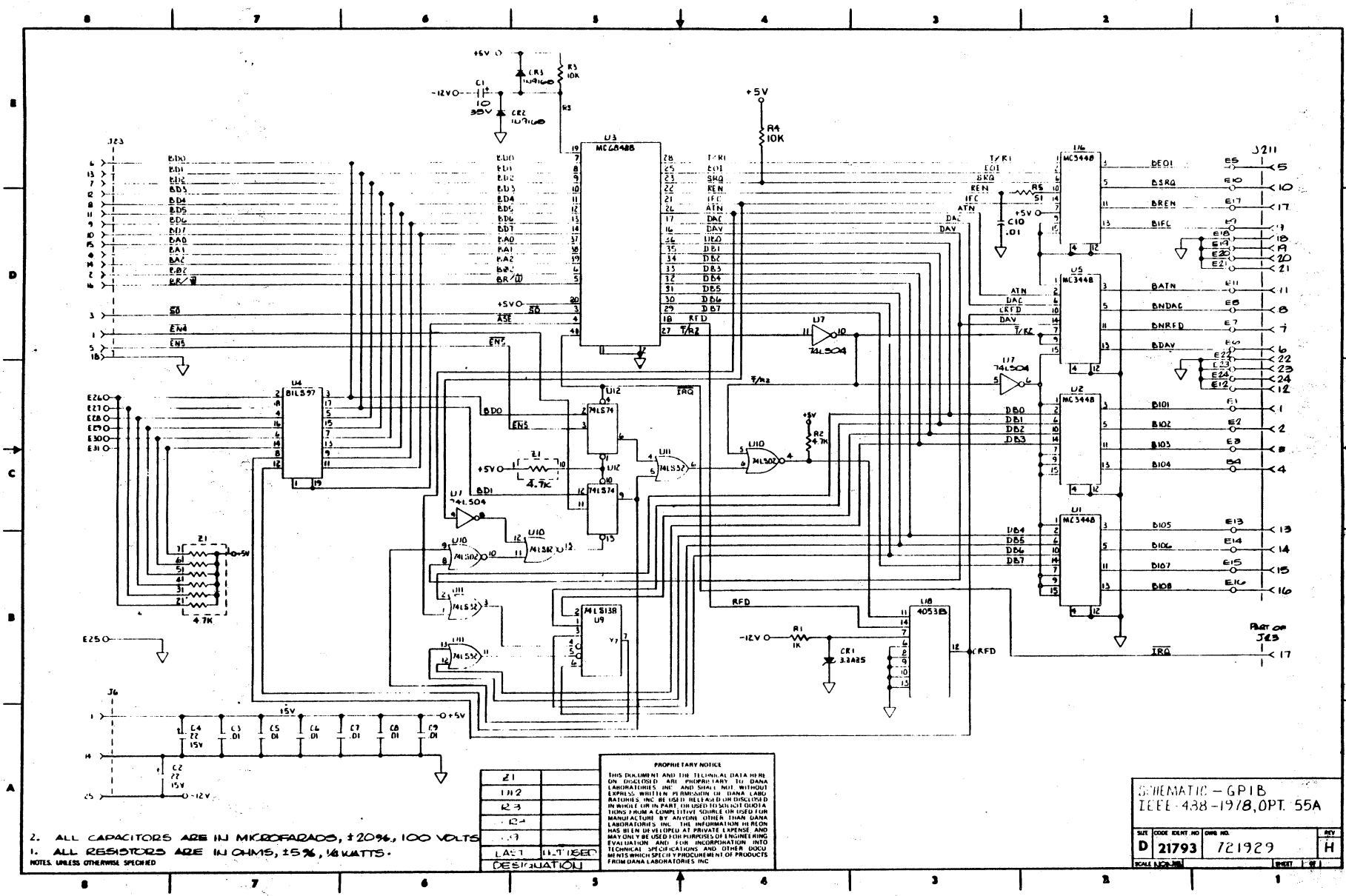
2. SCHEMATIC REFERENCE 721929
1. ASSEMBLE PER DANA WORKMANSHIP MANUAL

NOTES: UNLESS OTHERWISE SPECIFIED

P.C.BOARD ASSY
GPIB-IEEE-488-1978

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	406929	J

SCALE NONE SHEET 1 OF 1


+5V
-12V
R4 10K
R5 51
C10 .01
U3 MC6488
U4 BIL597
U5 MC3448
U6 MC3448
U7 74LS04
U8 4053B
U9 74LS138
U10 74LS02
U11 74LS32
U12 74LS74
R1 1K
R2 4.7K
Z1 4.7K
CR1 3.3ABS
J23
J211
J4
J65
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
DEOI
DSRQ
DREN
DIFC
DATN
DNDAC
DNRFD
DDAV
IRQ
RFD
SCHEMATIC – GPIB
IEEE-488-1978, OPT. 55A
SIZE D
CODE IDENT NO 21793
DWG NO 721929
REV H
SCALE NONE
SHEET 1 OF 1
PROPRIETARY NOTICE
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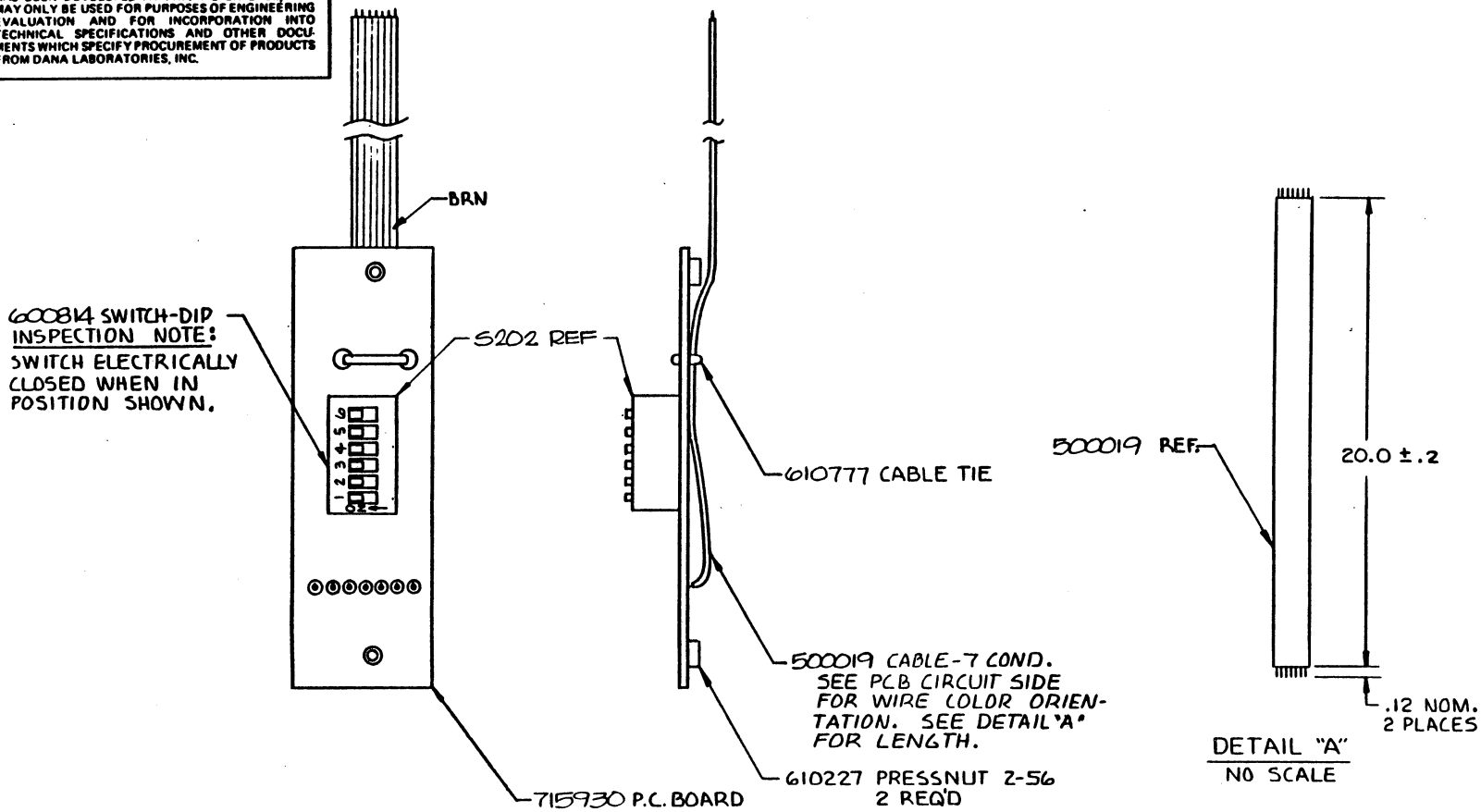
LAST UTILISED DESIGNATION
Z1
U12
R3
R4
C9
2. ALL CAPACITORS ARE IN MICROFARADS, ±20%, 100 VOLTS
1. ALL RESISTORS ARE IN OHMS, ±5%, ¼ WATTS.
NOTES UNLESS OTHERWISE SPECIFIED



2. SCHEMATIC REFERENCE 721930.

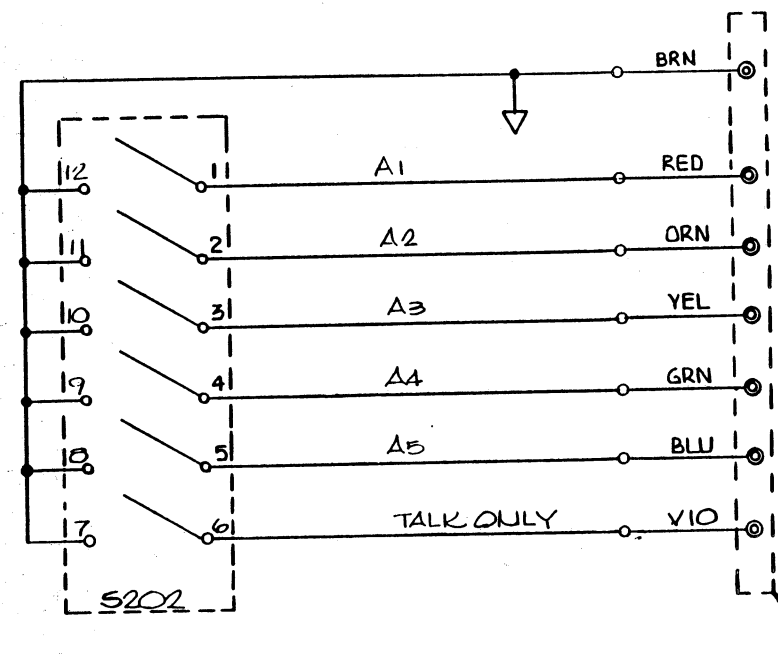
1. ASSY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

PCB ASSY, ADDRESS

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	406930	A

SCALE 2:1 SHEET 1 OF 2

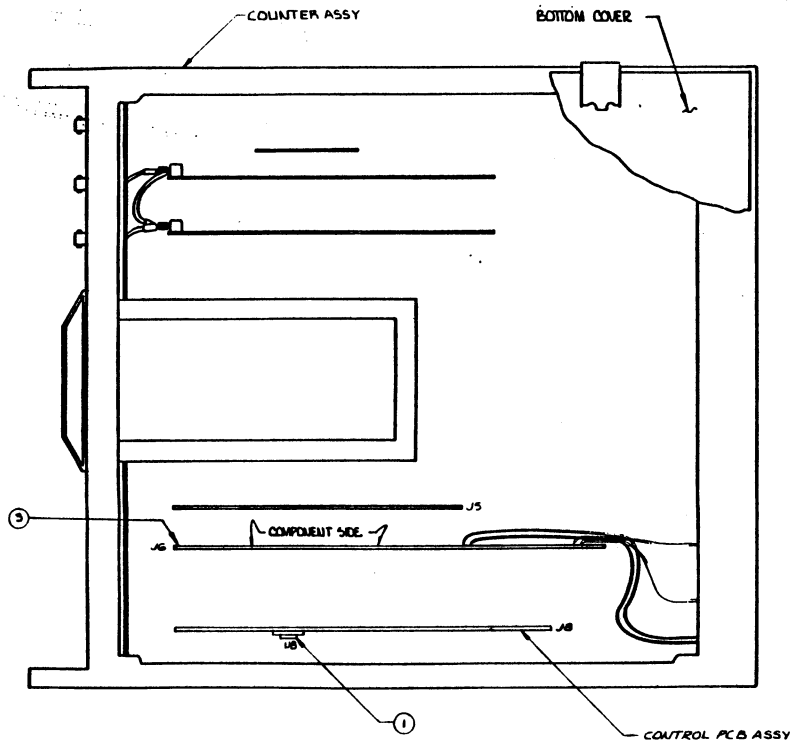


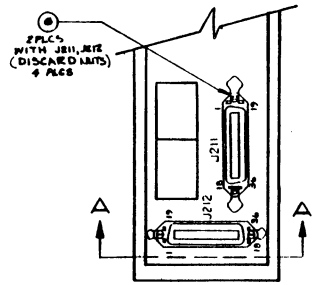
SCHEMATIC-ADDRESS

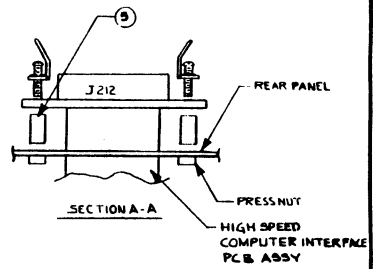
SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	721930	A

SCALE NONE | SHEET | OF

NOTES: UNLESS OTHERWISE SPECIFIED



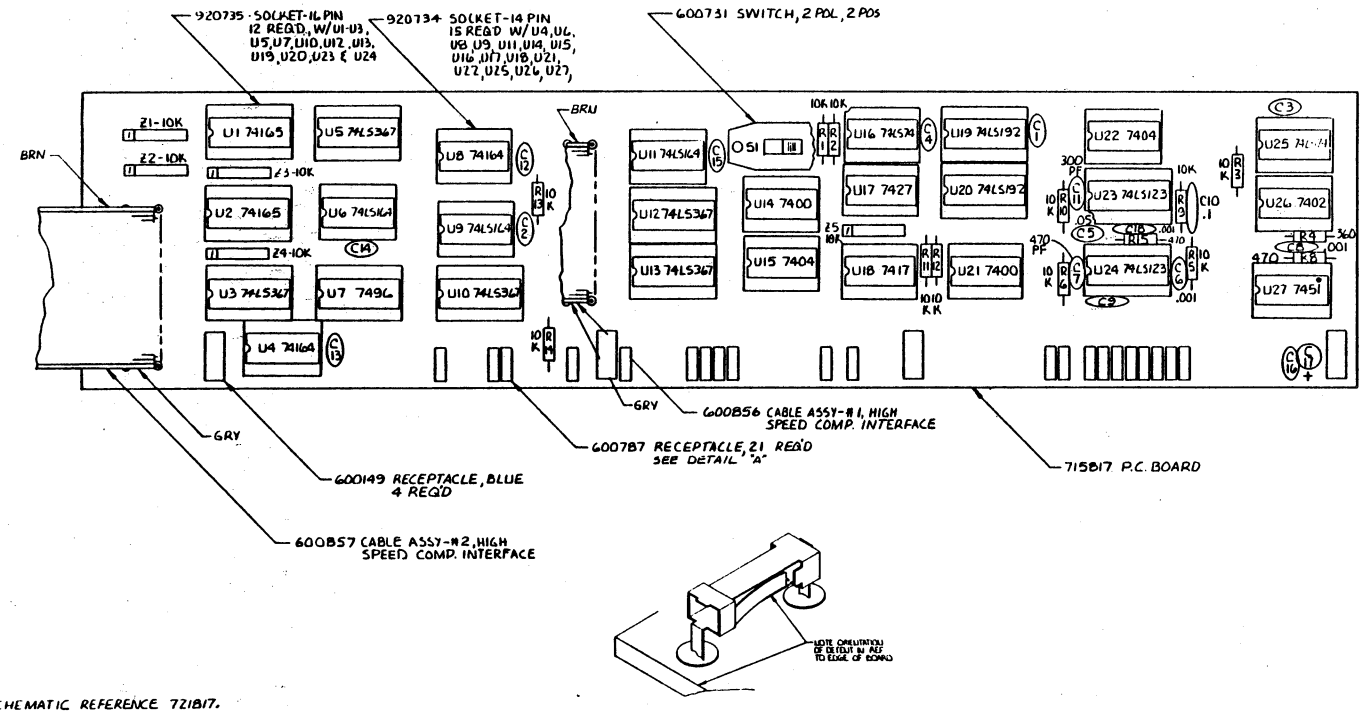




3 TYPE OPTION "56" ON SERIAL NO TAG USED ON BASIC ASSY UNIT
2 BAG & ATTACH (2) MATING CONNECTORS (ITEM 4)
1 ASSEMBLY PROCESSES & PROCEDURES TO CONFORM TO RACAL-DANA WORKMANSHIP STANDARDS

NOTES: UNLESS OTHERWISE SPECIFIED

COMPUTER INTERFACE ASSY, HIGH SPEED - OPTION "56"			
SIZE D	CODE IDENT NO 21793	DWG NO 406942	REV A
SCALE NONE		SHEET 1 OF 2	

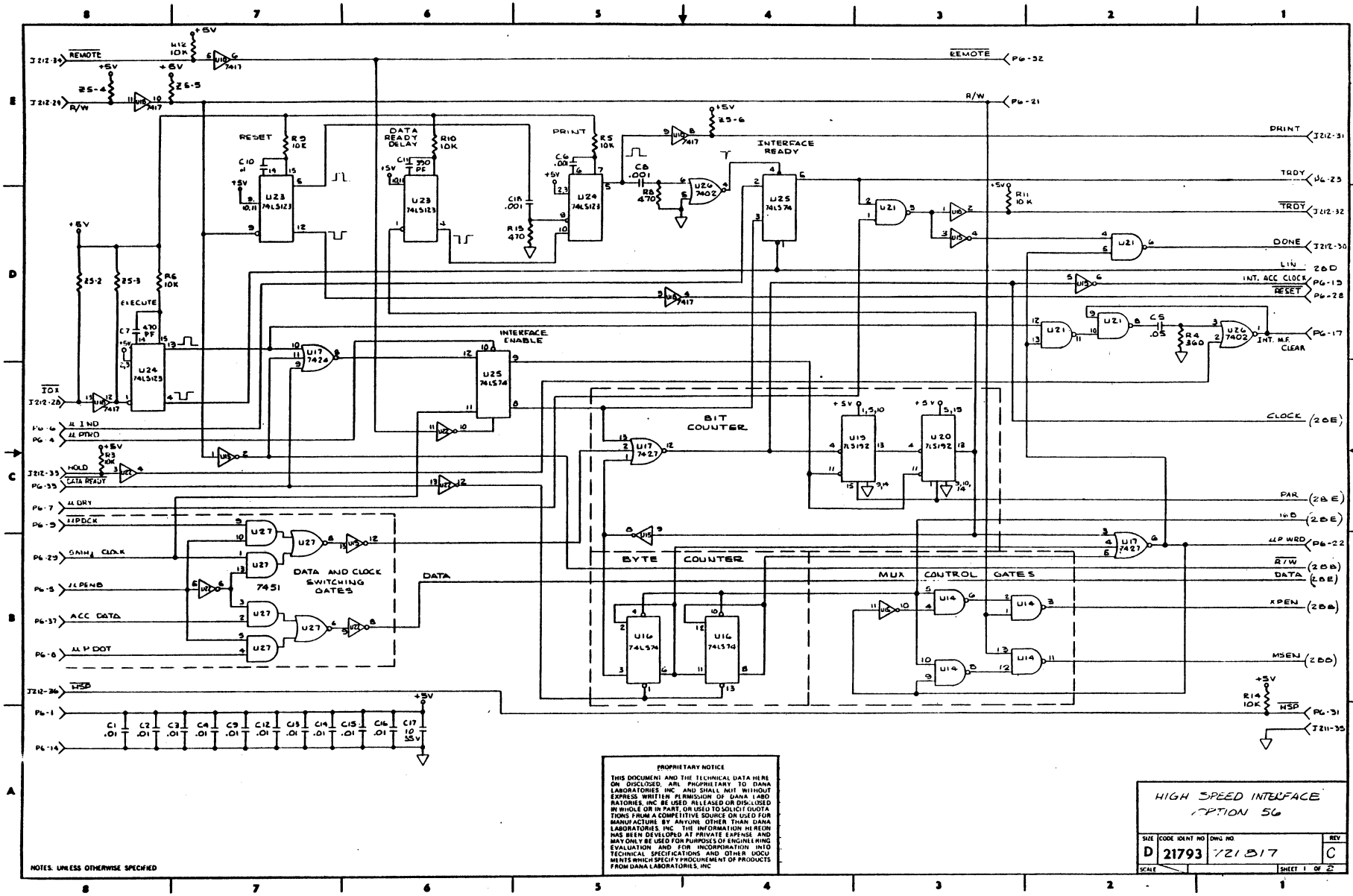


4. SCHEMATIC REFERENCE 721817.
3. CAPACITORS ARE .01.
2. RESISTORS ARE 1/4W 5%.
1. CAPICTANCE IS IN μF.
NOTES: UNLESS OTHERWISE SPECIFIED

PCB ASSY-HIGH SPEED COMPUTER INTERFACE OPT. 56

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	406817	K

SCALE 2/1 SHEET 1 OF 4


REMOTE
R/W
RESET
DATA READY DELAY
PRINT
INTERFACE READY
EXECUTE
INTERFACE ENABLE
BIT COUNTER
BYTE COUNTER
MUX CONTROL GATES
DATA AND CLOCK SWITCHING GATES
7451
DATA
ACC DATA
HOLD
DATA READY
HSD
INT. ACC CLOCK
INT. M.F. CLEAR
CLOCK
PAR
INHB
XPEN
MSEN
TRDY
DONE
LIN
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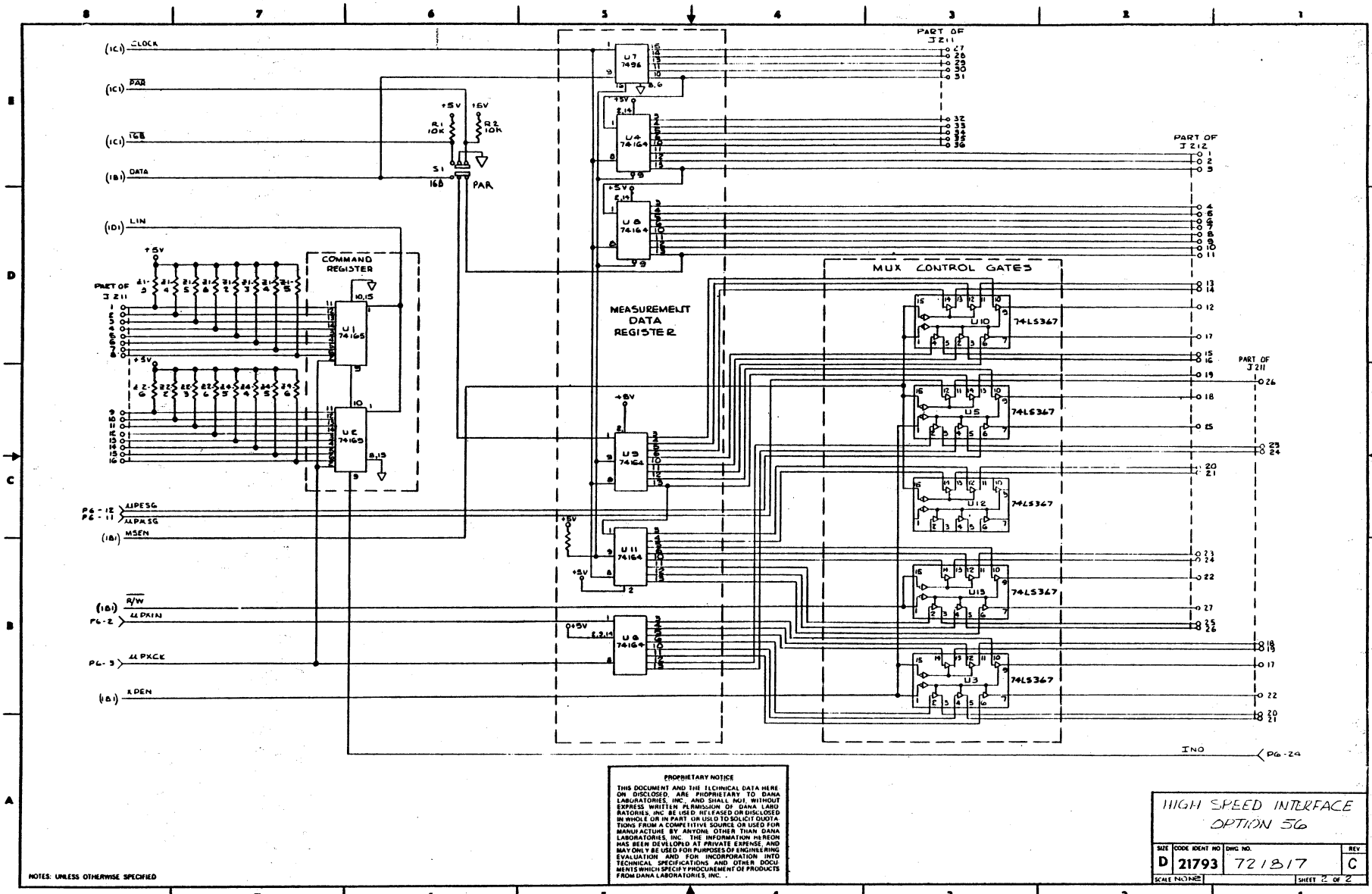
NOTES. UNLESS OTHERWISE SPECIFIED
HIGH SPEED INTERFACE
OPTION 56
SIZE D
CODE IDENT NO 21793
DWG NO 121817
REV C
SCALE
SHEET 1 OF 2



NOTES: UNLESS OTHERWISE SPECIFIED

HIGH SPEED INTERFACE
OPTION 56

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	72/817	C

SCALE NONE | SHEET 2 OF 2

SECTION 7 PARTS LIST

7.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

	Page
Main Logic (406931)	7-3
I/O (406926)	7-10
Control (406925)	7-11
Signal Conditioner "A" (406765)	7-12
Signal Conditioner "B" (406766)	7-15
DAC (406767)	7-18
Reference (406768)	7-20
Display (406764)	7-23
Keyboard (406831)	7-28
Keyboard (406832)	7-29
Prescaler (406793)	7-30
Rear Panel (406772)	7-34
Front Panel (406771)	7-34
Option 06P, Prog. Sync. Window & Sel. Gate Control (406875)	7-35
Option 07, Programmable 50Ω Signal Conditioner "A" (406894)	7-36
Signal Conditioner "B" (406895)	7-37
Option 22, Oven Oscillator Power Supply (406795)	7-38
Oscillator (406818)	7-38
Option 24, Oven Oscillator Power Supply (406795)	7-38
Oscillator (406819)	7-38
Option 55, GPIB Interface Assy(406938)	7-39
GPIB Interface PCB (406929)	7-39
Address (406930)	7-40
Option 56, High Speed Interface Assembly (406942)	7-41
High Speed Interface (406817)	7-42
Option 71, 22V Operation	7-44

NOTE

Several Manufacturer Part Numbers have changed. Consult the Errata Sheet in the front of this book.

7.2 Manufacturers are identified by FSC numbers listed in table 7.2, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-1, and their supplements.

7.3 Certain parts having 21793 (Racal-Dana) listed in the "FSC" column are specially-selected semiconductors. For some of these, standard commercial parts will serve as satisfactory replacements. These Racal-Dana parts are identified in table 7.1 along with the commercial equivalent.

Table 7.1

Semiconductor Type:		Equivalent:
007	Diode	Fairchild FD300
009	Transistor	Motorola 2N2905
014	Transistor	Motorola 2N3501

Table 7.2 - List of Suppliers

FSC	NAME
00779	AMP, INC. HARRISBURG, PENNSYLVANIA
01121	ALLEN BRADLEY CO. MILWAUKEE, WISCONSIN
01295	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS
02660	AMPHENOL CORP. BROADVIEW, ILLINOIS
04222	AEROVOX CORP. (Hi-Q DIVISION) MYRTLE BEACH, SO. CAROLINA
04713	MOTOROLA, INC. (Semiconductor Products Division) PHOENIX, ARIZONA
05397	UNION CARBIDE CORP. (Materials Systems Division) CLEVELAND, OHIO
07263	FAIRCHILD (Semiconductor Division) MOUNTAIN VIEW, CALIFORNIA
07716	TRW ELECTRONIC COMPONENTS (IRC) BURLINGTON, IOWA
11236	CTS OF BERNE, INC. BERNE, INDIANA

Table 7.2 - List of Suppliers continued

FSC	NAME
11237	CTS KEENE, INC. PASO ROBLES, CALIFORNIA
15636	ELEC-TROL, INC. SAUGUS, CALIFORNIA
17856	SILICONIX, INC. SANTA CLARA, CALIFORNIA
21793	RACAL-DANA INSTRUMENTS INC. IRVINE, CALIFORNIA
23936	PAMOTOR BURLINGAME, CALIFORNIA
24226	GOWANDA ELECTRONICS CORP. GOWANDA, NEW YORK
25403	AMPEREX ELECTRONIC CORP. (Semiconductor & Receiving Tube Division) SLATERSVILLE, RHODE ISLAND
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CALIFORNIA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
27556	IMB ELECTRONIC PRODUCTS, INC. SANTA FE SPRINGS, CALIFORNIA
29090	MECHANICAL ENTERPRISES, INC. ALEXANDRIA, VIRGINIA
32767	GRIFFITH PLASTIC PRODUCTS CO. BURLINGAME, CALIFORNIA
34553	AMPEREX/MEPCO-ELECTRA (Component Division) HAUPPAUGE, NEW YORK
34649	INTEL SANTA CLARA, CALIFORNIA
50088	MOSTEK CORP. CARROLLTOWN, TEXAS
50434	HEWLETT-PACKARD CO. (HPA Division) PALO ALTO, CALIFORNIA
52648	PLESSEY MEMORIES SANTA ANA, CALIFORNIA
52840	WESTERN DIGITAL COSTA MESA, CALIFORNIA
53387	3M COMPANY (Electrical Products Division) ST. PAUL, MINNESOTA
56289	SPRAGUE ELECTRIC CO. (Pacific Division) LOS ANGELES, CALIFORNIA
71400	BUSSMAN MFG. (Division of McGraw & Edison Co.) ST. LOUIS, MISSOURI
71471	AEROVOX CORP. (Cinema Plant) MONCKS CORNER, SOUTH CAROLINA
71590	CENTRALAB ELECTRONICS MILWAUKEE, WISCONSIN
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PENNSYLVANIA
73138	BECKMAN INSTRUMENTS, INC. (Helipot Division) FULLERTON, CALIFORNIA
74970	E. F. JOHNSON CO. WASECA, MINNESOTA
75915	LITTELFUSE, INC. DES PLAINES, ILLINOIS
76493	J. W. MILLER CO. COMPTON, CALIFORNIA
79727	C-W INDUSTRIES WARMINSTER, PENNSYLVANIA
80031	MEPCO-ELECTRA MORRISTOWN, NEW JERSEY
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D.C.
81349	MILITARY SPECIFICATION
82389	SWITCHCRAFT, INC. CHICAGO, ILLINOIS
86884	RCA (Electronics Components Division) HARRISON, NEW JERSEY
87730	UNITED MINERAL & CHEMICAL CORP. NEW YORK CITY, NEW YORK
91637	DALE ELECTRONICS, INC. COLUMBUS, NEBRASKA
95238	CONTINENTAL CONNECTOR WOODSIDE, NEW YORK
98291	SEALECTRO CORP. MAMARONECK, NEW YORK
99800	AMERICAN PRECISION INDUSTRIES, INC. (Delevan Division) EAST AURORA, NEW YORK
—	POWER MONOLITHICS INC. CORPUS CHRISTI, TEXAS

406931 – Assy., PCB, MAIN LOGIC.

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C2	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368A105M035AS
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C5.	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C6	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C8	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C9	100117	CAP	CERAM	470 PFD	1000 V	20%	56289	C023B102E471M
C10	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C11	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C12	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C13	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C14	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C15	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C16	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C17	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C18	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C19	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C20	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C21	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C22	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C23	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C24	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C25	110174	CAP	ELECT	10,000 MFD	15 V			3050HS103U015244G
C26	110174	CAP	ELECT	10,000 MFD	15 V			3050HS103U015244G
C27	110157	CAP	ELECT	470 MFD	25 V		34553	ET471X025A01
C28	110067	CAP	ELECT	2000 MFD	35 V		87730	2000DXW35
C29	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C30	100024	CAP	CERAM	.1 MFD	25 V	20%	72982	5815-000Y5U104Z
C31	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368A105M035AS
C32	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C33	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C34	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C35	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C36	100024	CAP	CERAM	1 MFD	25 V	20%	72982	5815-000Y5U104Z
C37	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C38	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368A105M035AS
C39	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C40	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS

406931 – Assy., PCB, MAIN LOGIC *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C41	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C42	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C43	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C44	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C45	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C46	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C47	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C48	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C49	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C50	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C51	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C52	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C53	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C54	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C55	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C56	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C57	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C58	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C59	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C60	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C61	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C62	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C63	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C64	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C65	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C66	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C67	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C68	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C69	100117	CAP	CERAM	470 PFD	1000 V	20%	56289	C023B102E471M
C70	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C71	100117	CAP	CERAM	470 PFD	1000 V	20%	56289	C023B102E471M
CR1	211083	DIODE	SILICO				81349	1N916B
CR2	210070	DIODE	POWER	3 AMP			04713	MR501
CR3	210070	DIODE	POWER	3 AMP			04713	MR501
CR4	210070	DIODE	POWER	3 AMP			04713	MR501
CR5	210070	DIODE	POWER	3 AMP			04713	MR501
CR6	210004	DIODE	SILICO				81349	1N4004
CR7	210004	DIODE	SILICO				81349	1N4004
CR8	210004	DIODE	SILICO				81349	1N4004
CR9	210004	DIODE	SILICO				81349	1N4004
CR10	210004	DIODE	SILICO				81349	1N4004
CR11	210004	DIODE	SILICO				81349	1N4004
CR12	210004	DIODE	SILICO				81349	1N4004
CR13	210004	DIODE	SILICO				81349	1N4004

406931 – Assy., PCB, MAIN LOGIC *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION			FSC	MANU P/N
CR14	210004	DIODE	SILICO		81349	1N4004
CR15	210004	DIODE	SILICO		81349	1N4004
CR17	211083	DIODE	SILICO		81349	1N916B
CR18	211083	DIODE	SILICO		81349	1N916B
CR19	211083	DIODE	SILICO		81349	1N916B
CR20	211083	DIODE	SILICO		81349	1N916B
J11	600798	CONN	PLUG	3 P	27264	09-18-5031
J12	600798	CONN	PLUG	3 P	27264	09-18-5031
J15	600798	CONN	PLUG	3 P	27264	09-18-5031
Q1	200088	TRANS	SILICO	PNP	80131	2N4248
Q2	200037	TRANS	SILICO	NPN	80131	2N3646
Q3	200088	TRANS	SILICO	PNP	80131	2N4248
Q4	200088	TRANS	SILICO	PNP	80131	2N4248
Q5	200088	TRANS	SILICO	PNP	80131	2N4248
Q6	200088	TRANS	SILICO	PNP	80131	2N4248
Q7	200099	TRANS		PNP	81349	2N4258
Q8	200099	TRANS		PNP	81349	2N4258
Q9	200088	TRANS	SILICO	PNP	80131	2N4248
Q10	200088	TRANS	SILICO	PNP	80131	2N4248
Q11	200088	TRANS	SILICO	PNP	80131	2N4248
Q12	200099	TRANS		PNP	81349	2N4258
Q13	200099	TRANS		PNP	81349	2N4258
Q14	200088	TRANS	SILICO	PNP	80131	2N4248
Q15	200088	TRANS	SILICO	PNP	80131	2N4248
Q16	200088	TRANS	SILICO	PNP	80131	2N4248
Q17	200088	TRANS	SILICO	PNP	80131	2N4248
Q18	200037	TRANS	SILICO	NPN	80131	2N3646
Q19	200037	TRANS	SILICO	NPN	80131	2N3646
Q20	200037	TRANS	SILICO	NPN	80131	2N3646
Q21	200037	TRANS	SILICO	NPN	80131	2N3646
Q22	200037	TRANS	SILICO	NPN	80131	2N3646

406931 – Assy., PCB, MAIN LOGIC *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION				FSC	MANU P/N
R1	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R2	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R3	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R4	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R5	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R6	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R7	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R8	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R9	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R10	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R11	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R12	000471	RES	CARBON	470 OHM	5% 1/4W	81349	RC07GF471J
R13	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R14	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R15	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R16	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R17	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R18	000132	RES	CARBON	1.3 K	5% 1/4W	81349	RC07GF132J
R19	000242	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R20	000132	RES	CARBON	1.3 K	5% 1/4W	81349	RC07GF132J
R21	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R22	000132	RES	CARBON	1.3 K	5% 1/4W	81349	RC07GF132J
R23	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R24	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R25	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R26	000221	RES	CARBON	220 OHM	5% 1/4W	81349	RC07GF221J
R27	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R28	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R29	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R30	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R31	000391	RES	CARBON	390 OHM	5% 1/4W	81349	RC07GF391J
R32	000181	RES	CARBON	180 OHM	5% 1/4W	81349	RC07GF181J
R33	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R34	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R35	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R36	000391	RES	CARBON	390 OHM	5% 1/4W	81349	RC07GF391J
R37	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R38	000391	RES	CARBON	390 OHM	5% 1/4W	81349	RC07GF391J
R39	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J

406931 – Assy., PCB, MAIN LOGIC *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R40	000391	RES CARBON 390 OHM 5% 1/4W	81349	RC07GF391J
R41	000391	RES CARBON 390 OHM 5% 1/4W	81349	RC07GF391J
R42	000181	RES CARBON 180 OHM 5% 1/4W	81349	RC07GF181J
R43	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R44	000391	RES CARBON 390 OHM 5% 1/4W	81349	RC07GF391J
R45	000181	RES CARBON 180 OHM 5% 1/4W	81349	RC07GF181J
R46	000471	RES CARBON 470 OHM 5% 1/4W	81349	RC07GF471J
R47	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R48	000910	RES CARBON 91 OHM 5% 1/4W	81349	RC07GF910J
R49	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R50	000471	RES CARBON 470 OHM 5% 1/4W	81349	RC07GF471J
R51	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R52	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R53	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R54	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R55	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R56	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R58	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R59	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R60	001731	RES CARBON 6.8 OHM FSV 5% 1/4W	21793	001731
R61	040244	POT CERMET 20 OHM 20% 1/2W	73138	72PX20
R63	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R64	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R65	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R66	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R67	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R68	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R70	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R71	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R72	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R73	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R74	020713	RES WW .10 OHM 5% 2W	07716	BWH Series
R75	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R76	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R77	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R78	000391	RES CARBON 390 OHM 5% 1/4W	81349	RC07GF391J
R79	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R80	000510	RES CARBON 51 OHM 5% 1/4W	81349	RC07GF510J
R81	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R82	000471	RES CARBON 470 OHM 5% 1/4W	81349	RC07GF471J
R83	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R84	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R85	000471	RES CARBON 470 OHM 5% 1/4W	81349	RC07GF471J
R86	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R87	000471	RES CARBON 470 OHM 5% 1/4W	81349	RC07GF471J
R88	000471	RES CARBON 470 OHM 5% 1/4W	81349	RC07GF471J
R89	000431	RES CARBON 430 OHM 5% 1/4W	81349	RC07GF431J
R90	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
U1	230118	INTEGRATED CIRCUIT NPN	86884	CA3086
U2	230205	INTEGRATED CIRCUIT	04713	MC10102P
U3	230112	INTEGRATED CIRCUIT	04713	MC10131
U4	230112	INTEGRATED CIRCUIT	04713	MC10131
U5	230205	INTEGRATED CIRCUIT	04713	MC10102P
U6	230205	INTEGRATED CIRCUIT	04713	MC10102P
U7	230112	INTEGRATED CIRCUIT	04713	MC10131
U8	230112	INTEGRATED CIRCUIT	04713	MC10131
U9	230193	INTEGRATED CIRCUIT CERAM	01295	74LS00
U10	230194	INTEGRATED CIRCUIT CERAM	01295	74LS74
U11	230064	INTEGRATED CIRCUIT CERAM	01295	7404
U12	230205	INTEGRATED CIRCUIT	04713	MC10102P
U13	230205	INTEGRATED CIRCUIT	04713	MC10102P
U14	230205	INTEGRATED CIRCUIT	04713	MC10102P
U15	230206	INTEGRATED CIRCUIT	04713	10109P
U16	230206	INTEGRATED CIRCUIT	04713	10109P
U17	230205	INTEGRATED CIRCUIT	04713	MC10102P
U18	230030	INTEGRATED CIRCUIT CERAM	01295	7402
U19	230193	INTEGRATED CIRCUIT CERAM	01295	74LS00
U20	230317	INTEGRATED CIRCUIT PLASTIC	07263	74LS90
U21	230112	INTEGRATED CIRCUIT	04713	MC10131
U22	230112	INTEGRATED CIRCUIT	04713	MC10131
U23	230112	INTEGRATED CIRCUIT	04713	MC10131
U24	230112	INTEGRATED CIRCUIT	04713	MC10131
U25	230112	INTEGRATED CIRCUIT	04713	MC10131
U26	230234	INTEGRATED CIRCUIT CERAM	01295	74LS04
U27	230028	INTEGRATED CIRCUIT CERAM	01295	7400
U28	230311	INTEGRATED CIRCUIT	50088	MK5009P
U29	230250	INTEGRATED CIRCUIT	01295	SN7412N
U30	230193	INTEGRATED CIRCUIT CERAM	01295	74LS00
U31	230237	INTEGRATED CIRCUIT	01295	SN74LS123N
U32	230510	INTEGRATED CIRCUIT SHIFT REGISTER	27014	DM74LS164
U33	230212	INTEGRATED CIRCUIT	27014	74164
U34	230510	INTEGRATED CIRCUIT SHIFT REGISTER	27014	DM74LS164
U35	230064	INTEGRATED CIRCUIT CERAM	01295	7404
U36	230072	INTEGRATED CIRCUIT CERAM	01295	7474
U37	230028	INTEGRATED CIRCUIT CERAM	01295	7400

406931 – Assy., PCB, MAIN LOGIC *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
U38	230383	INTEGRATED CIRCUIT	01295	SN74LS490N
U39	230383	INTEGRATED CIRCUIT	01295	SN74LS490N
U40	230383	INTEGRATED CIRCUIT	01295	SN74LS490N
U41	230383	INTEGRATED CIRCUIT	01295	SN74LS490N
U42	230433	INTEGRATED CIRCUIT	01295	74LS165
U43	230064	INTEGRATED CIRCUIT CERAM	01295	7404
U44	230099	INTEGRATED CIRCUIT CERAM	01295	7454
U45	230193	INTEGRATED CIRCUIT CERAM	01295	74LS00
U46	230433	INTEGRATED CIRCUIT	01295	74LS165
U47	230433	INTEGRATED CIRCUIT	01295	74LS165
U48	230433	INTEGRATED CIRCUIT	01295	74LS165
U49	230433	INTEGRATED CIRCUIT	01295	74LS165
U50	230193	INTEGRATED CIRCUIT CERAM	01295	74LS00
U51	230194	INTEGRATED CIRCUIT CERAM	01295	74LS74
U52	230306	INTEGRATED CIRCUIT	01295	74LS02
U53	230144	INTEGRATED CIRCUIT	27014	LM309KC
U54	230203	INTEGRATED CIRCUIT	04713	MC7812CK
U55	230204	INTEGRATED CIRCUIT	27014	LM320K-12
U56	230144	INTEGRATED CIRCUIT	27014	LM309KC
U57	230144	INTEGRATED CIRCUIT	27014	LM309KC
U58	230144	INTEGRATED CIRCUIT	27014	LM309KC
W1	600245	JUMPER, INSULATED		L-2007-1LP
W2	600245	JUMPER, INSULATED		L-2007-1LP
W3	600245	JUMPER, INSULATED		L-2007-1LP
Y1	730655	OSCILLATOR - TCXO 10 MHz	21793	730655
Z1	080008	RES CERMET 1 K NETWORK 2%	11237	761-3-R1K
Z2	080002	RES CERMET 500 OHM NETWORK 2%	11237	750-81-R500
Z3	080002	RES CERMET 500 OHM NETWORK 2%	11237	750-81-R500
Z4	080002	RES CERMET 500 OHM NETWORK 2%	11237	750-81-R500
Z5	080002	RES CERMET 500 OHM NETWORK 2%	11237	750-81-R500
Z6	080002	RES CERMET 500 OHM NETWORK 2%	11237	750-81-R500
Z7	080002	RES CERMET 500 OHM NETWORK 2%	11237	750-81-R500
Z8	080002	RES CERMET 500 OHM NETWORK 2%	11237	750-81-R500
Z9	080010	RES CERMET TTL to ECL NETWORK	11237	761-45
Z10	080002	RES CERMET 500 OHM NETWORK 2%	11237	750-81-R500
Z11	080002	RES CERMET 500 OHM NETWORK 2%	11237	750-81-R500
Z12	080010	RES CERMET TTL to ECL NETWORK	11237	761-45
Z13	080010	RES CERMET TTL to ECL NETWORK	11237	761-45

406765 – Assy., SIGNAL CONDITIONER "A"

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	C023B501E103M
C2	100079	CAP	CERAM	3.9±.5 PFD	1000 V		56289	C030B102E3R9D
C3	130146	CAP	TRIMMER	.25-1.5 PFD			74970	273-0001-002
C4	100119	CAP	CERAM	470 PFD	100 V	5%	72982	8121-M100-C0G-471J
C5	100081	CAP	CERAM	4.7 PFD	1000 V	5%	56289	C030B102E4R7D
C6	130146	CAP	TRIMMER	.25-1.5 PFD			74970	273-0001-002
C7	100102	CAP	CERAM	47 PFD	1000 V	5%	56289	C030B102H470J
C8	101174	CAP	CERAM	.001 MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C9	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C10	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C11	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C12	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C16	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C17	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C18	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C19	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C20	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C21	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C22	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C23	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C24	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C25	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C26	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C28	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C29	100051	CAP	CERAM	3 PFD	500 V		71471	TCD-B1-0
CR2	211083	DIODE	SILICO				81349	1N916B
CR3	211083	DIODE	SILICO				81349	1N916B
CR4	211083	DIODE	SILICO				81349	1N916B
CR5	211083	DIODE	SILICO				81349	1N916B
CR6	211083	DIODE	SILICO				81349	1N916B
CR7	211083	DIODE	SILICO				81349	1N916B
CR8	220031	DIODE	SILICO	ZENER	3.3 V		04713	1/4M3.3AZ5
CR9	220031	DIODE	SILICO	ZENER	3.3 V		04713	1/4M3.3AZ5
CR10	211236	DIODE	SILICO		007		21793	211236
CR11	211236	DIODE	SILICO		007		21793	211236
CR12	210064	DIODE	Matched Pair		018 Type		21793	210064
CR13	210064	DIODE	Matched Pair		018 Type		21793	210064
CR14	211083	DIODE	SILICO				81349	1N916B

406765 – Assy., SIGNAL CONDITIONER "A" *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
K1	310125	RELAY REED 1 FORM A 5 V	21793	310125
K2	310127	RELAY REED	15636	RA3032-1051
K3	310127	RELAY REED	15636	RA3032-1051
K4	310127	RELAY REED	15636	RA3032-1051
K5	310127	RELAY REED	15636	RA3032-1051
K6	310127	RELAY REED	15636	RA3032-1051
L1	310068	CHOKE RF 1 μH 10%	99800	1537-12
L2	310068	CHOKE RF 1 μH 10%	99800	1537-12
L3	310126	CHOKE RF .39 μH 10%	24226	10/390μH±10%
L4	310068	CHOKE RF 1 μH 10%	99800	1537-12
L5	310126	CHOKE RF .39 μH 10%	24226	10/390μH±10%
Q1	200241	TRANS FET MATCHED DUAL CHAN	17856	E420
Q2	200219	TRANS Matched Pair 2N3563	21793	200219
Q3	200219	TRANS Matched Pair 2N3563	21793	200219
R1	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R3	010991	RES METAL 990 K .1% 1/4W	81349	RN65C9903B
R4	010988	RES METAL 10.1 K .1% 1/10W	81349	RN55C1012B
R5	010990	RES METAL 900 K .1% 1/4W	81349	RN65C9003B
R6	010989	RES METAL 111 K .1% 1/10W	81349	RN55C1113B
R7	010879	RES METAL 1 M 1% 1/10W	81349	RN55D1004F
R8	000434	RES CARBON 430 K 5% 1/4W	81349	RC07GF434J
R9	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R10	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R11	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R12	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R13	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R14	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R15	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R16	000910	RES CARBON 91 OHM 5% 1/4W	81349	RC07GF910J
R17	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R18	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R19	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R20	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R21	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R22	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R23	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R24	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R25	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R26	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R27	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J

406765 – Assy., SIGNAL CONDITIONER "A" *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R28	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R29	000910	RES CARBON 91 OHM 5% 1/4W	81349	RC07GF910J
R30	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R31	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R32	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R33	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R34	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R35	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R36	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R37	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R38	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R39	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R40	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R41	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R42	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R43	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R44	000203	RES CARBON 20 K 5% 1/4W	81349	RC07GF203J
R45	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R46	000242	RES CARBON 2.4 K 5% 1/4W	81349	RC07GF242J
R47	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R48	040230	POT CERMET 2 K 10%	73138	89PR2K
R49	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R50	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R51	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R52	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R53	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R54	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R55	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R56	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R57	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R58	040228	POT CERMET 500 OHM 10%	73138	89PR500
R59	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
U1	230118	INTEGRATED CIRCUIT	86884	CA3086
U2	230118	INTEGRATED CIRCUIT	86884	CA3086
U3	230202	INTEGRATED CIRCUIT	86884	CA3102E
U4	230028	INTEGRATED CIRCUIT CERAM	01295	7400

406766 – Assy., SIGNAL CONDITIONER "B"

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100063	CAP	CERAM	.01 MFD	500 V	20%	56289	C023B501E103M
C2	100079	CAP	CERAM	3.9±.5 PFD	1000 V		56289	C030B102E3R9D
C3	130146	CAP	TRIMMER	.25-1.5 PFD			74970	273-0001-002
C4	100119	CAP	CERAM	470 PFD	100 V	5%	72982	8121-M100-C0G-471J
C5	100081	CAP	CERAM	4.7 PFD	1000 V	5%	56289	C030B102E4R7D
C6	130146	CAP	TRIMMER	.25-1.5 PFD			74970	273-0001-002
C7	100102	CAP	CERAM	47 PFD	1000 V	5%	56289	C030B102H470J
C8	101174	CAP	CERAM	.001 PFD	500 V	10%	04222	SCD-DI-2X5F-1000
C9	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C10	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C11	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C12	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C16	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C17	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C18	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C19	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C20	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C21	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C22	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C23	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C24	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C25	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C26	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C28	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C29	100051	CAP	CERAM	3 PFD	500 V		71471	TCD-B1-0
CR1	211083	DIODE	SILICO				81349	1N916B
CR2	211083	DIODE	SILICO				81349	1N916B
CR3	211083	DIODE	SILICO				81349	1N916B
CR4	211083	DIODE	SILICO				81349	1N916B
CR5	211083	DIODE	SILICO				81349	1N916B
CR6	211083	DIODE	SILICO				81349	1N916B
CR7	211083	DIODE	SILICO				81349	1N916B
CR8	220031	DIODE	SILICO	ZENER	3.3 V		04713	1/4M3.3AZ5
CR9	220031	DIODE	SILICO	ZENER	3.3 V		04713	1/4M3.3AZ5
CR10	211236	DIODE	SILICO		007		21793	211236
CR11	211236	DIODE	SILICO		007		21793	211236
CR12	210064	DIODE	Matched Pair		018 Type		21793	210064
CR13	210064	DIODE	Matched Pair		018 Type		21793	210064
CR14	211083	DIODE	SILICO				81349	1N916B

406766 – Assy., SIGNAL CONDITIONER "B" *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
K1	310125	RELAY REED 1 FORM A 5 V	21793	310125
K2	310127	RELAY REED	15636	RA3032-1051
K3	310127	RELAY REED	15636	RA3032-1051
K4	310127	RELAY REED	15636	RA3032-1051
K5	310127	RELAY REED	15636	RA3032-1051
K6	310127	RELAY REED	15636	RA3032-1051
K7	310127	RELAY REED	15636	RA3032-1051
L1	310068	CHOKE RF 1 μH 10%	99800	1537-12
L2	310068	CHOKE RF 1 μH 10%	99800	1537-12
L3	310126	CHOKE RF .39 μH 10%	24226	10/390μH±10%
L4	310068	CHOKE RF 1 μH 10%	99800	1537-12
L5	310126	CHOKE RF .39 μH 10%	24226	10/390μH±10%
Q1	200241	TRANS FET MATCHED DUAL CHAN	17856	E420
Q2	200219	TRANS Matched Pair 2N3563	21793	200219
Q3	200219	TRANS Matched Pair 2N3563	21793	200219
R2	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R3	010991	RES METAL 990 K .1% 1/4W	81349	RN65C9903B
R4	010988	RES METAL 10.1 K .1% 1/10W	81349	RN55C1012B
R5	010990	RES METAL 900 K .1% 1/4W	81349	RN65C9003B
R6	010989	RES METAL 111 K .1% 1/10W	81349	RN55C1113B
R7	010879	RES METAL 1 M 1% 1/10W	81349	RN55D1004F
R8	000434	RES CARBON 430 K 5% 1/4W	81349	RC07GF434J
R9	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R10	000301	RES CARBON 300 OHM 5% 1/4W	81349	RC07GF301J
R11	000132	RES CARBON 1.3 K 5% 1/4W	81349	RC07GF132J
R12	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R13	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R14	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R15	010705	RES METAL 4.53 K 1% 1/10W	81349	RN55C4531F
R16	000910	RES CARBON 91 OHM 5% 1/4W	81349	RC07GF910J
R17	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R18	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R19	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R20	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R21	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R22	000430	RES CARBON 43 OHM 5% 1/4W	81349	RC07GF430J
R23	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R24	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J
R25	000121	RES CARBON 120 OHM 5% 1/4W	81349	RC07GF121J

406766 – Assy., SIGNAL CONDITIONER "B" *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION				FSC	MANU P/N
R26	000132	RES	CARBON	1.3 K	5% 1/4W	81349	RC07GF132J
R27	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R28	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R29	000910	RES	CARBON	91 OHM	5% 1/4W	81349	RC07GF910J
R30	000430	RES	CARBON	43 OHM	5% 1/4W	81349	RC07GF430J
R31	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R32	010705	RES	METAL	4.53 K	1% 1/10W	81349	RN55C4531F
R33	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R34	010705	RES	METAL	4.53 K	1% 1/10W	81349	RN55C4531F
R35	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R36	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R37	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R38	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R39	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GG302J
R40	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R41	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R42	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R43	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R44	000203	RES	CARBON	20 K	5% 1/4W	81349	RC07GF203J
R45	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R46	000242	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R47	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R48	040230	POT	CERMET	2 K	10%	73138	89PR2K
R49	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R50	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R51	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R52	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R53	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R54	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R55	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R56	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R57	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R58	040228	POT	CERMET	500 OHM	10%	73138	89PR500
R59	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
U1	230118	INTEGRATED CIRCUIT		NPN		86884	CA3086
U2	230118	INTEGRATED CIRCUIT		NPN		86884	CA3086
U3	230202	INTEGRATED CIRCUIT				86884	CA3102E
U4	230028	INTEGRATED CIRCUIT		CERAM		01295	7400

406767 – Assy., PCB, DAC

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N.
C1	100103	CAP	CERAM	68 PFD	1000 V	5%	56289	C030A102K680J
C2	100103	CAP	CERAM	68 PFD	1000 V	5%	56289	C030A102K680J
C3	100103	CAP	CERAM	68 PFD	1000 V	5%	56289	C030A102K680J
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C6	100103	CAP	CERAM	68 PFD	1000 V	5%	56289	C030A102K680J
C7	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C8	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
Q1	200068	TRANS		PNP			80131	2N4250
Q2	200068	TRANS		PNP			80131	2N4250
Q3	200068	TRANS		PNP			80131	2N4250
Q4	200200	TRANS		NPN			21793	200200
Q5	200200	TRANS		NPN			21793	200200
Q6	200068	TRANS		PNP			80131	2N4250
Q7	200298	TRANS		NPN			04713	2N3904
Q8	200298	TRANS		NPN			04713	2N3904
R1	000392	RES	CARBON	3.9 K		5% 1/4W	81349	RC07GF392J
R2	010976	RES	METAL	3.24 K		1% 1/8W	81349	RN55C3241F
R3	040187	POT	CERMET	500 OHM		20% 3/4W	11237	360T501B
R4	040187	POT	CERMET	500 OHM		20% 3/4W	11237	360T501B
R5	010976	RES	METAL	3.24 K		1% 1/8W	81349	RN55C3241F
R6	000392	RES	CARBON	3.9 K		5% 1/4W	81349	RC07GF392J
R7	000392	RES	CARBON	3.9 K		5% 1/4W	81349	RC07GF392J
R8	000392	RES	CARBON	3.9 K		5% 1/4W	81349	RC07GF392J
R9	000513	RES	CARBON	51 K		5% 1/4W	81349	RC07GF513J
R10	000392	RES	CARBON	3.9 K		5% 1/4W	81349	RC07GF392J
R11	000392	RES	CARBON	3.9 K		5% 1/4W	81349	RC07GF392J
R12	000513	RES	CARBON	51 K		5% 1/4W	81349	RC07GF513J
R13	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R14	010926	RES	METAL	1.43 K		1% 1/8W	81349	RN55C1431F
R15	040187	POT	CERMET	500 OHM		20% 3/4W	11237	360T501B
R16	040187	POT	CERMET	500 OHM		20% 3/4W	11237	360T501B
R17	010926	RES	METAL	1.43 K		1% 1/8W	81349	RN55C1431F
R18	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R19	010873	RES	METAL	2.21 K		1% 1/10W	81349	RN55D2211F
R20	010873	RES	METAL	2.21 K		1% 1/10W	81349	RN55D2211F
R21	000822	RES	CARBON	8.2 K		5% 1/4W	81349	RC07GF822J
R22	000132	RES	CARBON	1.3 K		5% 1/4W	81349	RC07GF132J
R23	010969	RES	METAL	1.62 K		1% 1/10W	81349	RN55C1621F
R24	010969	RES	METAL	1.62 K		1% 1/10W	81349	RN55C1621F
R25	000132	RES	CARBON	1.3 K		5% 1/4W	81349	RC07GF132J
R26	000162	RES	CARBON	1.6 K		5% 1/4W	81349	RC07GF162J
R27	000162	RES	CARBON	1.6 K		5% 1/4W	81349	RC07GF162J
R28	000200	RES	CARBON	20 OHM		5% 1/4W	81349	RC07GF200J

406767 – Assy., PCB, DAC *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
U1	230212	INTEGRATED CIRCUIT	27014	74164
U2	230072	INTEGRATED CIRCUIT CERAM	01295	7474
U3	230212	INTEGRATED CIRCUIT	27014	74164
U4	230207	INTEGRATED CIRCUIT	04713	MC1408L-8
U5	230207	INTEGRATED CIRCUIT	04713	MC1408L-8
U7	230190	INTEGRATED CIRCUIT	27014	LM324
VR1	230535	INTEGRATED CIRCUIT	27014	LM329CZ
W1	600245	JUMPER INSULATED		L-2007-1LP
W2	600245	JUMPER INSULATED		L-2007-1LP

406768 – Assy., PCB, REFERENCE

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	100053	CAP	CERAM	56 PFD	1000 V	5%	56289	C030A102J560J
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C4	100051	CAP	CERAM	3 PFD	500 V		71471	TCD-B1-0
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C6	100087	CAP	CERAM	4.7 PFD	100 V	5%	72982	8101-A100-COG4791
C7	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C8	100097	CAP	CERAM	12 PFD	1000 V	5%	56289	C030B102E120J
C9	100018	CAP	CERAM	120 PFD	1000 V	10%	71471	ETCD(N5600)
C10	100019	CAP	CERAM	.002 MFD	1000 V	10%	56289	C023B102F202M
C11	100018	CAP	CERAM	120 MFD	1000 V	10%	71471	ETCD(N5600)
C12	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C14	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C16	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C17	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C18	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C19	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C20	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C21	100006	CAP	CERAM	10 PFD	500 V		71471	TCDI-1(N750)
C22	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C23	130052	CAP	CERAM	2-8 PFD			72982	538006A2-8
C24	100097	CAP	CERAM	12 PFD	1000 V	5%	56289	C030B102E120J
C25	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TCDI-1(N750)
C26	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C27	100006	CAP	CERAM	10 PFD	500 V		71471	TCDI-1(N750)
C28	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C29	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C30	130052	CAP	CERAM	2-8 PFD			72982	538006A2-8
C31	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C32	100097	CAP	CERAM	12 PFD	1000 V	5%	56289	C030B102E120J
C33	100072	CAP	CERAM	3.3±5 PFD	1000 V		56289	C030B102E3R3D
C34	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C35	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C36	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C37	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR1	211083	DIODE	SILICO				81349	1N916B
CR2	211083	DIODE	SILICO				81349	1N916B
CR3	211083	DIODE	SILICO				81349	1N916B
CR4	211083	DIODE	SILICO				81349	1N916B
CR5	211083	DIODE	SILICO				81349	1N916B

406768 – Assy., PCB, REFERENCE *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION				FSC	MANU P/N
L1	310072	CHOKE	RF	2.2 μH	10%	99800	1537-20
L2	310126	CHOKE	RF	.39 μH	10%	24226	10/390μH±10%
L3	310062	CHOKE	RF	22 μH		99800	1537-44
L4	310092	CHOKE	RF	.1 μH		76493	9230-94
L5	310062	CHOKE	RF	22 μH		99800	1537-44
Q1	200037	TRANS	SILICO	NPN		80131	2N3646
Q2	200037	TRANS	SILICO	NPN		80131	2N3646
Q3	200037	TRANS	SILICO	NPN		80131	2N3646
Q4	200037	TRANS	SILICO	NPN		80131	2N3646
Q5	200095	TRANS		NPN		81349	2N3563
Q6	200037	TRANS	SILICO	NPN		80131	2N3646
Q7	200037	TRANS	SILICO	NPN		80131	2N3646
Q8	200200	TRANS		NPN		21793	200200
Q9	200037	TRANS	SILICO	NPN		80131	2N3646
Q10	200200	TRANS		NPN		21793	200200
Q11	200037	TRANS	SILICO	NPN		80131	2N3646
Q12	200195	TRANS	SILICO	NPN		21793	200195
Q13	200195	TRANS	SILICO	NPN		21793	200195
Q14	200037	TRANS	SILICO	NPN		80131	2N3646
R1	000122	RES	CARBON	1.2 K	5% 1/4W	81349	RC07GF122J
R2	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R3	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
W1	600245	JUMPER	INSULATED				L-2007-1LP

406768 – Assy., PCB, REFERENCE *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R4	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R5	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R6	000122	RES CARBON 1.2 K 5% 1/4W	81349	RC07GF122J
R7	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R8	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R9	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R10	000510	RES CARBON 51 OHM 5% 1/4W	81349	RC07GF510J
R11	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R12	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R13	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R14	000201	RES CARBON 200 OHM 5% 1/4W	81349	RC07GF201J
R15	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R16	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R17	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R18	000122	RES CARBON 1.2 K 5% 1/4W	81349	RC07GF122J
R19	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R20	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R21	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R22	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R23	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R24	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R25	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R26	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R27	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R28	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R29	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R30	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R31	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R32	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R33	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R34	000200	RES CARBON 20 OHM 5% 1/4W	81349	RC07GF200J
R35	000241	RES CARBON 240 OHM 5% 1/4W	81349	RC07GF241J
R36	000200	RES CARBON 20 OHM 5% 1/4W	81349	RC07GF200J
R37	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
TP1	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP2	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP3	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
U1	230064	INTEGRATED CIRCUIT CERAM	01295	7404
U2	230028	INTEGRATED CIRCUIT CERAM	01295	7400
Y1	920583	CRYSTAL 9.9988 MHz	21793	920583

406764 – Assy., PCB, DISPLAY

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C4	110141	CAP	TANTA	22 MFD	15 V	20%	05397	T368B226M015AS
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C6	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR1	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR2	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR3	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR4	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR5	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR6	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR7	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR8	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR9	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR10	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR11	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR12	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR13	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR14	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR15	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR16	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR17	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR18	210080	DIODE	LED LAMP, RED				50434	HP5082-4665
CR19	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR20	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR21	210079	DIODE	LED LAMP, YELLOW				50434	HP5082-4555
CR22	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR23	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR24	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR25	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR26	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR27	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR28	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650
CR29	210071	DIODE	LAMP, HI Efficiency Red, Solid State				50434	HP5082-4650

406764 – Assy., PCB, DISPLAY *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION		FSC	MANU P/N
CR30	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR31	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR32	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR33	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR34	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR35	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR36	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR37	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR38	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR39	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR40	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR41	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR42	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR43	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR44	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR45	210071	DIODE	LAMP, HI Efficiency Red, Solid State	50434	HP5082-4650
CR46	210079	DIODE	LED LAMP, Yellow	50434	HP5082-4555
LED 1	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 2	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 3	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 4	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 5	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 6	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 7	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 8	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 9	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 10	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 11	210074	DIODE	LED DISPLAY, YELLOW	50434	HP5082-7660
LED 12	210060	DIODE	DISPLAY, LED, RED	50434	HP5082-7730
LED 13	210075	DIODE	DISPLAY, LED, 3-DIGIT RED	50434	HP5082-7433
LED 14	210075	DIODE	DISPLAY, LED, 3-DIGIT RED	50434	HP5082-7433

406764 – Assy., PCB, DISPLAY *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
Q1	200184	TRANS PNP	04713	MPSA55
Q2	200184	TRANS PNP	04713	MPSA55
Q3	200184	TRANS PNP	04713	MPSA55
Q4	200184	TRANS PNP	04713	MPSA55
Q5	200184	TRANS PNP	04713	MPSA55
Q6	200184	TRANS PNP	04713	MPSA55
Q7	200184	TRANS PNP	04713	MPSA55
Q8	200184	TRANS PNP	04713	MPSA55
Q9	200184	TRANS PNP	04713	MPSA55
Q10	200184	TRANS PNP	04713	MPSA55
Q11	200184	TRANS PNP	04713	MPSA55
Q12	200184	TRANS PNP	04713	MPSA55
Q13	200184	TRANS PNP	04713	MPSA55
Q14	200184	TRANS PNP	04713	MPSA55
Q15	200239	TRANS NPN	04713	MPSA06
Q16	200239	TRANS NPN	04713	MPSA06
Q17	200239	TRANS NPN	04713	MPSA06
Q18	200239	TRANS NPN	04713	MPSA06
Q19	200239	TRANS NPN	04713	MPSA06
Q20	200239	TRANS NPN	04713	MPSA06
Q21	200239	TRANS NPN	04713	MPSA06
Q22	200184	TRANS PNP	04713	MPSA55
Q23	200184	TRANS PNP	04713	MPSA55
Q24	200184	TRANS PNP	04713	MPSA55
Q25	200184	TRANS PNP	04713	MPSA55
Q26	200239	TRANS NPN	04713	MPSA06
Q27	200239	TRANS NPN	04713	MPSA06
Q28	200239	TRANS NPN	04713	MPSA06
Q29	200239	TRANS NPN	04713	MPSA06
Q30	200239	TRANS NPN	04713	MPSA06
Q31	200239	TRANS NPN	04713	MPSA06
Q32	200239	TRANS NPN	04713	MPSA06
Q33	200088	TRANS SILICO PNP	80131	PN4248
Q34	200088	TRANS SILICO PNP	80131	PN4248
Q35	200088	TRANS SILICO PNP	80131	PN4248
Q36	200088	TRANS SILICO PNP	80131	PN4248
Q37	200088	TRANS SILICO PNP	80131	PN4248
Q38	200088	TRANS SILICO PNP	80131	PN4248
Q39	200088	TRANS SILICO PNP	80131	PN4248
R1	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R2	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J

406764 – Assy., PCB, DISPLAY *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R3	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R4	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R5	000151	RES CARBON 150 OHM 5% 1/4W	81349	RC07GF151J
R6	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R7	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R8	000330	RES CARBON 33 OHM 5% 1/4W	81349	RC07GF330J
R9	001775	RES CARBON 33 OHM 5% 1 W	81349	RC32GF330J
R10	001775	RES CARBON 33 OHM 5% 1 W	81349	RC32GF330J
R11	001775	RES CARBON 33 OHM 5% 1 W	81349	RC32GF330J
R12	001775	RES CARBON 33 OHM 5% 1 W	81349	RC32GF330J
R13	001775	RES CARBON 33 OHM 5% 1 W	81349	RC32GF330J
R14	001775	RES CARBON 33 OHM 5% 1 W	81349	RC32GF330J
R15	001775	RES CARBON 33 OHM 5% 1 W	81349	RC32GF330J
R16	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R17	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R18	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R19	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R20	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R21	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R22	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R23	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R24	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R25	000100	RES CARBON 10 OHM 5% 1/4W	81349	RC07GF100J
R26	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R27	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R28	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R29	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R30	000681	RES CARBON 680 OHM 5% 1/4W	81349	RC07GF681J
U1	230208	INTEGRATED CIRCUIT	01295	SN74154N
U2	230209	INTEGRATED CIRCUIT	01295	SN7448N
U3	230065	INTEGRATED CIRCUIT CERAM	07263	7475
U4	230074	INTEGRATED CIRCUIT PLASTIC	07263	7442
U5	230065	INTEGRATED CIRCUIT CERAM	07263	7475
U6	230074	INTEGRATED CIRCUIT PLASTIC	07263	7442
U7	230065	INTEGRATED CIRCUIT CERAM	07263	7475
U8	230065	INTEGRATED CIRCUIT CERAM	07263	7475
U9	230065	INTEGRATED CIRCUIT CERAM	07263	7475
U10	230065	INTEGRATED CIRCUIT CERAM	07263	7475

406764 – Assy., PCB, DISPLAY *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
U11	230209	INTEGRATED CIRCUIT	01295	SN7448N
U12	230030	INTEGRATED CIRCUIT CERAM	01295	7402
U13	230099	INTEGRATED CIRCUIT CERAM	01295	7454
U14	230030	INTEGRATED CIRCUIT CERAM	01295	7402
W1	600245	JUMPER INSULATED		L-2007-1LP
Z1	080003	RES CERMET 2 K NETWORK 2%	11237	750-81-R2K
Z2	080007	RES CERMET 220 OHM NETWORK 2%	11237	761-3-R220
Z3	080007	RES CERMET 220 OHM NETWORK 2%	11237	761-3-R220
Z4	080003	RES CERMET 2 K NETWORK 2%	11237	750-81-R2K
Z5	080011	RES CERMET 1 K 2%	11237	750-81-R1K
Z6	080000	RES CERMET 220 OHM NETWORK 2%	11237	750-81-R220
Z7	080000	RES CERMET 220 OHM NETWORK 2%	11237	750-81-R220
Z8	080006	RES CERMET 68 OHM NETWORK 2%	11237	761-3-R68
Z9	080000	RES CERMET 220 OHM NETWORK 2%	11237	750-81-R220

406831 – Assy., PCB, KEYBOARD

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
A1	730712	KEYBOARD SUBASSEMBLY	21793	730712
CR5	211083	DIODE SILICO	81349	1N916B
CR6	211083	DIODE SILICO	81349	1N916B
CR7	211083	DIODE SILICO	81349	1N916B
CR8	211083	DIODE SILICO	81349	1N916B
CR9	211083	DIODE SILICO	81349	1N916B
S29	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S30	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S31	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S32	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S33	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S34	600805	SWITCH SLIDE 1P3T	79727	GF127L-3W/G-20-60
U1	230214	IC 16 PIN	34649	4003

406832 – Assy., PCB, KEYBOARD

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
A1	730711	KEYBOARD SUBASSEMBLY	21793	730711
CR5	211083	DIODE SILICO	81349	1N916B
CR6	211083	DIODE SILICO	81349	1N916B
CR7	211083	DIODE SILICO	81349	1N916B
CR8	211083	DIODE SILICO	81349	1N916B
CR9	211083	DIODE SILICO	81349	1N916B
S29	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S30	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S31	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S32	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S33	600804	SWITCH SLIDE 1P2T	79727	GF124-3W/G-20-60
S34	600805	SWITCH SLIDE 1P3T	79727	GF127L-3W/G-20-60
U1	230214	IC 16 PIN	34649	4003

406793 – Assy., PCB, 512 MHz PRESCALER

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
B1	406466	CHOKE ASSY	FERRITE BEAD				21793	406466
B2	406466	CHOKE ASSY	FERRITE BEAD				21793	406466
B3	406466	CHOKE ASSY	FERRITE BEAD				21793	406466
B4	406466	CHOKE ASSY	FERRITE BEAD				21793	406466
C1	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C2	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C3	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C4	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C5	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C6	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C7	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C8	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C9	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C10	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C11	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C12	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C13	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C14	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C15	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C16	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C17	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C18	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C19	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C20	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C21	100025	CAP	CERAM	.005 MFD	100 V	20%	72982	835-000-X5V0502Z
C22	130103	CAP	CERAM	.01 MFD	25 V	20%	72982	9ACF-W5R103M
C23	130103	CAP	CERAM	.01 MFD	25 V	20%	72982	9ACF-W5R103M
C24	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C25	130103	CAP	CERAM	.01 MFD	25 V	20%	72982	9ACF-W5R103M
C26	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C27	130103	CAP	CERAM	.01 MFD	25 V	20%	72982	9ACF-W5R103M
C28	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C29	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C30	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C31	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C32	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C33	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C34	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C35	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C36	130103	CAP	CERAM	.01 MFD	25 V	20%	72982	9ACF-W5R103M
C37	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A

406793 – Assy., PCB, 512 MHz PRESCALER *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C38	130103	CAP	CERAM	.01 MFD	25 V	20%	72982	9ACF-W5R103M
C39	130103	CAP	CERAM	.01 MFD	25 V	20%	72982	9ACF-W5R103M
C40	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C41	130103	CAP	CERAM	.01 MFD	25 V	20%	72982	9ACF-W5R103M
C42	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C43	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C44	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C45	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C46	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C47	100062	CAP	CERAM	.01 MFD	100 V	10%	72982	8121-100-W5R0-103K
C48	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C49	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C50	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C51	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C52	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C53	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C54	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C55	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C56	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C57	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C58	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C59	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C60	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR1	210022	DIODE					50434	HP5082-3080
CR2	210022	DIODE					50434	HP5082-3080
CR3	210022	DIODE					50434	HP5082-3080
CR4	210004	DIODE	SILICO				81349	1N4004
CR5	210022	DIODE					50434	HP5082-3080
CR6	210022	DIODE					50434	HP5082-3080
CR7	211083	DIODE	SILICO				81349	1N916B
CR8	211083	DIODE	SILICO				81349	1N916B
CR9	210089	DIODE	LOW OFFSET SCHOTTKY				50434	HP5082-2835
CR10	210089	DIODE	LOW OFFSET SCHOTTKY				50434	HP5082-2835
F1	920054	FUSE		1/10 AMP			71400	BMW1/10

406793 – Assy., PCB, 512 MHz PRESCALER *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
J20	600610	CONN	RECPTLE				98291	50-053-0000
L1	310062	CHOKE	RF	22 µH			99800	1537-44
L2	310062	CHOKE	RF	22 µH			99800	1537-44
L3	310062	CHOKE	RF	22 µH			99800	1537-44
L4	310062	CHOKE	RF	22 µH			99800	1537-44
L5	310062	CHOKE	RF	22 µH			99800	1537-44
L6	310062	CHOKE	RF	22 µH			99800	1537-44
L7	310062	CHOKE	RF	22 µH			99800	1537-44
Q1	200035	TRANS	SILICO	NPN	014		21793	200035
Q2	200011	TRANS	SILICO	PNP	009		21793	200011
Q3	200200	TRANS		NPN			21793	200200
Q4	200200	TRANS		NPN			21793	200200
Q5	200200	TRANS		NPN			21793	200200
Q6	200088	TRANS	SILICO	PNP			80131	2N4248
Q7	200200	TRANS		NPN			21793	200200
R1	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J
R2	001683	RES	CARBON	47 OHM		5% 1/2W	81349	RC20GF470J
R3	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R4	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J
R5	001812	RES	CARBON	270 OHM		5% 1/2W	01121	See Descrpt.
R6	000121	RES	CARBON	120 OHM		5% 1/4W	81349	RC07GF121J
R7	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R8	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J
R9	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J
R10	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R11	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R12	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R13	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J
R14	000510	RES	CARBON	51 OHM		5% 1/4W	81349	RC07GF510J

406793 – Assy., PCB, 512 MHz PRESCALER *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION				FSC	MANU P/N
R15	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R16	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R17	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R18	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R19	040261	POT	CERMET	2 K	20% .5 W	73138	72XW2K
R20	000222	RES	CARBON	2.2 K	5% 1/4W	81349	RC07GF222J
R21	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R22	000123	RES	CARBON	12 K	5% 1/4W	81349	RC07GF123J
R23	000121	RES	CARBON	120 OHM	5% 1/4W	81349	RC07GF121J
R24	000183	RES	CARBON	18 K	5% 1/4W	81349	RC07GF183J
R25	000222	RES	CARBON	2.2 K	5% 1/4W	81349	RC07GF222J
R26	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R27	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R28	000683	RES	CARBON	68 K	5% 1/4W	81349	RC07GF683J
R29	000222	RES	CARBON	2.2 K	5% 1/4W	81349	RC07GF222J
R30	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R31	040265	POT	CERMET	50 K	20% .5 W	73138	72XW50K
R32	000751	RES	CARBON	750 OHM	5% 1/4W	81349	RC07GF751J
R33	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R34	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R35	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R36	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R37	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R38	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R39	000153	RES	CARBON	15 K	5% 1/4W	81349	RC07GF153J
R40	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R41	000682	RES	CARBON	6.8 K	5% 1/4W	81349	RC07GF682J
R42	000241	RES	CARBON	240 OHM	5% 1/4W	81349	RC07GF241J
R43	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
TP1	600786	POST, MACHINE APPLIED STRIP				00779	1-87022-0
TP2	600786	POST, MACHINE APPLIED STRIP				00779	1-87022-0
U1	230119	INTEGRATED CIRCUIT			μA741	07263	741HC
U2	230273	INTEGRATED CIRCUIT				52648	SP8630B
U3	230205	INTEGRATED CIRCUIT				04713	MC10102P
U4	230183	INTEGRATED CIRCUIT				25403	ATF419
U5	230182	INTEGRATED CIRCUIT				25403	ATF417

406772 – Assy., REAR PANEL

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C201	100111	CAP CERAM .01 MFD 2000 V	71471	HVD6-2KV
C202	100111	CAP CERAM .01 MFD 2000 V	71471	HVD6-2KV
B101	920843	FAN 115 VAC-50/60 Hz		760-126LF-2182-11115
F201	920776	FUSE SLO-BLO 1-1/4 AMP 250 V	71400	MDX1-1/4
J201	600808	CONN BNC	02660	31-010
J202	600808	CONN BNC	02660	31-010
J203	600808	CONN BNC	02660	31-010
J204	600808	CONN BNC	02660	31-010
J205	600808	CONN BNC	02660	31-010
J206	600808	CONN BNC	02660	31-010
J210	600795	CONN	95238	6J1
J213	600808	CONN BNC	02660	31-010
J214	600586	BINDING POST, WHITE	32767	820-25
J215	600587	BINDING POST, BLACK	32767	820-45
J216	600586	BINDING POST, WHITE	32767	820-25
S201	600872	SWITCH, 3P.3P	79727	G-168-S
T201	730669	TRANSFORMER POWER	21793	730669
W201	600245	JUMPER INSULATED		L-2007-1LP
W202	600245	JUMPER INSULATED		L-2007-1LP

406771 – Assy., FRONT PANEL

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
S101	601109	SWITCH ROCKER DPST 6A/250V		1545-0102

406875 – Assy., PCB, Programmable Sync. Window & Sel. Gate Control (Option 06P)

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C3	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
J1	920735	SOCKET, IC		16 P			71785	133-51-02-006
J2	920734	SOCKET, IC		14 P			00779	583527-1
							71785	133-51-02-003
R1	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
U1	230346	IC	DUAL 4 TO 1 MULTIPLEXER				01295	74LS157
U2	230193	IC	14 DIP, NAND GATE				01295	SN74LS00N
U3	230234	IC	14 DIP, HEX INVERTER				01295	SN74LS04N
U6	230193	IC	14 DIP, NAND GATE				01295	SN74LS00N
Z1	080002	RES	CERMET	500 OHM	Network	2% 8P.7R	11236	750-81-R500Ω

406894 – Assy., PCB, SIGNAL CONDITIONER, CHANNEL "A" (Option 07)

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C27	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR15	211083	DIODE	SILICO		1N916B		81349	1N916B
K8	310125	RELAY	REED	1 Form A	5 V		21793	310125
R60	012032	RES	METAL	51.1 OHM		1% 1/2W	81349	RN70D51R1F

406895 – Assy., PCB, SIGNAL CONDITIONER, CHANNEL "B" (Option 07)

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C27	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR15	211083	DIODE	SILICO		1N916B		81349	1N916B
K8	310125	RELAY	REED	1 Form A	5 V		21793	310125
R60	012032	RES	METAL	51.1 OHM		1% 1/2W	81349	RN70D51R1F

406930 – Assy., PCB, ADDRESS (Option 55)

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
S202	600814	SWITCH 6SPST	11237	206-6

406942 – Assy., INTERFACE, HIGH SPEED COMPUTER, OPTION 56

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
P211	600871	PLUG 36 PIN	02660	57-30360
P212	600871	PLUG 36 PIN	02660	57-30360
U8	230424	IC ROM MOS 16K (2Kx8)	27014	MM2316E

406817 – Assy., PCB, HIGH SPEED COMPUTER INTERFACE, OPTION 56

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C2	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C3	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C4	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C5	100080	CAP	CERAM	.05 MFD	100 V	20%	56289	C023A101L503M
C6	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C7	101641	CAP	CERAM	470 PFD	500 V	10%	71471	SCD1X5F
C8	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C9	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C10	100024	CAP	CERAM	.1 MFD	25 V		72982	5815-000Y5U104Z
C11	101098	CAP	CERAM	330 PFD	500 V	10%	56289	10TS-T33
C12	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C13	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C15	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C16	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C17	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C18	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
R1	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R2	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R3	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R4	000361	RES	CARBON	360 OHM		5% 1/4W	81349	RC07GF361J
R5	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R6	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R8	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R9	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R10	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R11	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R12	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R13	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R14	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R15	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
S1	600731	SWITCH	SLIDE, DPDT				79727	G126
U1	230210	INTEGRATED CIRCUIT					01295	SN74165N
U2	230210	INTEGRATED CIRCUIT					01295	SN74165N
U3	230330	INTEGRATED CIRCUIT					27014	74LS367
U4	230212	INTEGRATED CIRCUIT					27014	74164
U5	230330	INTEGRATED CIRCUIT					27014	74LS367
U6	230238	INTEGRATED CIRCUIT					27014	74LS164

406817 – Assy., PCB, HIGH SPEED COMPUTER INTERFACE, OPTION 56 *continued*

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
U7	230080	INTEGRATED CIRCUIT PLASTIC	07263	7496
U8	230212	INTEGRATED CIRCUIT	27014	74164
U9	230238	INTEGRATED CIRCUIT	27014	74LS164
U10	230330	INTEGRATED CIRCUIT	27014	74LS367
U11	230238	INTEGRATED CIRCUIT	27014	74LS164
U12	230330	INTEGRATED CIRCUIT	27014	74LS367
U13	230330	INTEGRATED CIRCUIT	27014	74LS367
U14	230028	INTEGRATED CIRCUIT CERAM	01295	7400
U15	230064	INTEGRATED CIRCUIT CERAM	01295	7404
U16	230194	INTEGRATED CIRCUIT	01295	SN74LS74N
U17	230135	INTEGRATED CIRCUIT	01295	SN7427N
U18	230105	INTEGRATED CIRCUIT	01295	SN7417
U19	230309	INTEGRATED CIRCUIT	01295	SN74LS192
U20	230309	INTEGRATED CIRCUIT	01295	SN74LS192
U21	230028	INTEGRATED CIRCUIT CERAM	01295	7400
U22	230064	INTEGRATED CIRCUIT CERAM	01295	7404
U23	230237	INTEGRATED CIRCUIT	01295	SN74LS123N
U24	230237	INTEGRATED CIRCUIT	01295	SN74LS123N
U25	230194	INTEGRATED CIRCUIT	01295	SN74LS74N
U26	230030	INTEGRATED CIRCUIT CERAM	01295	7402
U27	230098	INTEGRATED CIRCUIT CERAM	01295	7451
Z1	080005	RESISTOR CERMET 10 K NETWORK 2%	11237	750-61-R10K
Z2	080005	RESISTOR CERMET 10 K NETWORK 2%	11237	750-61-R10K
Z3	080005	RESISTOR CERMET 10 K NETWORK 2%	11237	750-61-R10K
Z4	080005	RESISTOR CERMET 10 K NETWORK 2%	11237	750-61-R10K
Z5	080005	RESISTOR CERMET 10 K NETWORK 2%	11237	750-61-R10K

406860 – Option 71, 220V OPERATION FOR 9000 COUNTER

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
F201	920205	FUSE GLASS .75 A 250 V	75915	3AG3/4ASB

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5/88

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12/87

REPAIR REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline and include a copy with your instrument to be sent to your local Racal-Dana repair facility.

Model Number _____ Options _____ Date _____

Serial Number _____ P. O.# _____

Company Name _____

Address _____

City _____ State _____ Zip Code _____

Contact _____ Phone Number _____

1. Describe, in detail, the problem and symptoms you are having.

_____

_____

2. If you are using your unit on the bus, please list the program strings used and the controller type, if possible.

_____

_____

3. List all input levels, and frequencies this failure occurs.

_____

_____

4. Indicate any repair work previously performed.

_____

_____

5. Please give any additional information you feel would be beneficial in facilitating a faster repair time. (I. E., modifications, etc.)

_____

_____